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I Roger P. Lewis, whose address is 42 Bird Street North,
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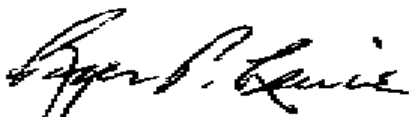
I am well acquainted with the English and Japanese languages and
have in the past translated numerous English/Japanese documents
of legal and/or technical content.

I hereby certify that the Japanese translation of the attached
documents identified as:

JP Hei 7 - 183518
Semiconductor Device and the Production Method Thereof

is true, and that all statements of information and belief are
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SINCERELY,



ROGER P. LEWIS

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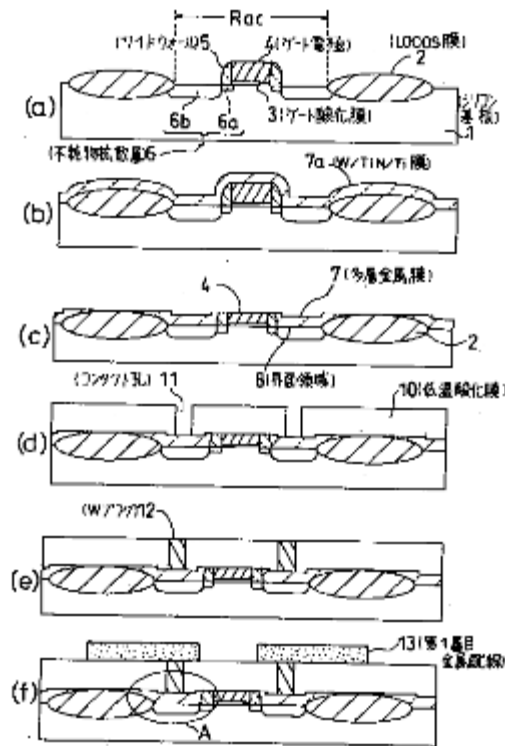
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[Translation of 1st page of source document continued on 2/2]



[Legend for Figure in the lower left of the 1st source document page]

(a) (サイドウォール) 5	(Side Wall) 5
4 (ゲート電極)	4 (Gate Electrode)
(LOCOS膜) 2	(LOCOS Film) 2
3 (ゲート酸化膜)	3 (Gate Oxide Film)
(シリコン基板) 1	(Silicon Substrate) 1
(不純物拡散層) 6	(Impurity Diffusion Layer) 6
(b) 7a (W/TiN/Ti 膜)	(b) 7a (W/TiN/Ti Film)
(c) 7 (多層金属膜)	(c) 7 (Multi-Layer Metal Film)
8 (界面領域)	8 (Surface Region)
(d) (コンタクト孔) 11	(d) (Contact Hole) 11
10 (低温酸化膜)	10 (Low Temperature Oxide Film)
(e) (W プラグ) 12	(e) (W Plug) 12
(f) 13 (第 1 層目金属配線)	(f) 13 (1 st Metal Interconnect)

【Scope of Claims】

【Claim 1】 A production method for semiconductors that include a plurality of MISFET and which is characterized by the fact that it is equipped with
a process for the formation of an outer periphery separation portion of the active region of the semiconductor substrate at a location that is higher than the surface of the above described active region,
a process for the introduction of threshold value control impurity of the above described MISFEET [sic],
a process for the formation, within the above described active region, of the gate electrode and gate insulation film of the above described MISFET,
a process for the formation of side walls, which are composed of insulation material, on both sides of the above described gate electrode,
a process for the formation of the above described MISFET's drain source, which becomes the 2 impurity diffusion layers,
a process for the deposition of a metal film on the entire surface of the substrate after the formation of the above described gate electrode, side wall and outer periphery separation part, [and]
a process by which a portion of the above described metal films, the outer periphery portion and the gate electrode are removed, and when the chemical machine polishing is completed, within the polished surface, the metal films on the above described impurity diffusion layer is surrounded by the above described gate electrode and outer periphery separation part so as to electrically isolate each [metal film].

【Claim 2】 A production method for semiconductors that described in Claim 1 and that is characterized by the fact that it is equipped, in the production method for semiconductors,
so that a LOCOS film is formed in the process for the formation of the above described outer periphery separation part, [and]
in the process wherein the above described chemical machine polishing is performed, when the chemical machine polishing is completed, within the polished surface, each of the metal films on the above described impurity diffusion layer is surrounded by the above described side wall and LOCOS film.

【Claim 3】 A production method for semiconductors that is described in Claim 1 that is characterized by the fact that it is equipped, in the production method for semiconductors,
so that in the process for the formation of the above described outer periphery separation part, after the formation on the semiconductor substrate of a groove that surrounds the above described active region a LOCOS film is formed in the process for the formation of the above described outer periphery separation part, [and]
so that in the process for performing the chemical machine polishing, when the chemical machine polishing is completed, within the polished surface, each of the metals films on each of the above described impurity diffusion layers are surrounded by each of the above described side wall and the above described embedded oxide film.

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