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(54) MOS semiconductor device production method
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SPECIFICATION

1. Title of the invention

MOS semiconductor device production method

2. Claims

(1) An MOS semiconductor device production method, comprising a step of selectively etching element separation regions of a semiconductor substrate to form grooves, a step of doping the grooves with an impurity giving the same conductivity type as the substrate to form an inversion prevention layer, a step of embedding a first insulating film in the grooves and making the top surface of the insulating film higher than the surface of the substrate, a step of selectively forming a gate electrode on an element formation region of the substrate via a gate insulating film and making the step between the top surface of the electrode and the substrate surface smaller than the step between the first insulating film and the substrate surface, a step of forming a second insulating film on the sidewalls of the steps by self-alignment, and a step of doping the substrate surface with an impurity giving the conductivity type opposite to the substrate using the first and second insulating films as a mask to form source/drain regions.

(2) The MOS semiconductor device production method according to Claim 1, wherein the step of forming a second insulating film consists of depositing a second insulating film on the entire surface and then overall etching the insulating film by reactive ion etching to leave the insulating film only on the sidewalls of the steps.

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3. Detailed explanation of the invention

[Scope of the invention]

The present invention relates to an MOS semiconductor device production method and particularly relates to a method of producing a MOS semiconductor device in which a number of MOS transistors are highly integrated.

[Technological background and problems]

Recently, semiconductor devices such as ICs and LSIs have increasingly been improved in integration and density. For example, MOS semiconductor memories are currently mass-produced with the highest integration of 64 Kbit dynamic RAM and the progress to higher integration of 256 Kbit dynamic RAM and even 1M bit dynamic RAM will be made with no doubt.

As factors of hampering higher integration on a semiconductor device, issues arise in microfabrication techniques. Particularly, the accuracy of stacking layers forming transistors is a factor of diminishing increase in the number of elements per unit area on a semiconductor substrate. Therefore, if the accuracy of stacking is determined with absolute accuracy, in other words, if the positions of elements are determined without taking into account stacking errors of the layers, higher integration can be achieved. In that sense, the polysilicon gate channel length self-alignment technique is among typical techniques currently practiced. This method comprises, as shown in a plane view of the MOS transistor in Fig. 1 (a) and a cross-sectional view at the arrowed line L-L in Fig. 1 (b), forming an oxide film in element separation regions by selective oxidization to insulate and separate each element formation region, forming a polysilicon gate electrode on the element formation region via a gate oxide film, and ion-injecting or diffusing from above the polysilicon gate electrode an impurity giving the conductivity type opposite to the substrate to form source/drain regions. Here, in the figures, the reference number 1 presents an Si substrate; 2, an element separation oxide film; 3, an inversion prevention layer; 4, a gate oxide film; 5, a gate electrode; 6 and7, source/drain regions; 8, an interlayer insulating film; and 9, a wiring Al film. In this method, no impurity is introduced under the gate electrode 5 and this portion serves as a channel region, and self-aligned with the gate electrode position, the source/drain are formed, whereby no positional shift with

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respect to the gate electrode 5, source 6, and drain 7 occurs. Therefore, higher integration is accordingly achieved.

However, the above kind of method has the following problem. In other words, in a MOS transistor produced by the above method, the inversion prevention layer 3 formed by doping of an impurity giving the same conductivity type as the substrate 1 under the element separation oxide film 2 makes contact at portions A with the source/drain regions 6 and 7 formed by doping the element formation region with an impurity giving the conductivity type opposite to the substrate 1. The impurity concentration is approximately 1x1017 [cm-3] in the inversion prevention layer 3 and approximately 5x1019 [cm-3] in the source/drain 6 and 7; PN junctions of two high concentration impurities are created. Therefore, the depletion layer at the portions A has a very small thickness of approximately 0.1 [µm]. On the other hand, the depletion layer at flat portions (portions C) shown in Fig. (b) can be approximately 1 [µm] or larger in thickness by using a high resistance substrate. Then, the junction capacitance is several times larger in value at the portions A than at the flat portions C. This is a major factor of aggravating the circuit properties of various kinds of semiconductor devices.

The above problem is discussed hereafter using an MOS dynamic memory by way of example. Fig. 2 explains the structure of a currently-used conventional MOS dynamic memory, showing the planar structure of a memory cell part of the folded bit line arrangement using Al bit lines 21. Here, the reference number 22 presents word lines serving as the gate electrode of the transfer gate; 23, a cell capacitor; and 24, a first-layer polysilicon window forming an electrode of the cell capacitor 23. The charge stored in the cell capacitor 23 is transferred to the bit line 21 via the transfer gate. In this regard, it is desirable to increase the capacitance CS of the cell capacitor 23 relative to the stray capacitance CB of the bit line 21 in order to increase the potential difference between the bit line and enter large signals into the sense amplifier. The stray capacitance CB of the bit line 21 is determined by the junction capacitance Ca of a drain part 25 of the transfer gate, the capacitance Cb between the gate and drain, the capacitances between the other gate and bit line and between the capacitor electrode and bit line, and the like. Among these, the capacitances excluding Ca and Cb can be diminished by increasing the interlayer

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insulating films. However, the capacitances Ca and Cb are determined by the processing steps and are difficult to diminish in value. Therefore, assuming that the bit line capacitance is determined by the capacitances Ca and Cb and CS is constant, the value CS/CB defining the sensitivity of the sense amplifier is determined mostly by the values of Ca and Cb. In other words, it is desirable to diminish the values of Ca and Cb as much as possible in order to increase the sensitivity of the sense amplifier.

Here, the junction capacitance Ca of the drain part of the transfer gate is mostly determined by the junction capacitance between the element separation region end and drain as described above. Therefore, the sensitivity of the sense amplifier can be improved by diminishing this junction capacitance. On the other hand, Cb is the capacitance between the part of the source/drain region that laterally extends under the gate and the gate in the regions B shown in Fig. 1 (a) and (b). It is also desirable to diminish Cb. The cell part of an MOS dynamic memory is described above. The above-described matters can apply to conventional integrated circuits. The source/drain stray quantity is determined by the junction capacitance with the field end, and if this is reduced, the circuit properties can significantly be improved.

However, as long as the current selection oxidization element separation technique and gate polysilicon self-alignment technique are used, increase in the junction capacitance at the field region ends is inevitable.

[Objective of the invention]

The objective of the present invention is to provide a MOS semiconductor device production method making it possible to significantly reduce the junction capacitance between the source/drain region and substrate at the element separation region ends of a MOS transistor and concurrently reduce the capacitance between the source/drain region and gate and thereby contributing to much smaller elements and their higher integration.

[Summary of the invention]

The present invention is summarized as follows. Using an element separation method of embedding an insulating film such as a CVD-SiO_2 film in the element separation regions (the BOX method), a field insulating film is embedded to a level higher than the surface of

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the substrate and the step between the element separation insulating film and the substrate surface is made larger than the step between the gate electrode formed later and the substrate surface, and an insulating film having a width proportional to the magnitudes of the steps is formed on the sidewalls of the steps by self-alignment, which is followed by doping of an impurity to form a source/drain so that the impurity layer makes contact with the undersides of the gate electrode ends and makes no contact with the inversion prevention layer.

In other words, the present invention provides a method of producing an MOS semiconductor device, comprising the steps of selectively etching element separation regions of a semiconductor substrate to form grooves, doping the grooves with an impurity giving the same conductivity type as the substrate to form an inversion prevention layer, embedding a first insulating film in the grooves and making the top surface of the insulating film higher than the surface of the substrate, selectively forming a gate electrode on an element formation region of the substrate via a gate insulating film and making the step between the top surface of the electrode and the substrate surface smaller than the step between the first insulating film and the substrate surface, forming a second insulating film on the sidewalls of the steps by self-alignment, and doping the substrate surface with an impurity giving the conductivity type opposite to the substrate using the first and second insulating films as a mask to form source/drain regions.

[Efficacy of the invention]

The present invention uses an insulating film formed on the sidewalls of the steps of the element separation insulating film and gate electrode as a mask in doping of an impurity to form a source/drain, whereby it is possible to prevent contact between the source/drain and inversion prevention layer and significantly reduce the junction capacitance between the source/drain and substrate at the element separation region ends. Thus, the stray capacitance of the circuit nodes connected to the source or drain is reduced, whereby high-speed signal response is possible, and it is useful for significantly improving the circuit operation speed. Moreover, it is also useful for improving the sensitivity of the sense amplifier of a dynamic memory. Furthermore, if the sensitivity of the sense amplifier is kept constant, the capacitance of the cell capacitor can also be reduced in

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