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(54) Title of the Invention: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

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Specification

Title of the Invention: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

Claims:

1. A method for a semiconductor device, comprising steps of:

   forming of trench separation regions comprising a flange part in a semiconductor substrate, respectively;

   forming a silicide layer on the surface of the semiconductor substrate; and

   forming of diffusion layers under the silicide layer.

2. The method for a semiconductor device according to claim 1, wherein

   the diffusion layers are formed by solid-phase diffusion from the silicide layer.

3. A method for a semiconductor device, comprising steps of:

   forming of separation regions on a semiconductor substrate by selective oxidation;

   forming a silicide layer on the surface of the semiconductor substrate; and

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forming of diffusion layers under the silicide layer by oblique ion implantation.

4. A method for a semiconductor device, comprising steps of:

forming of separation regions on a semiconductor substrate by selective oxidation;

forming a silicide layer on the surface of the semiconductor substrate; and

oblique ion implantation of impurities into the silicide layer, and forming of diffusion layers by solid-phase diffusion from the silicide layer.

DETAILED DESCRIPTION OF THE INVENTION

[Industrial field of application]

The present invention relates to a method for manufacturing a semiconductor device having diffusion layers under a silicide layer.

[Summary of the Invention]

The present invention is a method for manufacturing a semiconductor device having diffusion layers under a silicide layer so as to achieve reduction of a junction leakage current and improvement of junction withstand voltage, by having a step to form trench separation regions having a flange part on a semiconductor substrate, respectively; a step to form a silicide layer on the surface of the semiconductor substrate; and a step to form diffusion layers under a silicide layer.

Further, in the manufacturing method of the present invention above, the reduction of a junction leakage current and the improvement of junction withstand voltage are achieved by forming the diffusion layers by solid-phase diffusion from the silicide layer.

Further, the present invention is a method for a semiconductor device so as to achieve reduction of a junction leakage current and improvement of junction withstand voltage, by having a step to form separation regions on a semiconductor substrate by selective oxidation; a step to form a silicide layer on the surface of the semiconductor substrate; and a step to form diffusion layers under the silicide layer by oblique ion implantation.

In addition, the present invention is a method for a semiconductor device, so as to achieve further reduction of a junction leakage current and further improvement of junction withstand voltage, by having a step to form separation regions on a semiconductor substrate by selective oxidation; a step to form a silicide layer on the surface of the semiconductor substrate; and a step to obliquely implant impurity ions into the silicide layer, and to form diffusion layers by solid-phase diffusion from the silicide layer.

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[Prior Art]

Recently, in association with the increase of information, speed-up of IC, which is used for a computer element, is in demand to process a massive volume of data. As one method for this IC speed-up, a titanium salicide technology is attracting attention. For example, when an inverter CMOS ring oscillator is produced with a 0.5 μm rule, response speed without using any salicide is 90 psec, but it has already known that the speed will be increased to approximately 60 psec if titanium silicide is used.

In the meantime, a necessity of a high-voltage transistor is increased in association with miniaturization and diversification of semiconductor elements, and high-pressure resistance of an MOS transistor is emphasized especially in a Bi-CMOS transistor. The titanium salicide technology is used for speed-up in this MOS transistor, as well.

Fig. 14 shows one example of a conventional MOS transistor using titanium salicide. In this drawing, (1) represents a first conductive-shaped silicon substrate and (2) represents an element separation region by selective oxidation (LOCCS), and a gate electrode (4) with, for example, polycrystalline is formed on the surface of the substrate (1) via a gate insulating film (3), and, second conductive-shaped diffusion layers (5) and (6) to be a source and a drain across the gate electrode (4), respectively. A titanium silicide layer (i.e., titanium salicide) (7) is selectively formed on these diffusion layers (5) and (6), and a source electrode (9) and a drain electrode (9), for example, made of aluminum, are connected via contact holes of an interlayer insulating film (8), respectively.

Such MOS transistor using titanium salicide is disclosed in Japanese Patent Application Laid-Open No. S63-84064, as well.

[Problem to be Solved by the Invention]

Now, in the MOS transistor described above, deterioration of voltage resistance and a leakage current at a junction part have become problems. As causes of the deterioration of voltage resistance and the leakage current at a junction part in the MOS transistor, ones due to an effect of ion implantation damage (crystal defect) (13) at the time of forming the source/drain diffusion layers (5) and (6) using an ion implantation method as shown in Fig. 15 and due to a silicon crystal defect (14) on the interface between the element separation region (2) and the silicon substrate (1) have been discovered. In addition, when a titanium silicide (TiSi2) layer (7) is selectively formed on the surfaces of the diffusion layers (5) and (6), if the conventional configuration is used, it has already been confirmed that a junction leakage current is increased due to diffusion of titanium along an end edge of the element separation region (2) as shown in Fig. 16, and the junction withstand voltage is deteriorated according to experiments.

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In light of the issues above, in a semiconductor device having diffusion layers under a silicide layer, the present invention is to provide a method for manufacturing a semiconductor device enabling reduction of the junction leakage current and improvement of the junction withstand voltage.

[Means for Solving the Problem]

The method for manufacturing a semiconductor device relating to the present invention includes a step to form trench separation regions (25) having a flange part (29a) (or (25a)) on a semiconductor substrate (21); a step to form a silicide layer (31) on a surface of the semiconductor substrate; and a step to form diffusion layers (32) and (33) under the silicide layer (31). Here, the order of the formation step of the silicide layer (31) and the formation step of the diffusion layers (32) and (33) is reversible. Further, for the formation of the diffusion layers (32) and (33), an ion implantation method, a solid-phase diffusion method and the like are usable.

Further, the present invention is constituted so as to form the diffusion layers (32) and (33) by solid-phase diffusion from the silicide layer (31) in the manufacturing method above.

Further, the method for manufacturing a semiconductor device relating to the present invention includes a step to form separation regions (51) on a semiconductor substrate (21) due to selective oxidation; a step to form a silicide layer (31) on a surface of the semiconductor substrate; and a step to form diffusion layers (32) and (33) under the silicide layer (31) by oblique ion implantation. Here, the order of the formation step of the silicide layer (31) and the formation step of the diffusion layers (32) and (33) is reversible.

In addition, the method for manufacturing a semiconductor device relating to the present invention includes a step to form separation regions (51) on a semiconductor substrate (21) due to selective oxidation; a step to form a silicide layer (31) on a surface of the semiconductor substrate; and a step to obliquely implant impurities (38) into the silicide layer (31) and to form diffusion layers (32) and (33) by solid-phase diffusion.

[Operation]

According to the First Invention, since the trench separation regions (25) having a flange part (29a) (or (25a)) are formed on the semiconductor substrate (21) and the silicide layer (31) is formed on the surface of the semiconductor substrate, the formation of the silicide layer (31) along an interface between the trench separation regions (25) and semiconductor substrate (21) is prevented by the flange parts (29a) (or (25a)), and the joint leakage current is reduced and the joint withstand voltage is also improved [at the junction part].

According to the Second Invention, since the diffusion layers (32) and (33) are formed by the solid-phase diffusion from the silicide layer (31) where impurities have been further induced in the First Invention, a crystal defect due to the ion implantation will not occur, and in addition, the junction leakage current is reduced and the junction withstand voltage is improved.

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According to the Third Invention, since the diffusion layers (32) and (33) are formed by oblique ion implantation into the semiconductor substrate (21) where the separation regions (51) are formed by selective oxidation, deep diffusion layers (32) and (33) are formed even at the end portion of the separation region (51), and the position of the junction part becomes deeper than the position diffused along the end portion of the separation region (51). Therefore, the titanium diffusion along the end portion of the separation region (51), i.e., the junction leakage current based on the silicide layer (31) is reduced, and the junction withstand voltage is also improved.

According to the Fourth Invention, the silicide layer (31) is formed on the surface of the semiconductor substrate (21) where the separation regions (51) due to the selective oxidation have been formed, and impurities are obliquely implanted into the silicide layer (31) and the diffusion layers (32) and (33) are formed by the solid-phase diffusion from this silicide layer (31); thus, a junction part is formed at a position, which is deeper than the silicide layer (31), even under the end part of the separation region (51), and because of the phase-solid diffusion, a crystal defect like the one due to the ion implantation will never occur. Therefore, the junction leakage current is further reduced compared to the Third Invention, and, the junction withstand voltage is further improved.

[Embodiment]

Hereafter, embodiments of the method for manufacturing a semiconductor device according to the present invention are explained with reference to drawings. Furthermore, each embodiment indicates a case of applying [the present invention] to manufacturing of an MOS transistor.

Fig. 1 shows the First Embodiment of the present invention. First, as shown in Fig. 1A, trenches (22) for inter-element separation are formed in a first principal surface of a first conductive-shaped (for example, p-shaped or n-shaped) silicon substrate (21).

Next, as shown in Fig. 1B, an SiO2 layer (23) is formed including the substrate surface so as to implant SiO2 into the trenches (22) using, for example, a bias EDR plasma CVD method or the like. After that, resist masks (24) are formed on the SiO2 layer (23) corresponding to the trenches (22), respectively. Then, the SiO2 layer (23) other than the trenches (22) is selectively removed by, for example, etching back, and the so-called trench separation regions (25) where an upper part is projected from the principal surface of the substrate (21), respectively, are formed as shown in Fig. 1C.

Next, as shown in Fig. 1D, a gate electrode (28), for example, made from polycrystalline silicon, is formed on a predetermined area of an element formation region (26) separated by the trench separation regions (25) via a gate insulating film (27). Furthermore, the gate electrode (28) may be formed with tungsten silicide or others. Next, as shown in Fig. 1E, after a SiO2 layer (29) is deposited and formed on a front surface, the SiO2 layer (29) is etched back by anisotropic etching, such as reactive ion etching (RIE), and SiO2 sidewall parts (29a) are formed on the sidewalls on upper-side protrusion parts of the trench separation regions (25). At this time,

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