Filed on behalf of Godo Kaisha IP Bridge 1

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

_____

Case IPR2016-01246[1]
U.S. Patent No. 7,126,174

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# DECLARATION OF DR. E. FRED SCHUBERT, PH.D. IN SUPPORT OF PATENT OWNER'S RESPONSE

[1] Case IPR2016-01247 has been consolidated with this proceeding.

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I, E. Fred Schubert, declare as follows:

**Introduction**

1. My name is Dr. E. Fred Schubert. I have been asked to submit this declaration on behalf of Godo Kaisha IP Bridge 1 ("IP Bridge" or "Patent Owner") in connection with a Petition for *Inter Partes Review* of U.S. Patent No. 7,126,174 ("the '174 patent"), which I understand was submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office by petitioner Taiwan Semiconductor Manufacturing Company Ltd. ("TSMC").

2. I have been retained as a technical expert by IP Bridge to study and provide my opinions on the technology claimed in, and the patentability or non-patentability of, claims 1-3, 5-7, 9-12, and 14-18 in the '174 patent ("the Challenged Claims").

3. I understand the '174 patent is related to U.S. Patent Nos. 6,967,409 (the '409 patent), 6,709,950 (the '950 patent), and 6,281,562 (the '562 patent) and also claims the benefit of priority to two Japanese applications, JP 7-192181, which was filed on July 27, 1995, and JP 7-330112, which was filed on December 19, 1995.

**Summary Of Opinions**

4. I have reviewed the '174 patent, associated prior art, the TSMC Petition, the Declaration of Dr. Banerjee, as well as references cited therein. I

understand that the Petitioner and its expert, Dr. Banerjee, express the following contentions:

5. *First*, Petitioner and its expert contend that LOCOS isolation and trench isolation are interchangeable and one could simply substitute LOCOS isolation with trench isolation.

6. *Second*, Petitioner and its expert offer four combinations, (1) *Lee* and *Noble*, (2) *Lee* and *Ogawa*, (3) *Lowrey* and *Noble*, (4) *Lowrey* and *Ogawa*, and contend that the substitution of *Lee*'s LOCOS isolation or *Lowrey*'s LOCOS isolation, with either *Noble*'s or *Ogawa*'s trench isolation would result in the claimed invention of the '174 patent.

7. Based on my experience and knowledge in the field and based on my review of the documents, I express my opinions as follows:

8. *First*, it is my opinion that LOCOS isolation and trench isolation are substantially different structures thereby requiring that their fabrication processes as well as the processes that they are integrated into must be modified substantially when transitioning from LOCOS isolation to trench isolation.

9. *Second*, it is my opinion that a simple substitution of LOCOS isolation with trench isolation, without a detailed re-engineering of a fabrication process, is generally not obvious, not possible, and if done nonetheless, would result in a non-working Si IC device.

10. Accordingly, it is my opinion that the '174 patent is not obvious based on the prior art asserted by Petitioner and its expert. That is, the '174 patent is not obviated by the *Lee* and *Noble*, *Lee* and *Ogawa, Lowrey* and *Noble*, or *Lowrey* and *Ogawa* combinations.

**Background And Qualifications**

Previous Expert Witness Experience

11. I have served as a technical expert witness since the late 1990s. My expert activity included semiconductor materials, processing, devices, packaging, and systems. I have worked on behalf of Plaintiffs and Defendants, on behalf of domestic companies and foreign companies, and in proceedings at the USPTO (including *inter partes reviews*), District Court, and the International Trade Commission (ITC). My work included mostly utility patent cases, but also included design patent cases, a case of alleged misappropriation of a trade secret, and a case of alleged mishandling of a patent application.

Compensation

12. I am compensated at my customary rate of $500 per hour worked on the case plus reasonable and customary expenses. My compensation does not depend on the outcome of the *inter partes review.*

Background

13. I am currently a Professor in the Department for Electrical, Computer, and Systems Engineering at the Rensselaer Polytechnic Institute (RPI) located in Troy, New York.

14. I received a Master's Degree in Electrical Engineering from the University of Stuttgart, Germany, in 1981. While working towards my Master's Degree in Electrical Engineering, I had hands-on experience working in a silicon IC fabrication facility, working on silicon integrated piezo-resistive sensors. I received a Ph.D. degree in Electrical Engineering from the University of Stuttgart, Germany, in 1986. While working towards my Ph.D., in 1982, I worked as a summer intern at IBM's silicon integrated circuit fabrication facility in Böblingen, Germany. In this capacity, my work specifically focused on photolithography and mask design. My dissertation was titled "Modern Schottky Gate Field Effect Transistor Devices Made of III-V Semiconductors." Subsequent to my education, starting in 1985, I worked in industry, at AT&T Bell Laboratories in Holmdel and Murray Hill, New Jersey, for ten years. The transistor was invented at Bell Labs (in 1949) and the Labs were subsequently recognized as one of the world's premier industrial research laboratories. From 1990-1995, while at AT&T Bell Labs, I worked in the silicon integrated circuit fabrication facility. This facility was nicknamed "Blue Zoo" fabrication facility and was located in Murray Hill, New

Jersey. While working in this facility, my work focused on the doping of silicon, on the demonstration of shallow junctions, and on the design and fabrication of silicon MOSFETs, including LDD MOSFETs that employ gate sidewall spacers for a better control of the dopant distribution.

15. In 1995, I joined academia. My first position was at Boston University (Boston MA) where I worked as a full professor for seven years. In 2002, I joined RPI as a distinguished professor, the Wellfleet Senior Constellation Professor, with appointments in the Department for Electrical, Computer, and Systems Engineering and the Department for Physics, Applied Physics, and Astronomy. I served as Head of the Future Chips Constellation from 2002 to 2015. Furthermore, I am the founding Director of the Smart Lighting Engineering Research Center, which is funded by the US National Science Foundation at $40 million over 10 years.

16. I am co-inventor of more than 30 U.S. patents and have co-authored more than 300 publications. I authored the books "Doping in III–V Semiconductors" (1993), "Delta Doping of Semiconductors" (1996), and the first and second editions of "Light-Emitting Diodes" (2003 and 2006). My publications have been well recognized by the technical community as illustrated by the more than 25,000 citations that my publications have received. The high number of

citations shows the recognition of my research accomplishments and puts me in the top 1% of researchers in the field of semiconductors.

17. I have received several awards for my technical contributions. They include: Senior Member IEEE (1993); Literature Prize of Verein Deutscher Elektrotechniker for book "Doping in III–V semiconductors" (1994); Fellow SPIE (1999); Alexander von Humboldt Senior Research Award (1999); Fellow IEEE (1999); Fellow OSA (2000); Boston University Provost Innovation Award (2000); Discover Magazine Award for Technological Innovation (2000); R&D 100 Award for RCLED (2001); Fellow APS (2001); RPI Trustees Award for Faculty Achievement (2002 and 2008); Honorary membership in Eta Kappa Nu (2004); 25 Most Innovative Micro- and Nano-Products of the Year Award of R&D Magazine (2007); and the Scientific American 50 Award (2007).

18. My general expertise is in the field of electrical engineering and applied physics with a particular emphasis on semiconductor devices, semiconductor materials, semiconductor processing, and semiconductor device packaging. I have worked in semiconductor processing facilities, including facilities dedicated to silicon integrated circuit (IC) processing, for many years starting in 1980. I have numerous documented contributions to the field of semiconductor doping including the fabrication and analysis of ultra-shallow junctions in silicon, namely delta-function-like doping profiles that are deposited

with near-atomic precision. These doping profiles are more precise than what is currently attainable with ion implantation. At the present time, doping by ion implantation is the dominant doping technique in the silicon IC industry. I have also taught courses on silicon integrated circuit technology. This includes teachings at RPI and Boston University. My teachings concern the theory of silicon integrated circuits as well as the fabrication of silicon integrated circuits, including silicon MOSFETs, LDD MOSFETs, HKMG MOSFETs, LDMOS FETs, FINFETs, and GAAFETs[2]. The courses that I taught include practical hands-on laboratory sections.

19. Furthermore, I have made pioneering contributions to the field of porous silica thin films (porous $SiO_2$ thin films) deposited by oblique-angle deposition. These highly porous silica films, whose porosity can be as high as 90%, are highly desirable for high-speed interconnects in silicon ICs due to the low dielectric constant ("low k") of these materials and the resulting low capacitance of interconnect wires using interlayer dielectrics made of porous silica. My research also included the theoretical study, experimental verification, and the application

[2] LDD = Low-doped drain; HKMG = High k metal gate; LDMOS = Laterally diffused metal oxide semiconductor; FINFET = Fin-shaped FET; GAAFET = Gate all around FET

of the piezo-resistive coefficients of thin silicon membranes that are subjected to a mechanical stress and strain. My research contributions also include the use of delta-doped silicon for MOSFET applications for ultra-shallow junctions. Delta-doped silicon MOSFETs possess ultra-shallow junctions. Indeed, these junctions are the shallowest junctions attainable (delta-doped junctions are shallower than ion-implanted junctions). That is, I (along with my collaborators) demonstrated the shallowest junctions in silicon.

20. At my home institution, Rensselaer Polytechnic Institute (RPI), I teach on the subject of silicon microelectronics on a regular basis. The teaching includes undergraduate and graduate courses. The subject matter includes silicon metal-oxide-semiconductor field effect transistors (MOSFETs), complementary metal-oxide-semiconductor (CMOS) technology, constant-electric-field scaling, the theory of transistors and integrated circuits, and the fabrication of integrated circuits. I am well versed in the theory and the physics of semiconductor devices and associated electrical circuits. In addition, I regularly work with students and staff of a silicon microfabrication clean room facility at my home institution (RPI). Several of my former Ph.D. and Master students have worked or are currently working in the silicon integrated circuit industry including the following companies: IBM Company in Fishkill NY, Global Foundry Company in Malta NY,

Albany Nanotech in Albany NY, Micron Company in Boise Idaho, and Intel Company in Boise Idaho.

21. My experience includes the operation, modeling, driving, design, fabrication, and analysis of solid-state devices and integrated electrical circuits. I am the inventor on patents that concern silicon semiconductor devices, including the doping of silicon. My experience includes the employment and operation of various analysis techniques including SEM (scanning electron microscopy), TEM (transmission electron microscopy), EDXS (energy dispersive x-ray spectroscopy also called EDS or EDX), EELS (electron energy loss spectroscopy), and SIMS (secondary ion mass spectrometry).

22. I have consulted for companies in the semiconductor industry, including the semiconductor processing industry. Specifically, I have consulted for Varian Company in Gloucester, Massachusetts (now part of Applied Materials Company) and for Micron Technologies in Boise, Idaho. In my capacity as a consultant, I visited these companies multiple times and on a regular basis. My consulting has allowed the companies to enhance their understanding of semiconductor devices and take advantage of the technological advancements made in academia including my research laboratory and the microfabrication facility at RPI.

23. More details about my experience and background are included in my curriculum vitae, attached as Appendix A to my report.

**Materials Reviewed**

24. I have reviewed the following documents:

- The '174 patent and its file history
- US patent 6,281,562 and its file history
- US patent 6,709,950 and its file history
- US patent 6,967,409 and its file history
- The TSMC Petition and references cited therein
- Dr. Banerjee's expert declaration and references cited therein
- Various technical articles and patents cited herein and in Patent Owner's Response

**Understanding Of Claim Terms**

25. I understand that in a pending litigation involving the '174 patent (Case No. 2:16-cv-00134-JRG-RSP (E.D. Tex Feb 14, 2016)), the Court has construed certain terms in the claims of the '174 patent. In forming the opinions stated in this report, I have assumed the constructions of those terms as provided by the Court's Order (the "Order"). Dkt. No. 105. Exhibit 3001. In the claim construction order, the following terms of the '174 patent were given the following constructions:

| Claim Term | Construction |
|---|---|
| "a trench isolation region surrounding an active area of a semiconductor substrate" (claim 1) | *Plain meaning* |
| "first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area" (Claim 1) | "first silicide layers formed on regions that are within the active area and located on the sides of the first L-shaped sidewalls" |
| "L-shaped sidewalls" (Claims 1, 14) | "sidewalls that substantially resemble a capital letter 'L' or its mirror image" |
| "surface of the active area" (Claims 9, 10) | "top of the active area" |
| "a lower portion of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area" (Claim 10) | "a bottom surface of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area" |
| "composed of the same material" (Claim 11) | Plain and ordinary meaning |
| "made of the same insulating film" | "made of the same insulating material" |

*See* Exhibit 3001, Appendix A.

**Legal Standards**

26. I am not a lawyer. Counsel for IP Bridge has advised me regarding the

legal principles governing patent law. Based on counsel's advice, my understanding is as follows below.

27. In an IPR proceeding, the Petitioner has the initial burden of persuasion to establish a reasonable likelihood that at least one claim of an issued patent are unpatentable, and this burden remains throughout the entire proceeding

28. Petitioner must provide an analysis of how or why an element from a prior art teaching could be combined with the teaching of another reference

29. A person of ordinary skill in the art (POSITA) at the time the application leading to the '174 patent was filed would have at least a Bachelor's degree in Electrical, Materials, Mechanical, or Chemical Engineering, or a related degree, and at least two years of experience working in semiconductor processing and fabrication, semiconductor equipment manufacturing, or semiconductor materials. Integrated circuit (IC) design is different from IC processing and fabrication. It is one thing to have a theoretical understanding of circuit design, but quite another to be familiar with the problems associated with the IC fabrication process. Without any direction by Petitioner how or why a feature is to be combined, a naked assertion that such would be within the skill of a POSITA is not enough to establish a reasonable likelihood that at least one claim of an issued patent is unpatentable in an IPR proceeding.

30. Although the POSITA is entitled to use "common sense" to arrive at

the conclusion that the claimed invention is obvious, the POSITA must provide a reasoned explanation that avoids conclusory generalizations.

31. An assertion of invalidity cannot be based merely on conclusory statements when dealing with prior art, but must set forth the rationale on which it relies.

32. For an invention to be obvious it is not enough that there be a reason to combine individual elements from different prior art references; the POSITA must also be in possession of sufficient knowledge to know how to incorporate features from one reference into the other reference.

33. Petitioner's expert relies on the following Legal Standard:

> A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle;

Exhibit 1004, ¶37(f).

34. I understand this to not be a generalized starting point in every analysis because it entirely fails to take into account the specific technology, the complexity of the technology, certain constraints associated with the technology, and the specific documents being relied upon and which are being combined.

**Dr. Banerjee's Declaration**

35. I have reviewed Dr. Banerjee's Declaration to see how he addresses the issue if it would be possible to fabricate the combinations of elements that he

proposes would be obvious to combine. I note that he stated the following:

> a. *Ogawa* also discusses how to implement this trench isolation with "a series of ordinary steps available in the prior art" that "are employed for production of sources and drains 58, an inter-layer insulating layer 59 and an upper layer wiring 60 for the ultimate purpose of producing a MOS IC." (*Ogawa* at 8:3–7.)

Exhibit 1004, ¶79.

> b. Moreover, a person of ordinary skill in the art would have understood that replacing *Lee*'s LOCOS with *Noble*'s STI would have been entirely compatible and had no impact on the processes used for gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims. LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing, and how the isolation regions are formed would not affect *Lee*'s processes or the resultant device structures. It is therefore my opinion that the combined teachings of *Lee* and *Noble* render the Challenged Claims obvious. (emphasis applied)

Exhibit 1004, ¶82.

> c. Moreover, a person of ordinary skill in the art would have understood that replacing *Lee*'s LOCOS with *Ogawa*'s trench isolation would have been entirely compatible and had no impact on the processes used for gate formation,

source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims. LOCOS and trench isolation are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing, and how the isolation regions are formed would not affect *Lee*'s processes or the resultant device structures. (emphasis applied)

Exhibit 1004, ¶198.

d. Other references further demonstrate that replacing *Lee*'s LOCOS with *Ogawa*'s trench isolation would have constituted a simple substitution of one known element for another according to known methods to achieve predictable results.

Exhibit 1004, ¶201

e. *Ogawa* also discusses how to implement this trench isolation with "a series of ordinary steps available in the prior art" that "are employed for production of sources and drains 58, an inter-layer insulating layer 59 and an upper layer wiring 60 for the ultimate purpose of producing a MOS IC. (*Ogawa* at 8:3–7.)

Exhibit 1024, ¶78.

f. Moreover, a person of ordinary skill in the art would have understood that replacing *Lowrey*'s LOCOS with *Noble*'s STI would have been entirely compatible and had no impact on the processes used for gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other

> aspect of the claims. LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing,
>
> and how the isolation regions are formed would not affect *Lowrey*'s processes or the resultant device structures. It is therefore my opinion that the combined teachings of *Lowrey* and *Noble* render the Challenged Claims obvious. (emphasis applied)

Exhibit 1024, ¶93.

> g. Other references further demonstrate that replacing *Lowrey*'s LOCOS with *Ogawa*'s trench isolation would have constituted a simple substitution of one known element for another according to known methods to achieve predictable results.

Exhibit 1024, ¶166.

> h. A person of ordinary skill in the art would have understood that replacing *Lowrey*'s LOCOS with *Ogawa*'s STI would have been entirely compatible and had no impact on the processes used for gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims. LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing, and

> how the isolation regions are formed would not affect *Lowrey*'s processes or the resultant device structures. (emphasis applied)

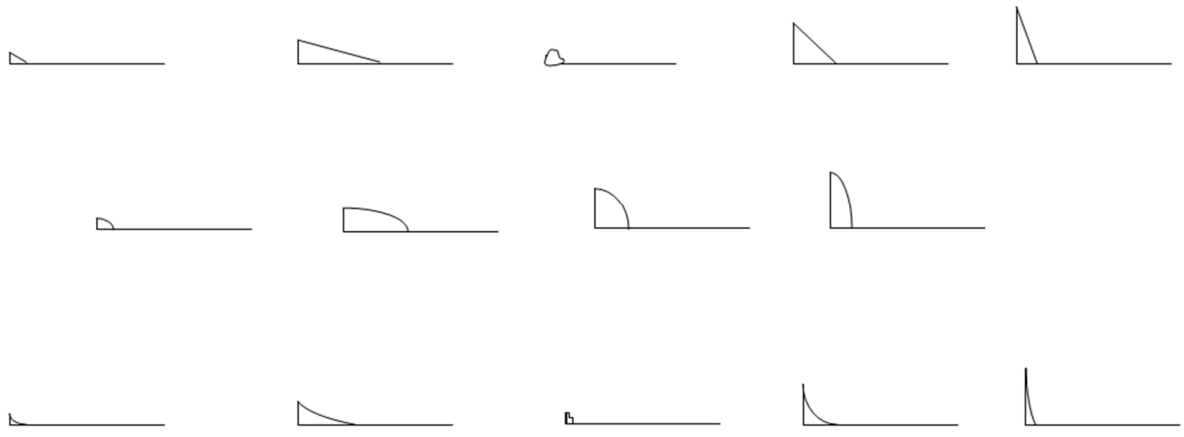
Exhibit 1024, ¶173.

36. I find these statements to be entirely superficial and conclusory. They do not begin to address the numerous considerations and obstacles associated with changing the configuration and processing sequence of an IC. Depending upon the configuration changes required when elements from one reference are substituted into another, such a substitution may well not be within the skill of the POSITA.

37. By way of example, I strongly disagree that "how the isolation regions are formed would not affect *Lowrey*'s processes or the resultant device structures" and that *Noble*'s STI would have had no impact on the processes used in gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims. Petitioner has not stated which steps of the references would be combined with one another or how this would be done, but based on the strong recognition in the literature to the effect that "Generally, a change in one phase of the fabrication process usually impacts other phases" (Exhibit 2015, 2:52-53; Exhibit 2016, 2:19-21), Dr. Banerjee is clearly in error when he dismisses the Si IC fabrication process, including the modification of the Si IC fabrication process by substitution of LOCOS isolation with trench isolation as "simple." Such characterization is contradicted by numerous reference articles (see ¶61 herein) and by the fact that hundreds of engineers work for years to

develop process modification in the field of Si ICs.

38. By way of example only, when the various references upon which Dr. Banerjee relies have their features combined in a fabrication process that he does not describe, if indeed they can be combined, there is no way of knowing what shape of sidewalls will emerge when relative dimensions are changed and different fabrication processes are used. Depending upon the relative dimensions of the structure on which the sidewalls are formed, the process by which they are formed, the substances of which they are formed, a wide variety of shapes of sidewalls may result. There is no way of knowing which shape actually results from the combinations that Dr. Banerjee is proposing as will be discussed herein. Examples of possible shapes are shown here:



39. Petitioner had no basis for assuming that the sidewalls of the interconnect of *Lee* would remain unchanged when trench isolation is substituted

for LOCOS isolation. This is because upon substitution, the gate conductor stops at the edge of the trench isolation.

**Technological Background**

Acronyms

40. For convenience, I list some acronyms that are commonly used in the field of Si IC technology:

| | | |
|---|---|---|
| BEOL | = | Back end of line (interconnect metallization fabrication) |
| CMOS | = | Complementary MOS |
| CMP | = | Chemical mechanical planarization (or polishing) |
| CVD | = | Chemical vapor deposition |
| FEOL | = | Front end of line (transistor and local interconnect fabrication) |
| FET | = | Field-effect transistor |
| IC | = | Integrated circuit |
| LOCOS | = | Local oxidation of silicon |
| MOS | = | Metal oxide semiconductor |
| PVD | = | Physical vapor deposition |
| S, D, G | = | Source, Drain, Gate (respectively) |
| STI | = | Shallow trench isolation |
| TSMC | = | Taiwan Semiconductor Manufacturing Company (Petitioner) |

Silicon Integrated Circuit (IC) Processing

41. Si integrated circuits (ICs) are highly complex electrical systems on a small microstructured chip. An integrated circuit can have millions of transistors that serve to process, store, and transport information. ICs consist of different units, e.g. a data processing unit for processing information, a memory unit for storing information, and an input / output unit for receiving and sending information.

42. The core element of an integrated circuit is a transistor, specifically the field-effect transistor (FET) that uses an electric field ("field effect") in order to induce charge carriers in the transistor's channel region. The channel region connects the transistor's source (S) with the transistor's drain (D). The source and drain are separated by the gate (G) that controls the flow of charge in the channel between the source and drain.

43. The transistor's gate has a typical three-layer stack consisting of a **m**etal or metal-like material (M), an insulator or **o**xide (O), and a **s**emiconductor (S), thereby forming the MOS layer stack. The top two layers (gate conductor "M" and gate insulating film "O") are called the gate layer stack, or simply gate stack. Accordingly, transistors based on the MOS layer stack are called MOSFETs.

44. There are two types of transistors, those using **n**egative electrons in the channel (n-channel FET) and those using **p**ositive holes in the channel (p-

channel FET). The two types of transistors have complementary properties. For example, a *positive* gate voltage induces an *electron* channel in an n-channel FET whereas a *negative* gate voltage induces a *hole* channel in a p-channel FET. If a single voltage is applied simultaneously to the two gates of the two types of transistors, one of them will conduct electricity (ON state) whereas the other one will not conduct electricity (OFF state). Due to the complementary nature of the two types of transistors, the technology is referred to as **c**omplementary MOS technology or simply CMOS technology. At the present time, the vast majority of ICs are based on CMOS technology.

45. The circuit layout is the result of (i) the circuit functionality designed by design engineers and (ii) how the designed circuit is implemented by a processing sequence devised by process engineers.

46. The processing sequence is carried out in a fabrication facility, also abbreviated as "fab" or "IC fab". Such fabrication facilities are highly advanced facilities that are highly automated so that the handling of Si wafers by humans is minimal. Regarding the processing sequence, we distinguish between a first group of fabrication processes called **f**ront **e**nd **o**f **l**ine (FEOL) processes and a second group of fabrication processes called **b**ack **e**nd **o**f **l**ine (BEOL) processes. The FEOL processes include the fabrication of the actual transistors (MOSFETs) including the silicidation of source, gate, and drain. The BEOL processes include

the fabrication of metal-based interconnect lines and associated dielectric layers (interlayer dielectrics) that electrically insulate the metal interconnects from each other.

47. Hallmarks of IC processing include (i) high spatial precision by means of lithography (to attain very small patterns with nanometer feature sizes) and (ii) cleanliness (to avoid contaminations).

48. The processing of wafers proceeds in a strict sequence of processing steps that are carefully chosen in sequence and content. For example, the gate stack of a transistor requires the availability of a Si substrate. A first step, the deposition or growth of the gate dielectric (commonly an oxide), is followed by a second step, the deposition of the gate electrode (or gate conductor). The processing of Si wafers proceeds in a strict sequence of processing steps (or processing modules) that are carefully chosen in sequence and content.

49. Furthermore, certain elements of an IC require the pre-existence of other elements and rely on their presence for the proper functioning of the ensemble of elements. For example, the source / drain dopant implant commonly requires the presence of the gate electrode so that the gate can mask the channel region from the implantation ion beam. That is, the gate enables the proper definition of the source / drain implanted regions. An implantation process in which the source / drain regions are automatically aligned with the gate electrode is

referred to as a "self-aligned implantation process". Exhibit 2013, p. 5; Exhibit 2014, p.4; Exhibit 2015, 2:52-61; Exhibit 2016, 2:19-24; Exhibit 2017, 6:23-31; Exhibit 2018, 1:18-29; Exhibit 2019, 2:9-19.

50. It is generally not possible to reverse the sequence of processing steps. A series of individual processing steps constitutes a "processing module". For example, the formation of shallow trench isolation is such a processing module with (i) trench etching, (ii) trench refill with silicon dioxide and (iii) planarization being the major steps of the module.

51. In addition to the major steps of trench formation, there are minor steps not listed above. A more complete series of steps employed for trench formation may include: pad or gate oxide deposition; pad or gate polysilicon deposition[3]; resist coating; photo-lithography; polysilicon etching; oxide etching; ***trench etching*** by means of a dry etch; resist strip; liner-oxide growth; ***trench refill*** with CVD silicon dioxide; annealing to improve quality of oxide; ***planarization*** by CMP (chemical mechanical planarization); various cleaning steps, rinsing steps, and metrology steps are used throughout the module (major steps emphasized).

52. Each processing step (or processing module) is intended and works

[3] *Noble* and *Ogawa* use such pad / gate oxide deposition followed by pad /gate poly-silicon deposition sequence.

for a specific *initial* configuration of the Si wafer. Upon completion of the processing step (or processing module), the Si wafer has a new, *final* configuration.

53. That is, each processing step (within a processing module) ***transforms*** the Si wafer from an ***initial configuration*** to a ***final configuration*** associated with this processing step.

54. Likewise, each processing module (with each processing module consisting of a sequence of processing steps) ***transforms*** the Si wafer from an ***initial configuration*** to a ***final configuration*** associated with this processing module.

55. When taking a specific processing step (within one processing module) out of its intended sequence and inserting it at another point in the sequence of processing steps, one must ensure the following: ***First***, the sequence of processing steps preceding the specific processing step must provide an initial configuration compatible with the specific processing step. ***Second***, the final configuration resulting from the specific processing step must be compatible with the subsequent processing step and beyond.

56. In other words, the initial and final configuration of a wafer associated with a specific processing step must be compatible with the entire fabrication process. As would be understood by a POSITA, a random change in the sequence in processing steps would not lead to the desired result; if done nonetheless, it will

likely lead to a non-functioning IC device. Changing the sequence of processing steps requires that the fabrication process be re-engineered, e.g. the entire front-end-of-line (FEOL) fabrication process may need to be re-engineered. This elucidates that the fabrication of an IC device is based on a specific sequence of processing steps that cannot be changed at random.

57. The same tenet discussed above for processing *steps* also applies to processing *modules*: When taking a specific processing module out of its intended sequence and inserting it at another point in the sequence of processing modules, one must ensure the following: ***First***, the processing modules preceding the specific processing module must provide an initial configuration that is compatible with the specific processing module. ***Second***, the final configuration resulting from the specific processing module must be compatible with the subsequent processing module and beyond.

58. As would be understood by a POSITA, a random change in the sequence of processing modules would not lead to the desired result; if done nonetheless, it will likely lead to a non-functioning IC device.

59. For example, trench isolation formation consists of three major processing steps, namely (i) etching the trench, (ii) refilling the trench with CVD oxide, and (iii) planarizing the wafer. Without elaborating further, it would be understood by a POSITA that it would not be possible to change the sequence of

these three processing steps.

60. Planarizing the wafer involves a process that makes the wafer surface planar or flat. The planarization can be accomplished by, for example, a technique called chemical mechanical planarization (CMP). This process uses a chemically enhanced mechanical polishing procedure to planarize or polish a wafer.

61. By 1995, the complexity of integrated circuit fabrication was appreciated by the technical community and widely supported by the technical literature. Quotes illustrating the complexity of fabrication include the following:

> The structure of an ***integrated circuit is complex*** both in the topography of its surface and in its internal composition. Each element of such a device has an ***intricate three-dimensional architecture*** that must be reproduced exactly in every circuit. The structure is made up of many layers, each of which is a detailed pattern. Some of the layers lie within the silicon wafer and others are stacked on the top. The manufacturing process consists in forming this sequence of layers precisely in accordance with the plan of the circuit designer. (Emphasis added)

Thompson, 1983, Exhibit 2013, p.5.

> This photolithography process is repeated (to more than 10 times) before the ***three-dimensional circuit geometries*** necessary for a completed metal oxide semiconductor (MOS) or bipolar device are achieved. The ***structure of an integrated***

> ***circuit is complex***, both in the topography of its surface and in its internal composition. Each element of this device has an intricate three-dimensional structure that must be reproduced exactly in every circuit. The structure is made up of many layers, each of which is a detailed pattern. Some of the layers lie within the silicon wafer and others are stacked on the top. (Emphasis added)

Roland, 1990, Exhibit 2014, p.4.

> Generally, ***a change in one phase of the integrated fabrication process usually impacts other phases***. Since integrated circuit fabrication processes are ***highly complex*** and require sophisticated equipment, developments of entirely new processes and materials can be quite costly. Thus, new apparatus and methods for control of the CMP process that can be incorporated into current fabrication technology would be highly desirable because expensive modification of equipment and processes can be avoided. (Emphasis added)

Yu, 1994 (U.S. Patent No. 5,314,843), Exhibit 2015, 2:52-61.

> ***Generally, a change in one phase of the fabrication process usually impacts other phases***. Since semiconductor device fabrication processes are highly complex and require sophisticated equipment, developments of entirely new processes and materials can be quite costly. (Emphasis added)

Meikle, 1993 (U.S. Patent No. 5,231,306), Exhibit 2016, 2:19-24.

> The result of these ***highly complex imaging, deposition and growth, and etching-masking processes*** is the transformation of each substrate into a large number of integrated circuits which may contain literally tens or hundreds of thousands of individual circuit elements. Once these processes are completed, each wafer is scribed and diced so as to separate it into individual integrated circuits or chips, to which wire leads are then bonded prior to final encapsulation and packaging. (Emphasis added)

Ballard, 1985 (U.S. Patent No. 4,529,621), Exhibit 2017, 6:23-31.

> Within the semiconductor industry, production of ***electronic circuits by very large scale integration ("VLSI") techniques is constrained*** by a variety of factors which limit yield and ***inhibit process flexibility***. These detrimental factors include, for example, the exposure of wafers to contaminants and/or oxidation during fabrication. Such processing constraints adversely affect mass production of integrated circuits. In addition, conventional processes are slow and inordinately expensive for the fabrication of low-volume products, thus posing an impediment to new device and circuit designs. (Emphasis added)

Ehrlich, 1994 (U.S. Patent No. 5,310,624), Exhibit 2018, 1:18-29.

> Depending on the fabrication technologies and techniques, and

> the materials used, ***different configuration constraints apply***. These constraints are commonly referred to as ***"geometric design rules" or "design rules."*** Design rules include, for example, specifications for minimum spacing between transistors and minimum separation between conductors to prevent shorting, specifications for minimum metal width, and specifications for maximum metal heights and slopes of walls which form metal junctions.

Corbin, II, 1992 (U.S. Patent No. 5,097,422), Exhibit 2019, p. 2:9-19.

62. The above citations directly rebut Dr. Banerjee's out of hand, dismissive, and conclusory statements regarding how the processes of the various references are to be integrated with one another. See ¶35 above.

Electrical Isolation In Silicon Integrated Circuit Wafers

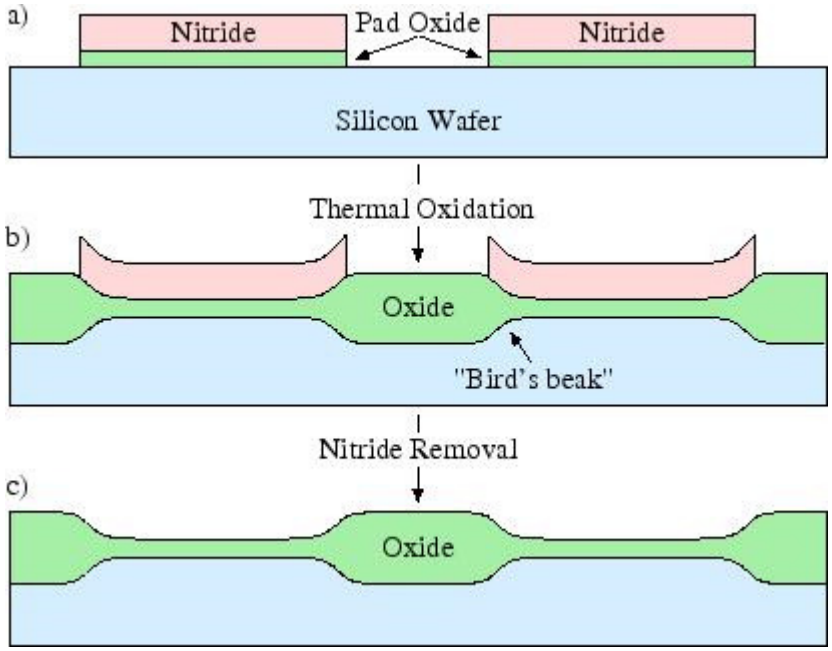
63. In a silicon (Si) integrated circuit (IC), it is necessary that different circuit elements are electrically isolated from each other. An example of a circuit element is a transistor, specifically a field-effect transistor (FET). A lack of electrical isolation would lead to undesired or parasitic electrical currents between different transistors of the IC. Such parasitic currents would negatively affect the proper functioning of the IC. Electrical isolation features have been used since the first generation of ICs back to the 1960s. The electrical isolation proceeded through several generations:

64. ***Mesa and pn junction isolation***: Early generations of semiconductor

devices used "mesa structures" (reminiscent of mesa-shaped mountains) and pn-junction structures for the electrical isolation. That is, different circuit elements on a wafer were electrically isolated from each other (i) by being located on different mesas or (ii) by being separated from each other by an electrically blocking pn junction.

65. ***LOCOS isolation***: In the 1970s, 1980s, and early 1990s, a widely-employed structure for the electrical isolation of circuit elements was LOCOS isolation. LOCOS means "**loc**al **o**xidation of **s**ilicon". The LOCOS process forms a thermal oxide of Si, i.e. $SiO_2$, which is a dielectric and thus electrically insulating. The formation of the oxide proceeds through a chemical reaction where the Si of the substrate chemically reacts with oxygen ($O_2$) to form $SiO_2$. The LOCOS oxide is also called the "field oxide" because it defines the active field where the transistors are located. The "field oxide" is distinguished from the "gate oxide". At the end of the 1990s, LOCOS isolation started to be no longer used in then-state-of-the art Si IC devices. The images below show the process sequence of LOCOS isolation as of 1995:[4]

[4] The images are found at: http://www.iue.tuwien.ac.at/phd/hollauer/node7.html

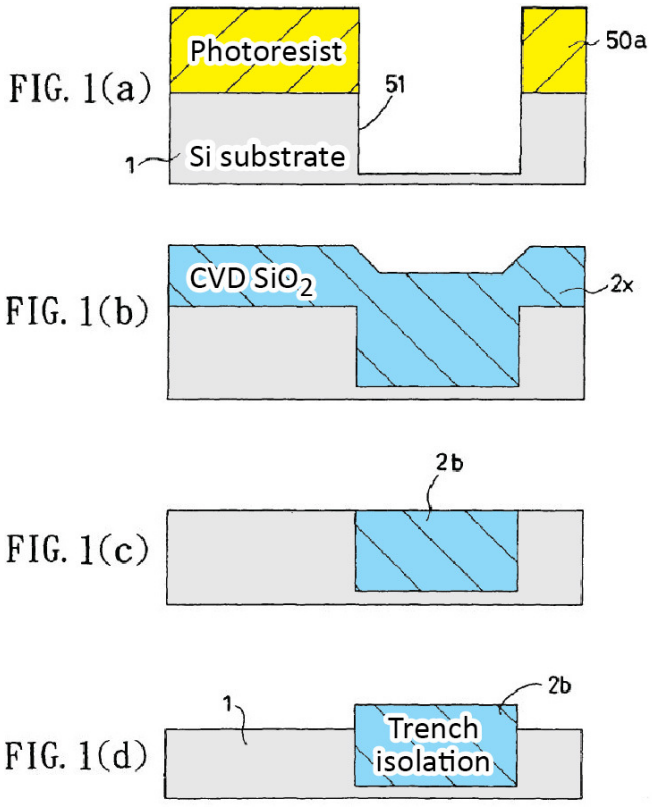



66. ***Trench isolation***: A more recent generation of electrical isolation is a trench isolation which is formed by etching a trench, then refilling the trench with a dielectric material (such as $SiO_2$), followed by planarization of the wafer. During planarization, the wafer surface is flattened so that the next processing step is performed on a planar wafer surface. The planarization can be accomplished by, for example, chemical mechanical planarization (CMP)[5].

67. The process steps of forming a raised trench isolation disclosed in the '174 patent and illustrated in Figure 1 (shown below) include the (i) etching of a trench ("The silicon substrate ***1*** is dry-etched by using the resist film ***50a*** as a

[5] CMP is an acronym for both "chemical mechanical *planarization*" and "chemical mechanical *polishing*".

mask, thereby forming a trench ***51*** with a depth of 1 μm." Exhibit 1001, 12:35-37), (ii) refilling of the trench with deposited $SiO_2$, e.g. CVD-deposited $SiO_2$ ("the resist film ***50a*** is removed, and then a silicon oxide film ***2x*** is deposited on the entire top surface of the silicon substrate ***1***." Exhibit 1001, 12:38-40), and (iii) planarization ("the silicon oxide film ***2x*** on the silicon substrate ***1*** is removed by, for example, a CMP (chemical mechanical polishing) method." Exhibit 1001, 12:43-45).




68. CMP is a process that includes a polishing pad that is soaked with a chemical solution. The semiconductor wafer is slightly pressed onto the polishing

pad. The semiconductor wafer and polishing pad are subjected to rotating motions to ensure uniformity of the CMP process. CMP includes a chemical-etching component and a mechanical-polishing component both of which contribute to the planarization (or flattening) of the wafer surface. Two schematics of the CMP process[6] and a photograph of a CMP tool[7] are shown below. The schematics and photograph show a Si wafer subjected to CMP:

[6] The first schematic illustration of the CMP process is from Kaufman et al. from 1992. Exhibit 2032. The second schematic illustration of the CMP process is from Landis et al. from 1992. Exhibit 2033.

[7] The photograph shows a CMP tool (Chemical Mechanical Polishing tool) of the Applied Materials Company (http://www.businesswire.com/news/home/20040711005007/en/AppliedMaterials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion). Although this photograph is from after 1995, the basic concept is consistent with a CMP tool from the 1995 timeframe. Exhibit 2004.

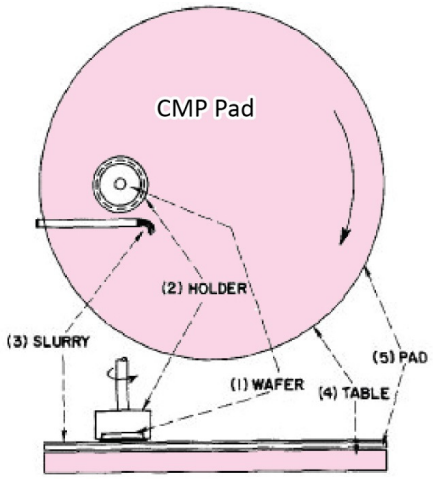



Fig. 3. Schematic of chemical mechanical-polishing technique, top and side views. For clarity, overarm mechanism connected to wafer holder has been omitted. Wafer (1) is held in holder (2) using commercially available template; slurry (3) flows between wafer surface and pad (5) covered table (4). See text for further details.

From *Kaufman et al.* Exhibit 2032.

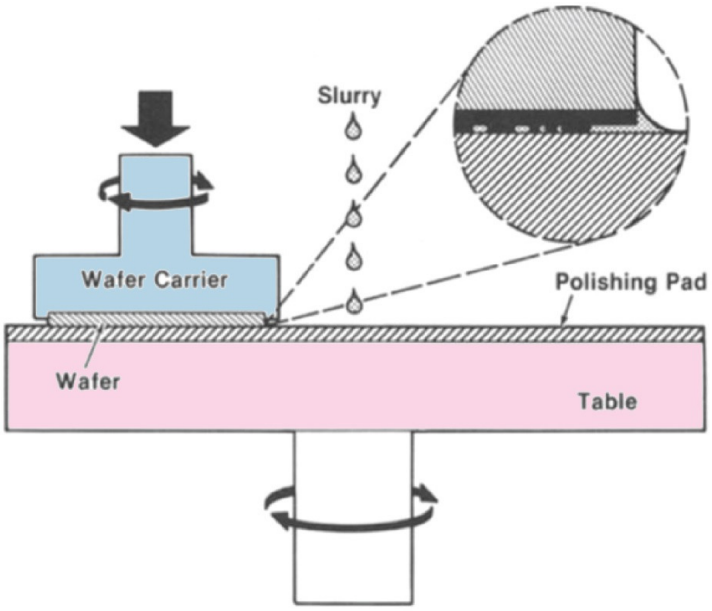
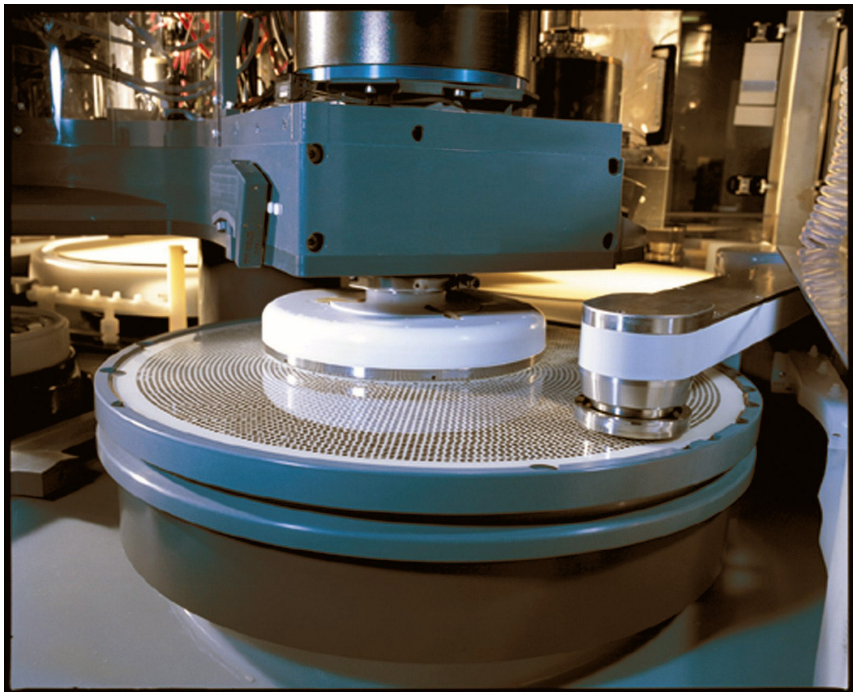



Fig. 2. Schematic diagram of a chemical–mechanical polish tool.

From *Landis et al.* Exhibit 2033



From Exhibit 2004

Differences Between LOCOS Isolation And Trench Isolation

69. The two processes, LOCOS isolation and trench isolation, are fundamentally different. The first one, LOCOS, is based on a chemical reaction in which the silicon of the substrate wafer chemically reacts with oxygen according to the chemical reaction $Si + O_2 \rightarrow SiO_2$. It lies in the very nature of chemical reactions that they are primarily controlled by the laws of chemistry and only secondarily by process engineering. As a result, the oxidation of Si occurs in areas that are undesirable, specifically, the oxide growth proceeds under a silicon nitride mask that is intended to prevent the oxidation in the first place. The resulting feature is referred to as a "bird's beak" where the tip of the beak is the point that

has intruded deepest under the silicon nitride mask. Due to the chemical nature of LOCOS and the resulting "bird's beak", the LOCOS isolation feature grows to have a greater spatial extent than is desirable.

70. On the other hand, the trench isolation process starts by etching a trench into the semiconductor substrate. If the trench depth is about 1.0 μm or shallower, the trench isolation can be referred to as a shallow trench isolation (or STI). Subsequent to etching the trench, it is refilled with $SiO_2$ (silicon dioxide) typically deposited by chemical vapor deposition (CVD). Subsequently, the wafer is planarized by a suitable planarization technique such as CMP. The planarization step is mandated due to the modulated surface topology created by the refilling of the trench (the CVD $SiO_2$ indeed coats the entire Si wafer). The planarization creates a planar or flat surface topology that is advantageous for subsequent processing steps.

71. I summarize the differences between LOCOS isolation and trench isolation as follows: **(1)** LOCOS is based on a chemical oxidation of the Si substrate. Trench isolation does not involve such chemical reaction. **(2)** Trench isolation requires a planarization step whereas LOCOS isolation does not. **(3)** The need for planarization (i.e. a flat surface) in conjunction with trench isolation may not be compatible with certain processing steps in conventional fabrication processes particularly if the conventional fabrication processes have produced a

non-planar surface topology before forming a trench isolation. **(4)** The feature size of the trench isolation is generally smaller than the feature size of the LOCOS isolation (field oxide). **(5)** The $Si / SiO_2$ interface of trench isolation is more prone to contamination than the $Si / SiO_2$ interface in LOCOS. This is because the unfilled (empty) trench (once "dug" out) is subject to unavoidable surface contamination. The fact that the interface in LOCOS is formed by chemical reaction involving the Si substrate makes it one of the cleanest interfaces attainable. As a consequence, the magnitude of the leakage current and the associated transport mechanism is different for LOCOS isolation and trench isolation.

LOCOS Isolation And Trench Isolation Are Not Functionally Equivalent

72. Dr. Banerjee characterizes LOCOS isolation and shallow trench isolation (STI) as "functionally equivalent":

> Trench isolation techniques, such as shallow trench isolation (STI), replaced LOCOS to avoid the scaling problem of the latter. In STI, selected areas of a substrate are etched to form trenches, which are filled with insulating material. Although marginally more expensive and complex than LOCOS, STI does not encroach laterally into neighboring regions, thus resolving the problems of LOCOS. Because the two processes are so similar otherwise, STI and LOCOS are interchangeable

and functionally equivalent.

(Exhibit 1004 and 1024, ¶52-53; internal citations omitted).

73. I disagree with Dr. Banerjee in this regard. My detailed discussion of LOCOS and trench isolation (see above) make it abundantly clear that the two processes are fundamentally different and cannot be simply swapped out of one process into another without considering the multitude of consequences that will result from such swap.

74. As an example, we consider a wafer having a non-planar surface topology, i.e. a wafer that, much like a landscape, has a modulated surface topology that varies in height, i.e. has "hills" and "valleys". Assume that such non-planar wafer is being prepared for the formation of a trench isolation. Given that the wafer's initial configuration includes a non-planar surface topology and given that the trench isolation formation concludes with a planarization step, e.g. by CMP, creates the following dilemma: Since the entire wafer is subject to planarization, a wafer-wide planar surface topology will be created, so that (i) some of the above-mentioned "hills" may be chopped off and / or (ii) some of the above-mentioned "valleys" may remain filled with oxide. Neither one of these

scenarios is acceptable.[8] This is because a semiconductor wafer that is being processed consists of a multitude of films that can be as thick as several 100 nm (for example interconnect-layer dielectrics) and as thin as one or a few nm (for example the gate dielectric). If planarization is performed on a wafer exhibiting a non-planar surface topology, one or more of these layers may be physically interrupted thereby creating an open circuit and potentially rendering the IC non-functional.

75. That is, as a primary consequence, "hilltops" of the modulated surface may be chopped off and/or "valleys" may remain filled with insulating material. As secondary consequences, vital elements of the wafer may be removed and/or vital elements that should be exposed become undesirably buried. In 1995, a POSITA using the CMP process would not have had the means of addressing the problems arising from the non-planar topology.

76. In his declaration, Dr. Banerjee does not address at all the planarization process that is associated with trench isolation formation. Furthermore, Dr. Banerjee gives no consideration to the interference of the

[8] One can consider a third intermediate scenario in which hilltops are partially chopped off and valleys remain partially filled. This scenario would be unacceptable as well.

planarization process with a wafer's non-planar surface topology. Dr. Banerjee's consideration in this regard is insufficient because the effect of planarization on a non-planar surface topology will render the IC non-functional. Indeed, the employment of trench isolation on a wafer having non-planar surface topology would generally result in a non-functioning IC device unless the fabrication process is completely re-engineered. Dr. Banerjee never says how this could be done while still achieving the final structure recited in the challenged claims of the '174 patent. The purpose of the CMP process is to ***planarize*** the wafer surface. To suggest otherwise would be contrary to the basic purpose and teachings associated with the CMP tool. This is particularly true in 1995 when CMP tools were not as advanced as they are at the present time (2017).

77. As I have pointed out, the technical literature has detailed the complexity of Si IC fabrication numerous times. Quotes from the technical literature elucidate the small tolerances, highly constrained processes, and highly complex processes common in the art of Si ICs: "The structure of an integrated circuit is complex […] intricate three-dimensional architecture […] three-dimensional circuit geometries […] structure of an integrated circuit is complex […] a change in one phase of the integrated fabrication process usually impacts other phases […] integrated circuit fabrication processes are highly complex […] Generally, a change in one phase of the fabrication process usually impacts other

phases […] highly complex imaging, deposition and growth, and etching-masking processes […] electronic circuits by very large scale integration ("VLSI") techniques is constrained … which … inhibit process flexibility […] different configuration constraints apply" (Exhibits 2013-2019). Accordingly, details, such as the non-planar topology of a Si IC, are highly relevant and cannot be ignored.

78. If CMP is performed on a wafer surface having a non-planar topology, a multitude of problems are created: They include unintended electrical short circuits (undesired electrical connections) and unintended electrical open circuits (undesired electrical disconnects).

79. In 1995, CMP was in fact not used on a wafer having non-planar surface topology (such as *Lowrey*). Indeed, the suggestion that CMP in 1995 could have been used for non-planar surface topologies is contrary to the very nature and purpose of CMP.

80. I find it difficult to understand that Dr. Banerjee, when describing the trench isolation process, neither discloses nor discusses the planarization process that is part of trench isolation fabrication. The planarization will necessarily interfere with a modulated or non-planar topology of a partially processed Si wafer surface.

81. Petitioner's invalidity arguments assume that a POSITA could easily replace the conventional LOCOS isolation of *Lee* and *Lowrey* with the non-

conventional trench isolation of *Noble* and *Ogawa*. Petitioner's assumption is misguided. A POSITA would understand that the establishment of a new process involving trench isolation would, in the best case, require a significant re-engineering of the fabrication process, and, in the worst case, not be possible because the combination would result in a non-functional device.

82. I agree with Dr. Banerjee that LOCOS isolation and trench isolation serve the purpose of electrically isolating different active areas of an IC. However, I disagree with Dr. Banerjee that LOCOS and STI are "functionally equivalent". "Functionally equivalent" implies that they would function in an equivalent manner. However, there are fundamental differences in the way these features function and are fabricated as discussed above.

83. Because of the above-discussed fundamental differences, ***different components and configurations are necessary*** at the initial stage, during the process, and at the final stage of LOCOS and trench isolation. Accordingly, I am unable to agree that LOCOS and trench isolation would be "functionally equivalent".

Difficulties Of Employing STI On Wafers Having A Non-Planar Topology

84. Performing the trench isolation process on a wafer having a non-planar surface topology (i.e. a surface topology that varies in height and thus has "hills" and "valleys") is difficult or impossible for the reasons explained below.

85. Consider LOCOS isolation being performed on such modulated surface topology. This can be done since the LOCOS structure will add a local isolation feature to the wafer (the local isolation feature includes the LOCOS field oxide plus the two bird's beak regions).

86. Next consider the shallow trench isolation (STI) process being performed on such modulated surface topology keeping in mind that the STI process concludes with a required planarization step. When deposited, the material filling the trench (commonly $SiO_2$) will follow the "hilltops" and "valleys" of the wafer's modulated surface topology. Upon planarization, a key question is: How far should the planarization proceed? If the planarization stops relatively early, the "valleys" will remain filled with $SiO_2$; this is an unwanted effect.

87. On the other hand, if the planarization stops relatively late, the "hilltops" will be cut off; this is an unwanted effect as well.[9] In other words, every possible level at which the planarization is terminated would result in an unwanted effect (either filling in the valleys or cutting off the hilltops or both). That is, any planarization level chosen would damage at least some part of the pre-existing modulated surface topology. This makes it difficult or impossible to use trench

[9] Planarizing the wafer to an intermediate level would leave unwanted material in "valleys" and cut off wanted materials at "hilltops".

isolation, particularly its planarization, on a preprocessed wafer that exhibits a modulated surface topology (and a POSITA in 1995 would not have proceeded this way).

88. *Lowrey* is an example of a modulated surface topology. Indeed, *Lowrey* has several processing steps that precede the LOCOS process. Dr. Banerjee does not explain in his Declaration how or when the required planarization would be performed if a trench isolation were to be substituted for LOCOS isolation.

89. *Lowrey* describes a process sequence by means of several figures that illustrate the process flow. *Lowrey*'s Figures 1-4 illustrate the modulated features resulting from processes that precede LOCOS. *Lowrey*'s Figure 5 illustrates the LOCOS field oxide feature.

90. In summary, if one were to substitute trench isolation for LOCOS isolation, one would face the above-detailed dilemma of how to choose a planarization level that would not damage some part of the pre-existing modulated surface topology. Accordingly, it is difficult or impossible to form trench isolation features at a later stage of the processing, particularly at a stage when the wafer has a non-planar modulated surface topology (and a POSITA in 1995 would not have proceeded this way).

91. The Petition fails to address the fact that when combining references relating to semiconductor devices, the process ("process sequence") by which the integrated circuit (IC) devices are formed is inseparable from their final structure as claimed. As such, simply substituting a component from one device, *e.g.,* STI, for a different component in another device, *e.g.,* LOCOS isolation, can provide unworkable results, both in terms of how the substituted component cooperates with other components, and how the changed manufacturing sequence, which is required to effectuate such substitution, can be implemented. This is particularly true for Si ICs where a single film can serve multiple purposes, and where a multitude of different functional features are condensed into a minimum number of layers and processing steps.

92. Petitioner's obviousness arguments simply take out the LOCOS isolation (*Lee and Lowrey*) for the STI (*Noble* and *Ogawa*) without describing how such a substitution could be accomplished and without giving due consideration to the strong interconnectedness and interdependency of the Si IC fabrication process. A LOCOS isolation is formed using a very different process sequence than the process sequence used to form a STI. To produce an operative device, their very different respective fabrication processes must be merged, integrated, and made

compatible with their respective gate stack and interconnect stack fabrication processes. If this is not possible, a merged structure will not be possible.[10]

93. Petitioner never once addresses how and when *Noble's* and *Ogawa's* STI can be substituted in for *Lee or Lowrey's* LOCOS isolation. Indeed, it would have been apparent to a POSITA at the time of invention that the incompatible process sequences for forming the STI disclosed in *Noble* or *Ogawa* would not have been substitutable for the LOCOS isolation of *Lee or Lowrey*, and as such, there would have been no motivation for the POSITA to substitute the LOCOS isolation of *Lee or Lowrey* with the STI of *Noble* or *Ogawa*.

94. It is recognized that both LOCOS isolation and trench isolation serve the purpose of electrically insulating transistors of a Si IC device. However, LOCOS isolation and trench isolation are created by fundamentally different fabrication processes. LOCOS isolation is based on the oxidation of the Si wafer

[10] I understand that it would have been the burden of Petitioner to show that a fabrication process that follows from the various combinations of *Lee*, *Lowrey*, *Noble* and *Ogawa* would have obviated the '174 patent. To meet its burden, Petitioner could have provided a pictorial or narrative process flow of the combined prior art references. However, I was not provided with such pictorial or narrative process flow.

by means of a high-temperature chemical reaction (LOCOS means Local ***Oxidation*** of Si). The oxidation process proceeds according to the laws of chemistry and thus creates the undesired yet unavoidable bird's beak. In contrast, trench isolation does not involve such problematic oxidation of the Si wafer by means of a chemical reaction and therefore does not create the undesired bird's beak. Any discussion on the substitution of LOCOS isolation with trench isolation must take into account these differences.

95. *Noble* and *Ogawa* are aware of these differences and for this reason employ trench isolation by using a process sequence that starts with the deposition of the gate stack (gate insulating film plus the gate conductor) followed by trench etching, trench refilling with an oxide, and CMP. This is contrary to *Lee* and *Lowrey* who are able to deposit the gate stack on the (LOCOS) isolation. *Noble* and *Ogawa*, cannot deposit the gate stack on the (trench) isolation. Accordingly, **although some documents say that LOCOS isolation and trench isolation can substitute for each other, that entirely misses the point because** review of the detailed process sequence elucidates that the two processes, as practiced by each of the combinations (*Lee* with *Noble*, *Lee* with *Ogawa*, *Lowrey* with *Noble*, and *Lowrey* with *Ogawa*), are incompatible.

96. Furthermore, the inventors of *Lee* and *Lowrey* were aware of trench isolation (to be discussed later). Despite their awareness, they did not suggest that

LOCOS isolation could be substituted by trench isolation. This suggests that *Lee* and *Lowrey* understood that the underpinning process design must be taken into account and that the replacement of LOCOS isolation by trench isolation is not a matter of simple substitution. Exhibit 2021, 1:8-9; Exhibit 2031, 2:23-28.

**The Invention Of Claim 1 Of The '174 Patent**

97. The '174 patent (Exhibit 1001) is directed to a semiconductor device comprising a trench isolation surrounding an active area of a semiconductor substrate. A gate insulating film is formed over the active area, and a gate electrode is formed over the gate insulating film. First L-shaped sidewalls are formed over the side surfaces of the gate electrode with first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area, and with an interconnection formed on the trench isolation. Second L-shaped sidewalls are formed over the side surfaces of the interconnection.

98. The '174 invention is directed to a semiconductor device which includes a number of claimed elements as part of a device. Thus, when combining prior art references in order to reproduce the '174 patent, it is insufficient to simply pluck out specific components from various prior-art devices and then re-assemble these components to re-construct the device claimed in the '174 patent. Not only the components themselves but also the fabrication process of how they are configured in a device must be considered. How the components are positioned

and connected in a device depends on how the device and its components have been fabricated.

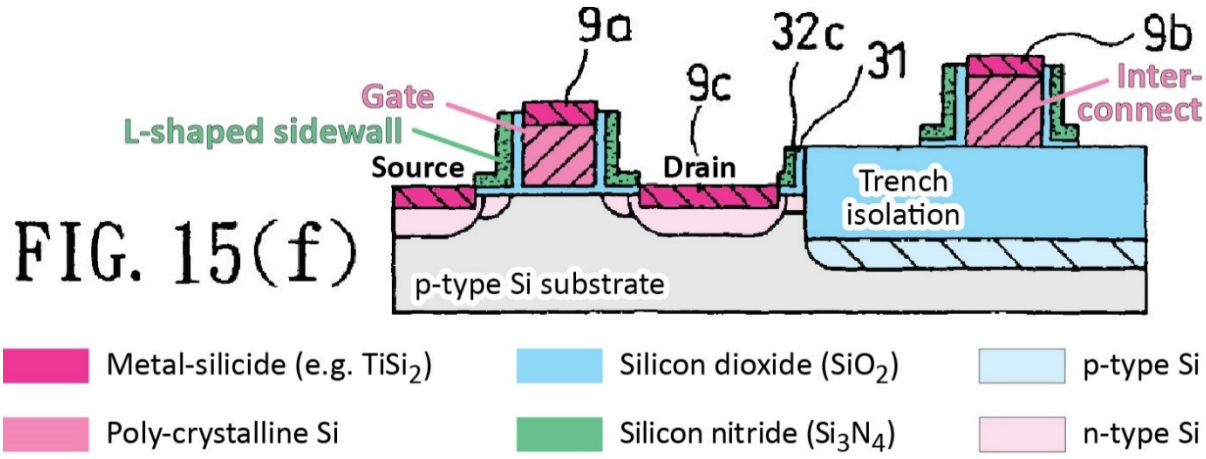



FIG. 15(f)

99. Fig. 15(f) of the '174 patent above illustrates a semiconductor device comprising a trench isolation (blue) surrounding an active area of a semiconductor substrate; a gate insulating film formed over the active area (blue); a gate electrode formed over the gate insulating film (pink); first L-shaped sidewalls formed over the side surfaces of the gate electrode (green); first silicide layers formed on regions located on the sides of the first L-shaped sidewalls within the active area (dark pink); an interconnection formed on the trench isolation (pink); and second L-shaped sidewalls formed over the side surfaces of the interconnection (green). As is clearly seen, silicide layers are located on the sides of the L-shaped sidewalls within the active area.

100. An intricate process is necessary to fabricate the device shown Fig. 15(f). Fig. 15(f) is identified as Embodiment 10 of the '174 patent. Exhibit 1001, 26:35 *et seq.* To explain how the device of Fig. 15 is formed, the specification refers back to Embodiment 8, depicted in Figs. 12 and 13. *Id.*, 26:36–27:51.

101. The '174 patent devotes several columns and Figures describing the fabrication process to form the structure of Figure 15(f). "Now, the manufacturing procedures for realizing the structure shown in FIG. 12 will be described referring to FIGS. 13(a) through 13(e)." Exhibit 1001, 22:12-53. In the embodiment shown, the gate electrode **4*a*** (through polysilicon film **4***x*) is applied after the trench isolation is formed (Fig. 13(c); Exhibit 1001, 22:66-23:6).

Benefits Of The Claimed Features Of The '174 Patent And Their Synergies

102. The '174 related to Si integrated circuit (Si IC) fabrication. Si IC fabrication is a multi-hundred-billion-dollar business. Decades ago, more than 100 companies were active in the fabrication of Si ICs. At the present time, there are about 20 major companies active in the field of Si integrated circuits. All fabrication technology has in common that it is based on complementary MOS (CMOS) field-effect transistors, i.e. a combination of n- and p-channel MOSFETs. Each MOSFET has three electrodes, the source (S), gate (G), and drain (D) with the gate consisting of at least a gate insulating film and a gate conductor.

103. Transistors or groups of transistors generally need to be electrically

isolated from one another, which is accomplished by electrical isolation features. A group of transistors may form a small functional unit such as an inverter unit, which is accomplished by electrically interconnecting several transistors with each other by means of interconnects. These interconnects can have a relatively short length ("local interconnects"), medium length ("interconnects") or a relatively long length ("global interconnects" or "Al or Cu interconnects"). The above-recited components, i.e. transistors, isolation features, and interconnects, are the key components of a Si IC that are necessarily found in all Si ICs. Accordingly, the '174 patent recites some of these features, including transistor features, such as a gate insulating film and a gate electrode.

104. The claimed invention of the '174 patent includes multiple elements that (i) are not found in the prior art in the specific combinations taught in the '174 patent, (ii) are not used in the prior art in the specific manner claimed in the '174 patent, and (iii) do not provide the synergies enabled by the '174 patent. An exemplary embodiment of the claimed invention is shown in the figure below ('174 patent figure 15(f)). The figure reveals key elements to be discussed below.

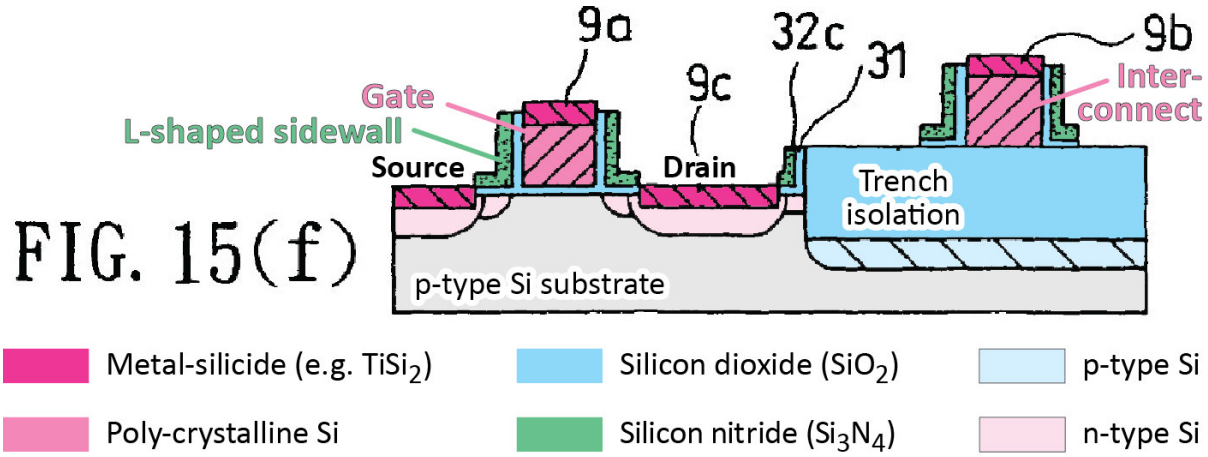



FIG. 15(f)

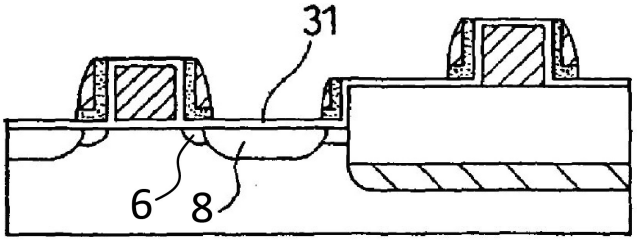
105. ***First key element – trench isolation:*** The trench isolation has a smaller spatial extent than LOCOS isolation thereby allowing for a general reduction of the Si IC's feature sizes and thus allowing for further miniaturization and higher transistor integration density.

106. ***Second key element – L-shaped sidewalls***: The '174 patent teaches gate and interconnect sidewall spacers that include an L-shaped feature. The '174 patent also teaches two major doping implants associated with the L-shaped sidewalls: A *shallow implant* located close to the gate and performed *prior* to the deposition of the L-shaped sidewalls and a *deep implant* located at the S / D contact and performed *after* to the deposition of the L-shaped sidewalls. The two implants are bath-tub shaped as illustrated in the '174 patent's Figure 15(d), shown below. Inspection of the figure reveals a shallow implant **6** ("low-concentration source/drain region **6**" Exhibit 1001, 2:58-59)[11] and deep implant **8** ("high-

[11] Numeral "6" was added to Figure 15(d) for clarity.

concentration source/drain region 8" Exhibit 1001, 2:59).

FIG. 15(d)




107. The shallow implant generally has a relatively lower concentration of doping atoms and therefore can be referred to as a *low-concentration implant*. The deep implant generally has a relatively higher concentration of doping atoms and therefore can be referred to as a *high-concentration implant*.

108. The sidewall disclosed in the '174 patent has multiple purposes including the following: *First*, the sidewall controls the deep implant by serving as a mask during the implantation process. The two implants denoted by numerals 6 and 8 are fabricated as follows:

> Each of the sidewalls has a width of, for example, approximately 0.1 μm. After forming the polysilicon electrode **4***a*, an n-type impurity with a low concentration is ion-injected into the active area, so as to form a low-concentration source/drain region **6**. After forming the electrode sidewalls **7***a*, an n-type impurity with a high concentration is ion-injected into the active area, so as to form a high-concentration source/drain region **8**. This is a generally adopted method of manufacturing a MOSFET having the so-called LDD structure.

Exhibit 1001, 14:58-67 (emphasis added).

109. The L-shaped sidewall as disclosed in the '174 patent includes a "protection oxide film **31**" ($SiO_2$), a "silicon nitride film **32**" ($Si_3N_4$), and a "polysilicon film **33**" (poly-Si) with the "silicon nitride film" being an L-shaped feature[12]. Exhibit 1001, 26:45-46.

110. The employment of L-shaped sidewalls allows for precise control of the shallow implant since the shallow implant is performed ***before*** the deposition of the sidewall, i.e. closer to the edge of the gate electrode. Furthermore, the sidewalls disclosed in the '174 patent are excellent barriers against impurity diffusion and migration. The L-shaped sidewalls disclosed in the '174 patent are *multilayer* sidewalls with the individual layers being made of different materials. As noted above, the '174 patent discloses sidewalls that include a "protection oxide film **31**" ($SiO_2$), a "silicon nitride film **32**" ($Si_3N_4$), and a "polysilicon film **33**" (poly-Si). Exhibit 1001, 26:45-46. Due to the multilayer nature of the sidewall, the sidewalls act as effective barriers against impurity diffusion and migration.

111. One of the benefits afforded by the invention of the '174 patent is that no alignment margin is needed for the W (tungsten) contact plug. As a consequence of the claimed L-shaped sidewalls, the claimed silicidation of the S/D contacts, and the claimed trench isolation, a W (tungsten) plug may straddle the

[12] The "polysilicon film **33**" may be removed in subsequent processing.

$Si/SiO_2$ boundary (active-region/trench-isolation boundary) so that no alignment margin is needed (that would prevent the W plug from being partially formed on the trench isolation). The '174 patent states: "There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed." Exhibit 1001, Abstract. The '174 patent further states: "In this method, in the fourth step, an alignment margin is not provided for preventing the exposing area of the masking member from including a portion above the isolation when mask shift is caused in photolithography." Exhibit 1001, Summary of the Invention, 8:36-40.

112. The claimed trench isolation in conjunction with the advantageous features taught in the specification (avoidance of the intrusion of the silicided region into the trench isolation region that occurred in the prior art as illustrated in the '174 patent's Figure 21) results in no alignment margin being required at the boundary between the active region and the trench isolation region. That is, silicidation of S/D electrodes next to a trench isolation can be accomplished (without margin). The L-shaped sidewalls give the control over the low-doped region, high-doped region, silicided region, and contact region. Without trench isolation, L-shaped sidewalls and silicidation of electrodes, such lack of alignment margin would not be possible.

113. The L-shaped sidewalls provide protection from intrusion of silicide formed in the S/D contact regions. Metal silicides are formed by means of a chemical reaction between a deposited metal and the Si substrate. The chemical reaction can proceed in multiple directions. The silicide must not intrude into the low-doped S/D region. The L-shaped sidewalls provide excellent protection from such intrusion.

114. The L-shaped sidewalls provide electrical insulation of the gate electrode and interconnect electrode from other electrically conductive elements that are close to the gate / interconnection electrode. A short-circuit between the different gate / interconnection electrodes and other conductive elements can thus be avoided.

115. The method by which L-shaped sidewalls are employed in the prior art cited by Petitioner, i.e., in the *Lee and Lowrey* patents, is very different from the method employed in the '174 patent. ***Lee***: *Lee* performs the shallow implant ***after*** the formation of the L-shaped sidewall not ***before*** as taught in the '174 patent. Similarly, *Lowrey* performs the shallow implant ***after*** the deposition of a first sidewall component, not ***before***, as taught in the '174 patent.

116. ***Third key element – Silicide***: Another key feature of the '174 patent are silicide S / D contacts. Silicides, such as titanium disilicide, $TiSi_2$, are more metal-like than a semiconductor and thus allow for very low contact resistances.

Silicides are formed by a chemical reaction and thus can have a similar tendency as the LOCOS isolation: Silicides can encroach on other elements of the integrated circuit (e.g. by silicide intrusion, bridging, or spiking). The L-shaped sidewalls help in reducing, limiting, and controlling such encroachment near the gate as well as near the trench isolation.

117. There are synergies that arise from the claimed invention, specifically the combination of the claimed L-shaped sidewalls, claimed silicidation, and the claimed trench isolation.

118. ***Synergistic benefit****: No alignment margin needed.* As a consequence of the claimed L-shaped sidewalls, silicidation of S/G/D, and the claimed trench isolation, a W plug may straddle the $Si/SiO_2$ boundary (active-region/trench-isolation boundary) so that no alignment margin is needed (that would prevent the W plug from being partially formed on the trench isolation). The '174 patent states: "There is no need to provide an alignment margin for avoiding interference with the isolation and the like to a region where a connection hole is formed." Exhibit 1001, Abstract. The '174 patent further states: "In this method, in the fourth step, an alignment margin is not provided for preventing the exposing area of the masking member from including a portion above the isolation when mask shift is caused in photolithography." Exhibit 1001, Summary of the invention.

119. ***Synergistic benefit****: Greater tolerance afforded.* As a consequence of

the claimed L-shaped sidewalls, silicidation of S/G/D, and the claimed trench isolation, the invention disclosed in the '174 patent allows for a greater tolerance in the alignment of a W contact plug on the S / D contact so that these contact plugs can terminate (or 'land') not only on the S / D regions, but in part also on the trench isolation. The '174 patent states:

> In addition, the area of the active area can be decreased because no alignment margin from the isolation is provided, resulting in improving the integration of the manufactured semiconductor device.

Exhibit 1001, Summary of the Invention.

120. The silicidation of the S/D electrode allows for low contact resistance. This allows for the W plug to only *partially* contact the S/D electrode. Furthermore, the high control afforded by the L-shaped sidewalls and their excellent insulating properties (and diffusion-barrier and migration-barrier properties) allow for clear separations between the lowly-doped region, highly-doped region, silicided region, and contact region.

121. The availability of L-shaped sidewalls enhances the control over silicided S / D areas. The silicided S / D areas are formed by a chemical reaction between a metal (e.g. Co, Ti, Ni) and the Si substrate. As a consequence, intrusion, bridging, and spiking of the silicide can occur. The L-shaped sidewalls preserve the advantage of greater tolerance for the W plug while allowing for the control

over the silicided S / D.

122. ***Synergistic benefit****: L-shaped sidewalls are superior to single-material sidewalls.* The L-shaped sidewalls disclosed in the '174 patent may include a protective oxide layer ($SiO_2$), a silicon nitride layer ($Si_3N_4$), and a polysilicon layer (poly-Si). Multi-material sidewalls are superior over a single-material sidewall when the sidewall acts as a barrier against the unwanted diffusion and migration of impurities.[13]

123. The optimized transistor structure disclosed in the '174 patent includes four distinct regions for S/D: The (i) lowly-doped / low conductivity region close to the channel, (ii) highly-doped / high conductivity region farther away from the channel, (iii) silicided / very high conductivity region, and (iv)

[13] Thin films can have pinholes. In films consisting of multiple layers of different materials, it is very unlikely that the pinholes in each of the multiple layers align with each other. That is, the probability of a pinhole penetrating the entire multilayer film is extremely low. As a consequence, multilayer films are highly effective as diffusion barriers. In addition, due to the high interconnectedness of the molecular bonds in silicon nitride (Si forms four valence bonds and N forms three valence bonds), the Si3N4 layers of the sidewalls by themselves are excellent barriers against the diffusion and migration of unwanted impurities.

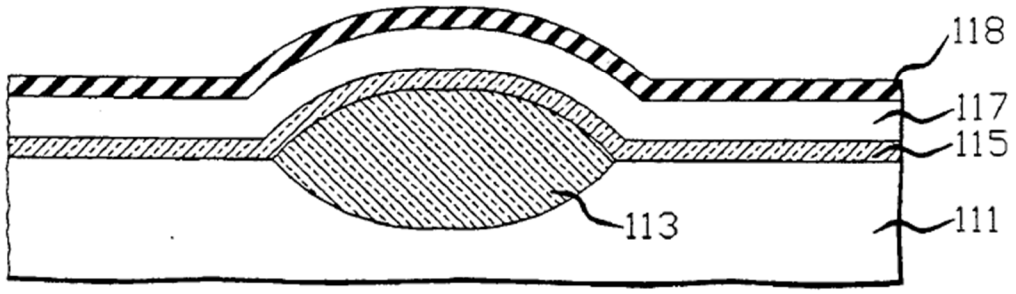
contact region (where the W plug is in contact with the silicide). The delineation between these regions must not be blurred. In addition, chemical elements from these regions must not diffuse or migrate through the L-shaped sidewalls or into the trench isolation region. The unique combination of trench isolation, L-shaped sidewalls, and silicided regions (as taught in the '174 patent) allows for this benefit.

**Applied Prior Art**

U.S. Patent No. 5,153,145 ("*Lee*")

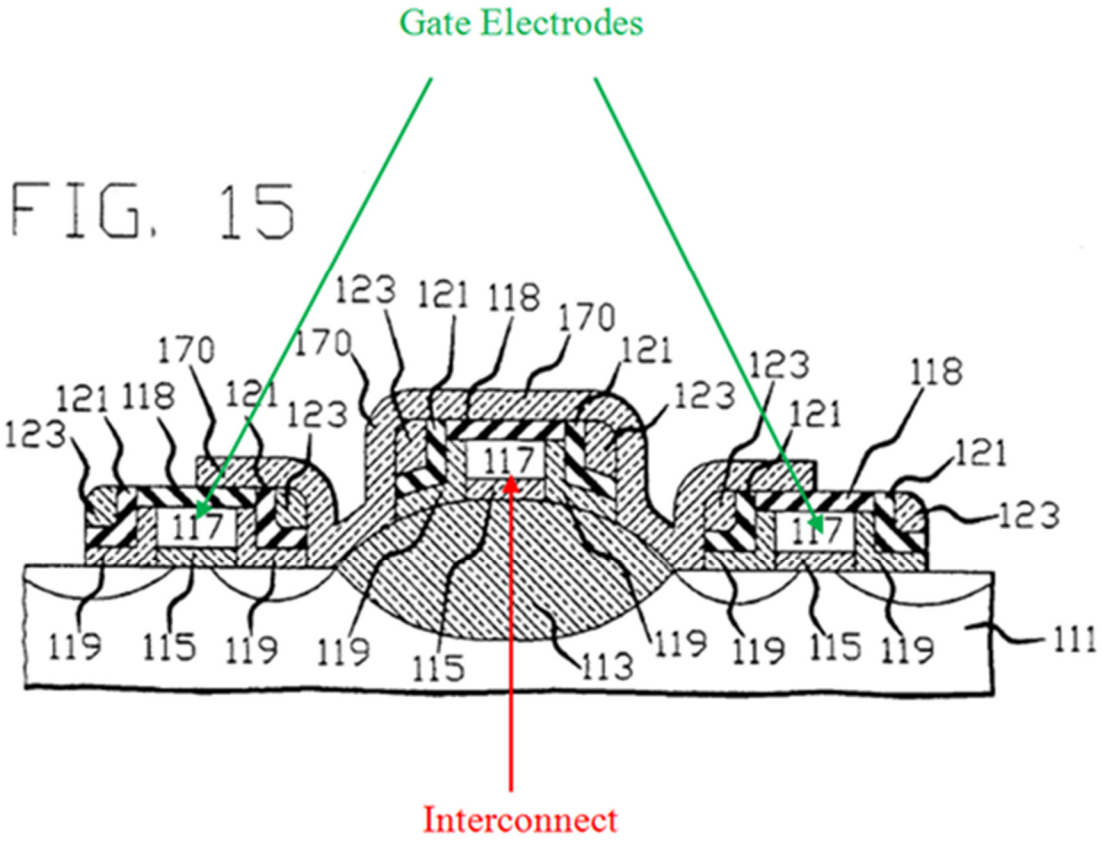
124. *Lee* concerns a "semiconductor integrated circuit structure and method of fabrication." Exhibit 1002, Abstract. The first processing step is the formation of the LOCOS isolation denoted by numeral **13** (LOCOS "field oxide"). Exhibit 1002, 2:34-35. The LOCOS isolation defines the active Si field where transistors will be located. The LOCOS isolation field oxide **13** is shown in *Lee*'s Figure 11 (numeral **113** in Figure 11), reproduced below.

FIG. 11




125. *Lee* does not teach "a trench isolation surrounding an active area of a semiconductor substrate," since *Lee* teaches LOCOS isolation instead of trench isolation. Petitioner asserts that it would have been obvious to modify *Lee* using *Noble's/Ogawa's* teaching of shallow trench isolation in place of LOCOS isolation. Petitioner relies primarily on Figures 11-15 of *Lee* for their combination.

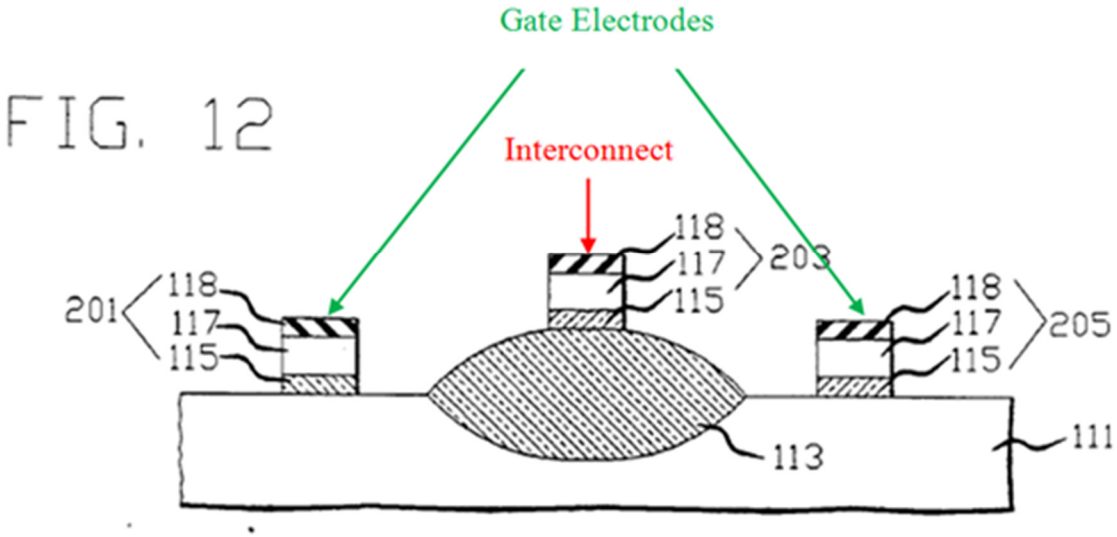
126. *Lee's* basic design is centered on the use of the gate conductor **117** to serve a dual purpose – it serves to form the gate electrodes over the active areas, and it extends directly as a "gate runner" or simply "runner" to form the interconnect on top of the isolation.




127. *Lee* is able to achieve this structure because *Lee* first forms the LOCOS isolation and lays down layers **115**, **117** and **118** thereafter.

128. Layers **115**, **117** and **118** will form gate stacks **201**, **203** and **205**.[14]

[14] The "gate conductor" is frequently called the "gate electrode." The "gate dielectric" PLUS the "gate conductor" can be referred to as the "gate layer stack" or simply "gate stack." The "gate stack" may also include the layer **118**. *Lee* calls **201** and **205** the "gates" and **203** the "gate runners" or simply "runners."



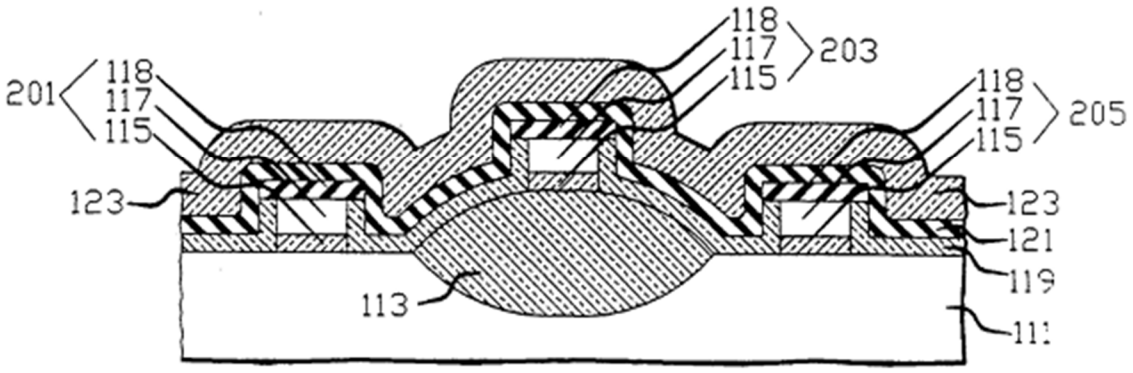

129. By proceeding in this fashion, there is a gate electrode including "runner" (aka gate conductor) **117** which "runs" over the LOCOS. Runner **117** is continuous thereby inherently connecting gate stacks with interconnections.

130. Subsequent to the formation of the LOCOS isolation, the layers of gate dielectric **15** ("gate dielectric," numeral **115** in Figure 11) and gate conductor **17** ("a layer [of] conductive material which may be, for example, polysilicon," numeral **117** in Figure 11) are deposited. Exhibit 1002, 2:46-59. Subsequently, the gate dielectric film and gate conductor film are structured into the gate dielectric and gate electrode by means of photolithography. Inspection of *Lee*'s Figure 1 reveals that the LOCOS isolation is formed prior to the gate dielectric **15** and gate conductor film **17**.

131. *Lee*'s "L-shaped" spacers (Exhibit 1002, 3:8-21) are formed by etching away layers **119** and **121** shown in Fig. 13. Layers **115**, **117** and **118** are

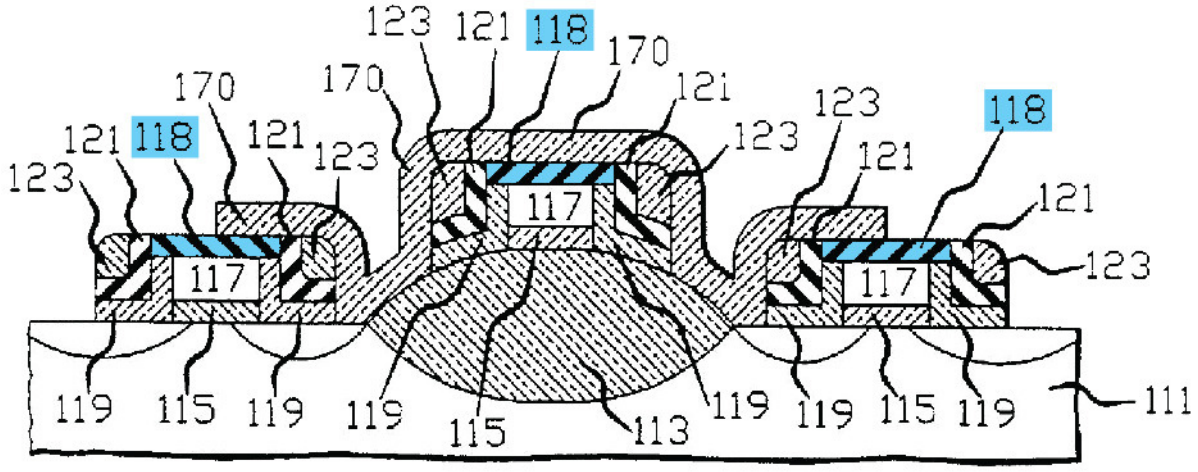
"typically formed during initial steps of semiconductor fabrication." Exhibit 1002, 6:53-56. The purpose of the "L-shaped" spacers is to allow for the specific method used by *Lee* to dope the source/drain regions. *Lee*'s method includes the implantation into the Si partially through the sidewalls, rather than using the sidewalls as a mask for the implantation. *Lee* discloses: "Referring first to FIG. 5, an ion implantation step, shown schematically by species denoted by reference numeral **31** is performed to form deeply-doped junctions **25** and **27**." (Exhibit 1002, 3:51-54) (Emphasis added.) *Lee* then discloses: "After spacer **23** has been removed. a second implant using ion species **37** shown in FIG. 6 is performed. The second implantation species must penetrate the 'foot' of spacers **21** and **19**. The foot serves to absorb some of the ionic species. Thus, creating shallow junction regions **33** and **35** in portions **28** and **30** of substrate **11**." (Exhibit 1002, 4:24-29) (Emphasis added.). That is, *Lee*'s removal of spacer **23** enables the shallow implant contrary to the teachings of the '174 patent. In summary, the *Lee* sequence and the '174 sequence with respect to the deep/shallow S/D implant are opposite, the purposes of the sidewalls are different, and the function of the individual elements are different.

FIG. 13




132. A significant aspect of *Lee* is its desire to insulate its gate stacks, not only with vertical sidewalls, but also with "insulating caps" **118** on top of the gate stacks. These "insulating caps" help encapsulate the gate conductors to protect against shorting. These "insulating caps" are inconsistent with the use of a conductive wiring level on top of the gate stacks (and in electrical contact with the gate conductor as practiced by *Noble* and *Ogawa*). *Lee*'s Figure 15, below, shows that the "insulating caps" **118** are required to prevent an electrical short between the gate conductor **117** and the local interconnect **170** ("overlying conductive layer **170**"). However, when using the trench isolation of *Noble* or *Ogawa*, which is based on the use of a conductive wiring layer ("conductive wiring level **140**" in *Noble*, and "molybdenum silicide ($MoSi_2$) layer **56**" in *Ogawa*), an "insulating cap" **118** would make the gates non-functional.

FIG. 15




U.S. Patent No. 5,021,353 ("*Lowrey*")

133. *Lowrey* concerns the fabrication of a Si IC device. *Lowrey* states: "By processing N-channel and P-channel devices separately, the number of photo masking steps required to fabricate complete CMOS circuitry in a single-polysilicon-layer or single-metal layer process can be reduced from eleven to eight." Exhibit 1017, Abstract. *Lowrey* Figures 1-4 illustrate the first, second and third photomasking steps. Exhibit 1017, 7:57-8:30. The LOCOS oxidation only occurs after these initial steps, i.e. after multiple photomasking steps. Dr. Banerjee contends: "[LOCOS in *Lowrey* and STI in *Noble*] are both performed near the very beginning in device processing." Exhibit 1024, ¶93. I disagree. LOCOS in *Lowrey* is not performed "near the very beginning in device processing". It is in fact performed after several photomasking steps have been completed, but still before the gate layer stack is applied.

134. The *Lowrey* process sequence uses eight (8) masking steps instead of the eleven (11) steps (required prior to *Lowrey*) on an unprocessed silicon wafer. *Id.*, 10:43-46. *Lowrey* Figs. 1-4 illustrate the first, second and third photomasking steps. *Id.*, 7:57-8:30. These photomasking steps are undertaken *before* LOCOS oxidation takes place. The fabrication process starts with a first pad oxide layer **11** that is grown on a lightly doped silicon substrate. A silicon nitride layer **13** is then deposited on top of the first pad oxide layer, after which a first photomask **14** is used to expose only those regions on the Si substrate which are to receive a first phosphorus implant.

135. Referring to *Lowrey*'s Fig. 5, and as described in *Lowrey*, it is only after the stripping of the third photomask that field oxide regions **51** are grown using a conventional LOCOS oxidation process. Exhibit 1017, 8:31-35.

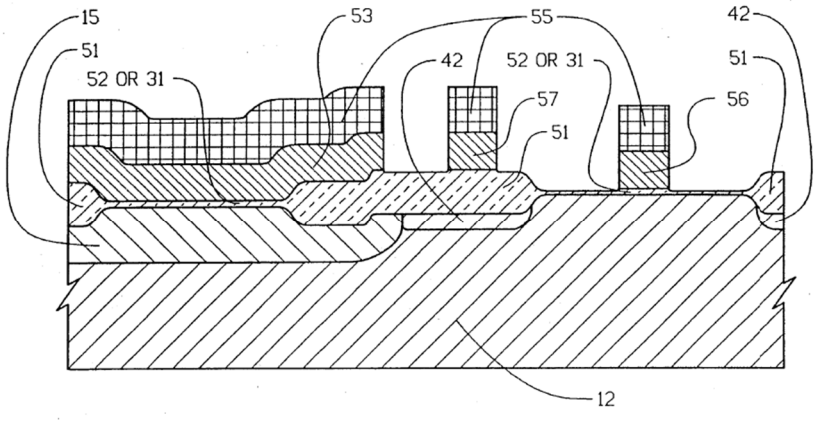



FIG. 5

136. *Lowrey* has sidewalls, which in their final form do not substantially resemble a capital "L" shape.

137. In *Lowrey,* the "L-shaped" sidewall members (Fig. 8) are not actually L-shaped structures at all. The "L-shape" shown in *Lowrey* is simply used as a convenience to illustrate the process by which the device is formed, and does not represent a distinguishable component of the sidewall. In particular, in *Lowrey*, mini-spacer oxide layer **62**, which covers transistor gates **56** and N-channel interconnects **57** is initially deposited, and then mini-spacer oxide layer **62** is blanketed followed by first spacer oxide layer **71** (Fig. 7 below).

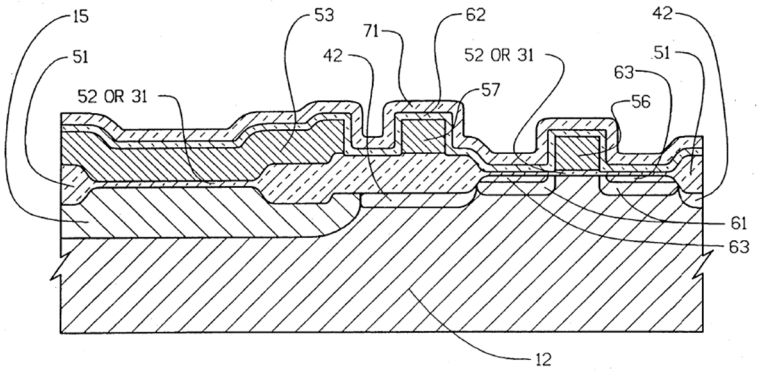



FIG. 7

138. Then, as shown in Figure 8, layers **62** and **71** are etched with an anisotropic etch, and then optionally isotropically etched again to form a first set of sidewall spacers **81**. The etch is used to remove most of the spacer oxide layers, but not to the point where the substrate is cleared. Then, a selective wet etch is used to clear the substrate. Exhibit 1017, 8:53 – 9:22.

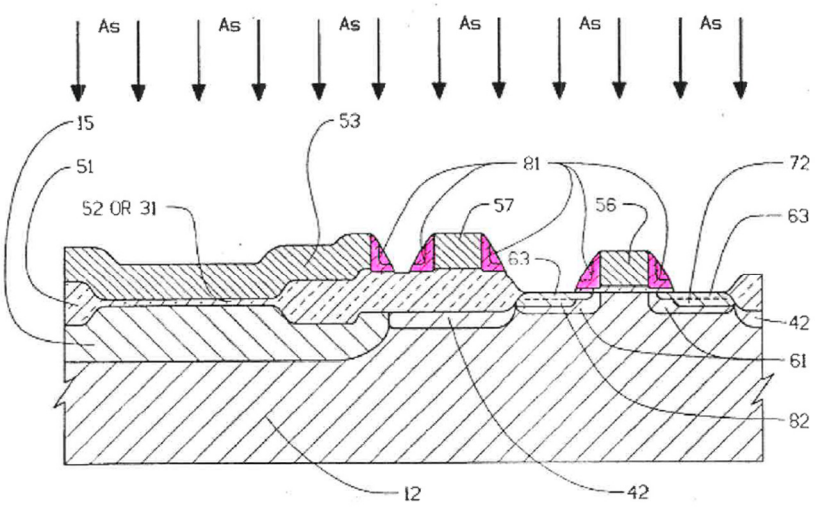



FIG. 8

139. As a result, both layers **62** and **71** are made of silicon oxide and thus, the two layers **62** and **71**, taken together, substantially appear as one, and do not substantially resemble an "L-shape," but instead resemble a rounded triangle **81**. This is because the boundary between the two layers is not "visible" to the type of equipment normally used to examine such layers (scanning electron microscopy, SEM) and thus, no component of the sidewall substantially "resembles a capital L." That is, there are no first or second L-shaped sidewalls in the final device.

140. The reason that the two layers, **62** and **71** are separately applied is to allow for two sequential implantations, a shallow implant and a deep implant. The lower layer, **62**, may appear as an "L" in the *Lowrey's* Figures because *Lowrey* is consistently showing that the sidewall is formed in a multi-step process that

involves the deposition of two layers of silicon oxide, **62** and **71**. But when the same compound is overlaid twice to form the sidewalls consisting of the same material, the boundary between the two layers becomes indistinguishable, such that the original two distinct layers, **62** and **71**, appear as one single entity, **81**, i.e. a sidewall structure without an L-shaped component.

141. Importantly, as processing proceeds, a non-planar wafer surface topology is being built up. For example, *Lowrey*'s Figure 4, reproduced below, shows a non-planar topology including a step in the Si wafer surface. Such non-planar topology would not be acceptable when forming trench isolation.

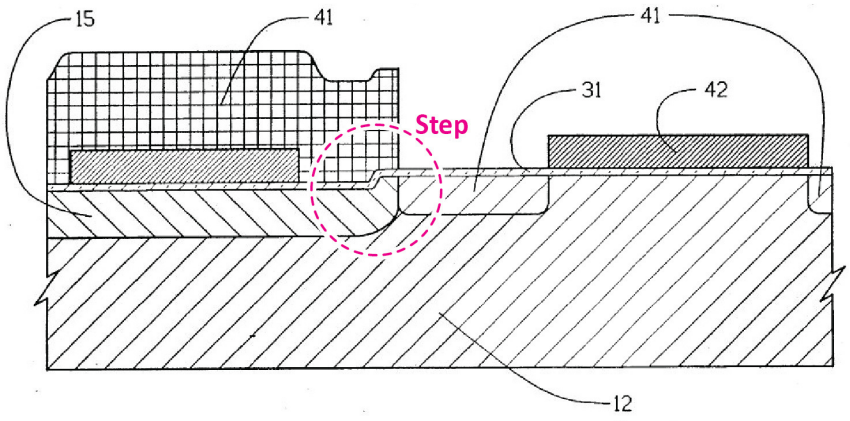



FIG. 4

142. Then, Fig. 5 reproduced below, after the LOCOS isolation **51** (pink) has been formed, gate oxide and gate conductor electrode are laid down, and then etched such that the gate electrodes **53**, **56**, and **57** (green) remain, with the gate conductor electrode **57** sitting on top of the LOCOS isolation and acting as an interconnection. Exhibit 1017, 8:31-57. There are no schematics illustrating the

steps between Figures 4 and 5; instead the text explains the intervening processing steps.

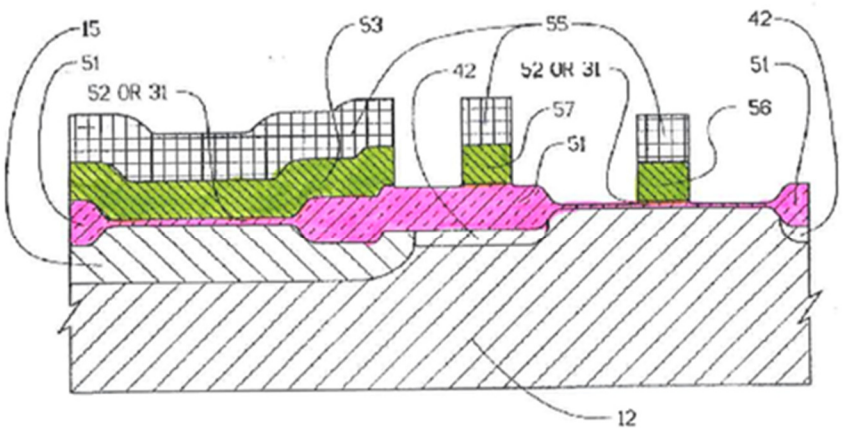



FIG. 5

143. As a result of further patterning and etching, the gate electrodes and the interconnections are left with sidewalls formed on them. Fig. 7 shows the device after deposition of layer **62** ("mini-spacer oxide layer **62**") and **71** ("first spacer oxide layer **71**"). The mini-spacer oxide layer **62** coats the sides of transistor gates **56** so that when the wafer is subjected to doping regions **63**, which are offset from the vertical boundaries of punch-through implant regions **61** by the vertical segments of mini-spacer oxide layer **62** on the edges of N-channel transistor gates **56.** Exhibit 1017, 8:61-9:2.

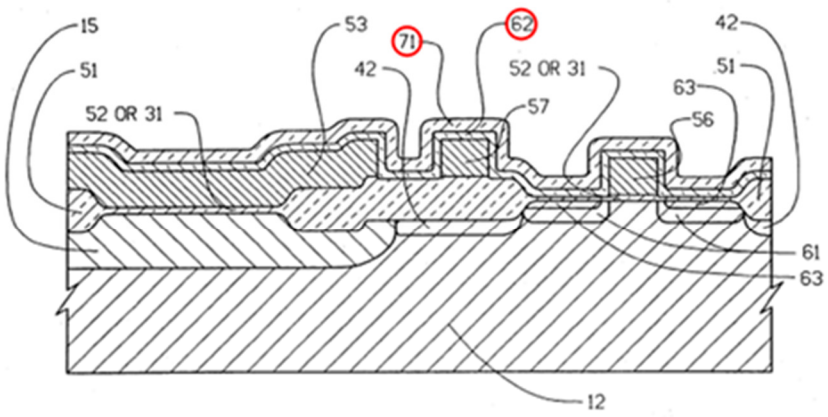



FIG. 7

144. However, after a subsequent etch, the distinction between layers **62** and **71** disappears (no separate reference to **62** and **71**), and the patent then refers to the combined sidewall by numeral **81**.

145. Referring now to FIG. 8, first spacer oxide layer **71** and mini-spacer oxide layer **62** are etched with a first anisotropic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers **81** for N-channel transistors gates **56**, N-channel interconnects **57** and the portion of polysilicon layer **53** which blankets the P-channel regions. Exhibit 1017, 9:6-12.

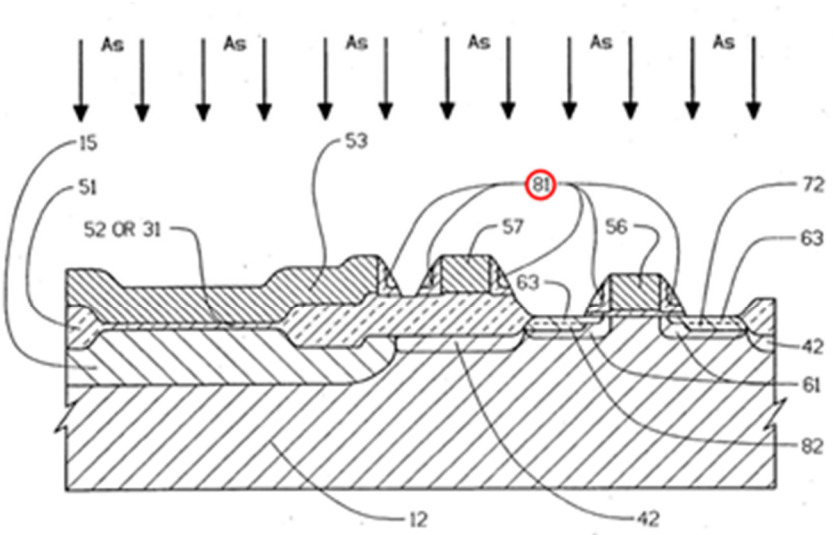
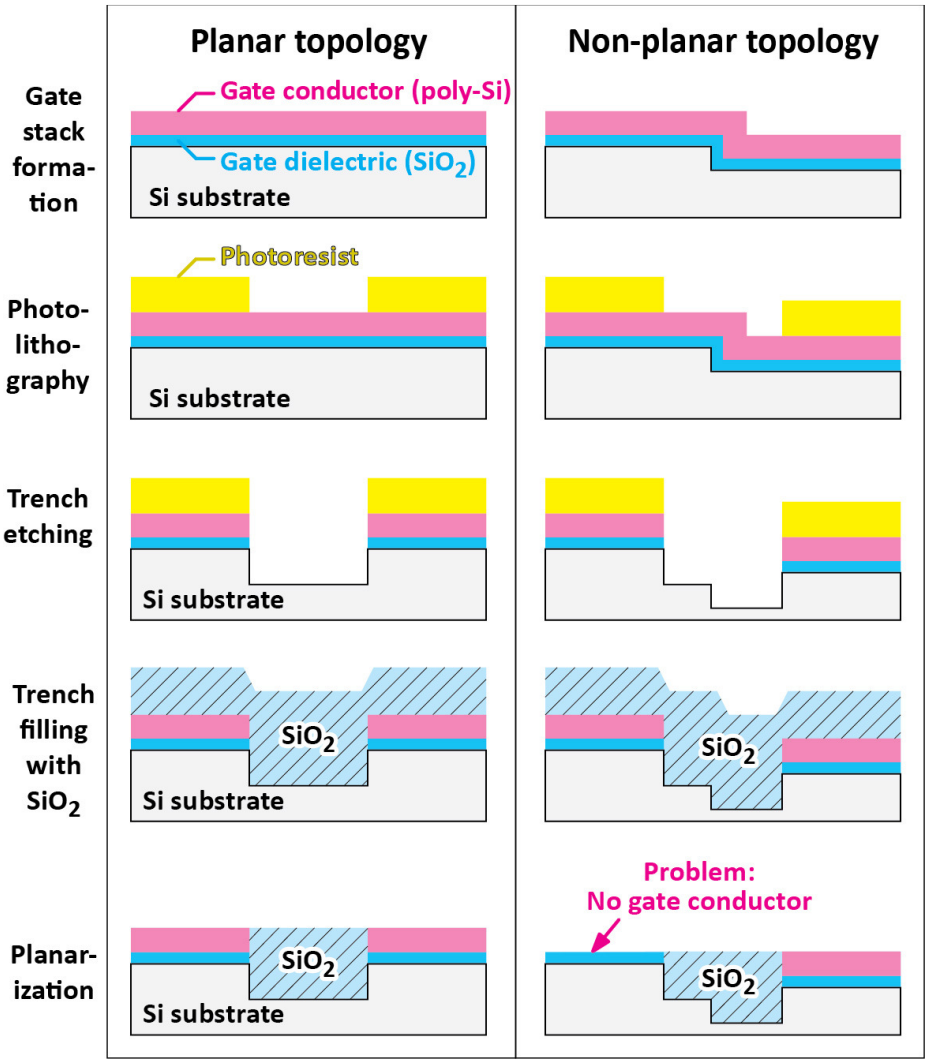



FIG. 8

146. The schematic figure below shows the formation of trench isolation on a wafer having (i) planar surface topology (left-hand side column) and (ii) non-planar surface topology (right-hand side column). The steps indicated are gate stack formation, photolithography, trench etching, trench re-filling with silicon dioxide, and planarization.

147. The figure also shows the problem that arises when forming a trench isolation feature on a wafer having non-planar surface topology (such as *Lowrey*): Due to the non-planar starting topology, a structural element (e.g. the gate conductor) partially vanishes during planarization (see bottom figure at right). Such destruction of a structural element is not acceptable. For this reason, the

formation of trench isolation in *Lowrey* (at the stage where *Lowrey* performs LOCOS isolation) would be unacceptable.[15]




[15] By definition, a planarization process (such as CMP) planarizes a non-planar surface topology. Planarization indeed is the very purpose of the CMP process. However, in the specific context of *Lowrey*, the CMP process associated with the trench isolation formation would be harmful as illustrated in the figure and would inevitably destroy part of the structure (by removing wanted material or leaving unwanted material).

U.S. Patent No. 5,539,229 ("*Noble*")

148. *Noble* discloses a MOSFET with raised STI[16] self-aligned to the gate stack along the gate width direction. The gate conductor has first and second edges bounded by raised isolation structures (i.e. STI). A source is self-aligned to the third edge and a drain diffusion is self- aligned to the fourth edge of the gate electrode. Exhibit 1015, Abstract, 2:54-56. The process of forming the trench isolation is described in the summary of the invention wherein it is specifically stated that: a gate dielectric layer and a gate conductor layer are first deposited wherein the first portion of the gate stack is removed to allow for etching of a trench. Exhibit 1015, 2:58-63. *Noble* is directed to the self-alignment of the gate stack with respect to the STI (shallow trench isolation); this requires (as a pre-requisite) the deposition of layers **14** and **116** *before* the trench is formed. *See* Exhibit 1015, Fig. 10.

149. *Noble* points out problems associated with forming the trench isolation prior to depositing the gate dielectric and conductor ("wrap-around effect" and "Corner Parasitic Device") (Exhibit 1015, 1:31-33 and *Noble*'s citation of the 1988 Furukawa article "Process and Device Simulation of Trench Isolation Corner Parasitic Device", Exhibit 1015, 1:23-26). In consideration of this warning,

[16] STI is an acronym for shallow trench isolation.

*Noble* discloses the deposition of the gate dielectric layer and gate conductor layer before the trench formation. This sequence is evident from *Noble*'s Figure 10, shown below and inherent to the process design and engineering of *Noble*. A POSITA would have no reason whatsoever to ignore *Noble*'s warning. Indeed, a trench isolation formation without the pre-deposited structures would substantially deviate from the teaching of *Noble* and thus be unacceptable.

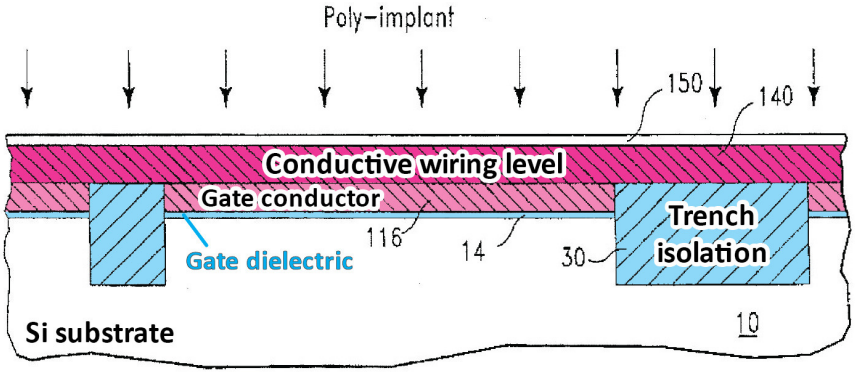



FIG. 10

150. *Noble* was preoccupied with the problems associated with forming the trench isolation prior to laying down the gate conductor. *Noble* discloses, before trench formation, the deposition of the gate dielectric layer and gate conductor layer. This sequence is part and parcel of the process design and engineering of *Noble*, and a POSITA would have absolutely no reason whatsoever to ignore it since the trench isolation that would be formed without these pre-deposited structures would be unacceptable.

151. Entirely missing from *Noble* are the claimed first L-shaped sidewalls formed over the side surfaces of the gate electrode, and second L-shaped sidewalls

formed over the side surfaces of the interconnection. Moreover, a POSITA would not have formed the sidewalls. This is because the purpose and function of the sidewalls in *Noble* and *Lee* are different, so that they are not amenable to substitution. Different from *Lee*, *Noble* uses S/D extension implants prior to the deposition of the sidewalls. In this regard, *Noble* states:

> In the aspect of the invention illustrated in FIGS. 9-13 a source/drain extension is first formed by implanting a medium dose (less than 1 x $10^{14}$ $cm^{-2}$) of a dopant such as arsenic or boron, for source/drain **138** before spacers **152** are formed (FIG. 11)."

Exhibit 1015, 6:13-17. (emphasis added).

152. Different from *Lee*, *Noble* uses a diffusion process to form ultrashallow S/D junctions after the spacers are formed.

In this regard, *Noble* states:

> Then, after spacers **152** are formed (FIG. 12), intrinsic polysilicon (or intrinsic amorphous silicon) is deposited or selective silicon is growth for raised source/drain **154** as shown in FIG. 13. Dopant for the raised source/drain is implanted at low energy so as to avoid damage to the single crystal silicon below. Then the dopant is diffused from the polysilicon to form [source/drain] ultrashallow junctions **156** without damage.

Exhibit 1015, 6:17-24 (emphasis added). Based on these differences, a POSITA implementing *Noble*'s transistor would not be motivated to implement the spacers **152** using the L-shaped sidewalls of *Lee*.

153. Furthermore, as explained earlier, *Noble* deposits the gate dielectric and gate conductor film ***before*** forming the STI (isolation field oxide). The first step of *Noble* is the deposition (or growth) of the thin gate dielectric film **14** ("gate dielectric") and the gate conductor **116** ("gate conductor") on substrate **10**. It is only thereafter, that the raised shallow trench isolation (STI) **30** ("raised STI") is formed so as to define and surround the active area. The STI process concludes with a planarization step (*e.g.* CMP) that leaves the Si wafer (substrate **10**) surface planarized or flat as shown in *Noble*'s Fig. 9.

154. Pointing to *Noble's* Fig. 13, Petitioner notes that *Noble* illustrates trench isolation in a semiconductor, together with a variety of other components. '1246 and '1247 Petitions, p. 19. Petitioner, however, completely and conveniently overlooks the deposition of the gate layer film which is, in effect, a prerequisite to the formation and very existence of the trench isolation.

155. Entirely missing from *Noble* are the claimed first L-shaped sidewalls formed over the side surfaces of the gate electrode, and second L-shaped sidewalls formed over the side surfaces of the interconnection.

156. Petitioner relies on *Lee* to teach the "L-shaped" sidewalls, but never explains how the sidewalls of *Lee* could still be formed once the trench isolation of *Noble* was formed.

157. *Noble's* configuration is different from *Lee* (and the process sequence is opposite to *Lee*) and needs a conductive wiring level **140** on top of, and separate from, the gate conductor electrode **116** in order to connect the gate stack to the interconnection.

158. This configuration is achieved because *Noble* begins the fabrication process by first laying down layers **14** and **116** and then boring (or etching) through these layers to form a trench that is then filled with oxide material. The opening formed through layers **14** and **116** is bordered by these two layers.

159. After the raised trench isolation is formed, layers **140** and **150** are applied. Layer **140** is a conductive wiring level.

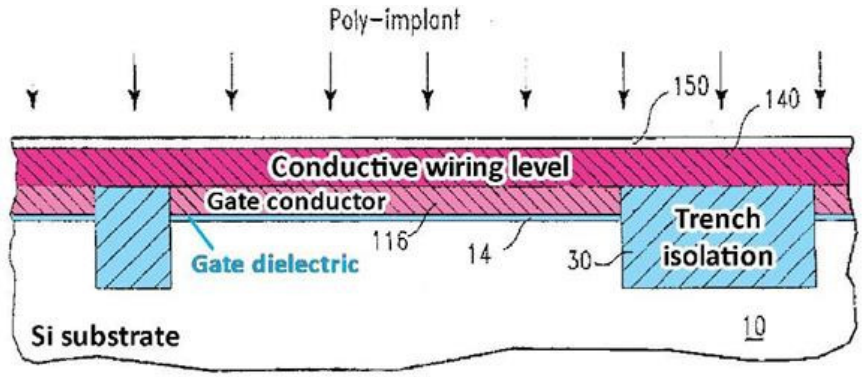



FIG. 10

160. There is no gate conductor electrode **116** on top of the isolation acting as a "runner" i.e. interconnection. Conductive wiring **140** is all that is needed. Fig. 11 illustrates the device after patterning/etching of layers **140** and **150**.

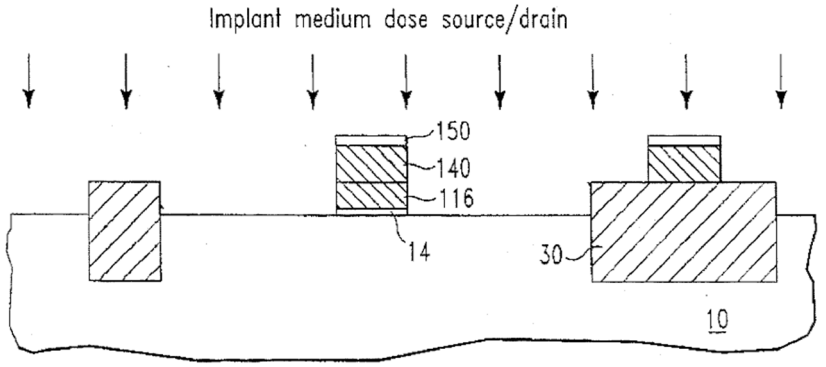



FIG. 11

U.S. Patent No. 4,506,434 ("*Ogawa*")

161. *Ogawa* states that polycrystalline silicon (Si) layer **43** can also function for production of electrodes for gates and or some of the metal wiring (Exhibit 1010, 7: 35-37), and this is what is shown in Figs. 5(a) – 5(c) which depict a substrate including trench isolation **52** (previously designated as **47**). After planarization etching, the trench isolation **52** and gate electrode are overlaid with molybdenum silicide layer **56** which, as shown in Fig. 5(b), extends from the upper surface of the trench isolation to the top of polycrystalline silicon layer **55**.

162. Significantly the trench isolation is formed near the beginning of the process, but after the gate electrode layer **55** has been applied as in Fig. 5(c) above.

163. The trench formation process of *Ogawa* involves a trench isolation **52**, which is necessarily surrounded by layers **54** and **55** (Fig. 5(b)). There is no gate electrode on top of the trench isolation **52** because of the way that the trench isolation is formed. With no gate electrode on top of the trench isolation, there would be no L-shaped sidewall member on the interconnection as claimed (to be discussed in detail below).

164. *Ogawa*, issued in 1985, was an early attempt at trench isolation, but was not practical in the early 1990s. Without a viable planarization process, the repeated deposition and lateral structuring of layers would build up a topology characterized by hills (*e.g.*, where wires crossed other features) and valleys (*e.g.,* where no material is deposited). Once such topology has been built up, it needs to be protected and cannot be planarized without damaging these features.

165. Like *Noble*, *Ogawa* relies on the initial deposition of the gate dielectric and gate conductor prior to the trench formation. Therefore, the same or similar arguments used for *Noble* and the *Lee-Noble* combination apply to *Ogawa* and the *Lee-Ogawa* combination.

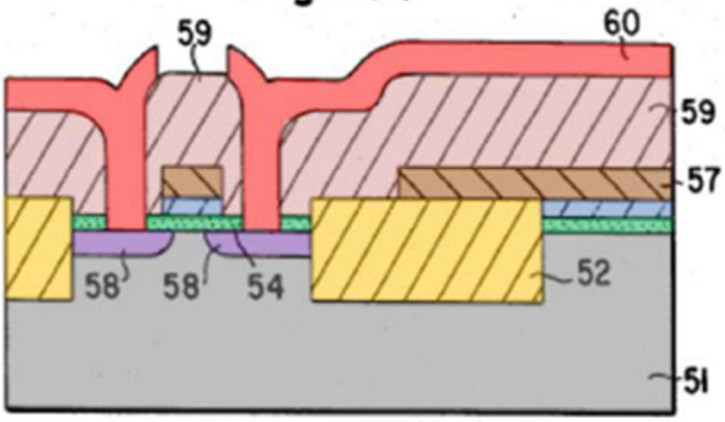
166. *Ogawa* suffers from not teaching a viable planarization process. In *Ogawa*, planarization is done by attempting to dry etch photoresist and silicon dioxide ($SiO_2$) at an equal etch rate. An equal etch rate is very difficult to attain because the substances being etched in *Ogawa* are so different (photoresist is an

organic, soft, and temperature-unstable material, whereas $SiO_2$ is a hard, brittle, and temperature-stable material). Taking into account (i) the photoresist's unavoidable variation of the etching rate with temperature and (ii) the unavoidable temperature variations (temperature rise) during the etching process makes the *Ogawa* planarization process inherently deficient.

167. Not surprisingly, trench isolation was not introduced in Si IC fabrication based on *Ogawa*. *Ogawa* simply lacked the maturity of a stable and viable planarization process. For this reason, a POSITA when trying to modify *Lee*, would not have resorted to *Ogawa*, which inherently included an early, primitive and unreliable trench isolation formation process.

168. *Ogawa* discloses a method for producing semiconductor devices in which a trench isolation is formed. Petitioner relies upon Fig. 5(c) which shows a raised trench isolation **52**. '1246 Petition, p. 20. Petitioner never discusses how trench isolation **52** is formed. However, the formation process of the trench isolation is relevant.

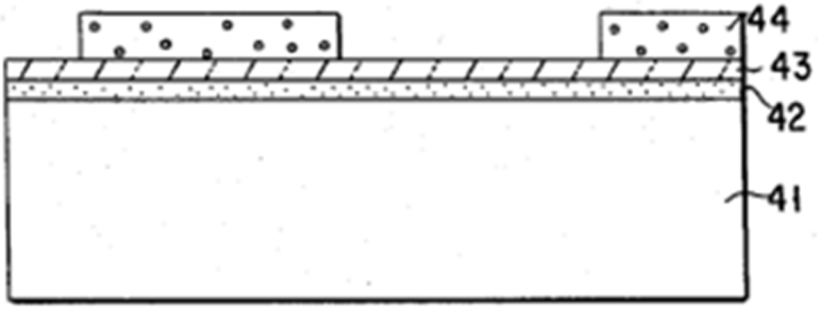
Fig.5(c)




51—Substrate (Si)
52—Buried Oxide ($SiO_2$)
54—Gate Oxide ($SiO_2$)
55—Polysilicon Layer
57[sic]—Gate Electrode/Interconnect (silicide)
58—Source/Drain
59—Interior-Layer Insulating Layer
60—Upper Layer Wiring

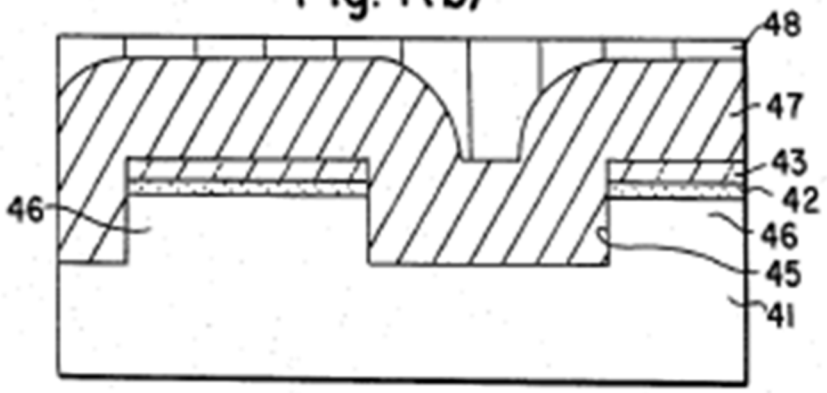
169. To see how the trench isolation in *Ogawa's* Fig. 5(c) is formed, reference is first made to *Ogawa's* Figs. 4(a), 4(b), and 4(c) which illustrate the formation of the raised trench isolation. First layers **42** and **43** are deposited:

Fig.4(a)



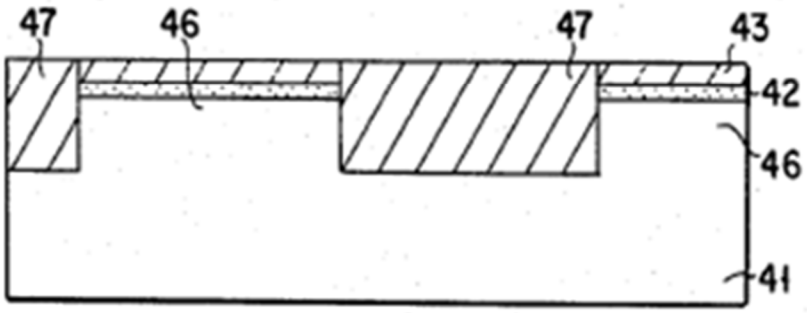
170. After formation of layers **42** and **43**, a trench (groove) is made through layers **42** and **43** (*Ogawa*, 6:9-14). $SiO_2$ layer **47** is then grown into the groove and entirely covers the top surface of the substrate **41** (*Ogawa*, 6:25-30) Fig. 4(b) below:

Fig.4(b)




171. Next, planarization leaves the wafer surface flat. Fig. 4(c) below:

Fig. 4(c)




172. Substrate **41** (renumbered as substrate 51) is then processed as in Figs. 5(a) - 5(c) shown below. As in *Noble*, gate electrode **55** does not extend above the isolation trench (now numbered as **52**). All that does extend onto the STI raised

trench is the conductive wiring layer **56**, which it is patterned/etched to leave a conductive wiring layer on the gate electrode, and a portion on the interconnection.

Fig.5(a)

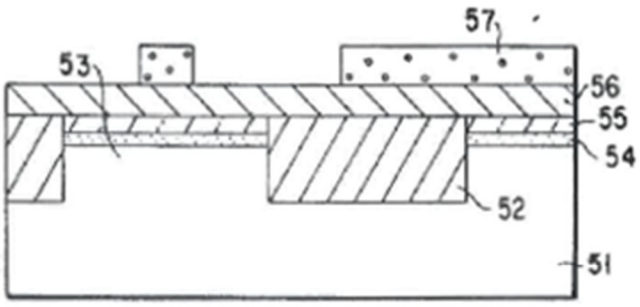



Fig.5(b)

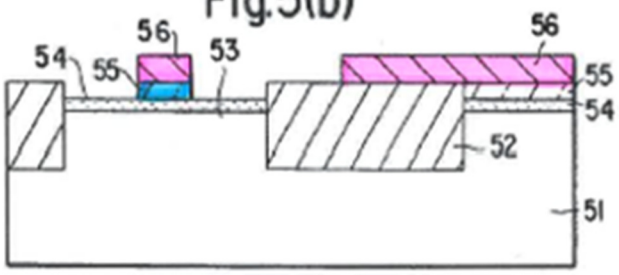



Fig.5(c)

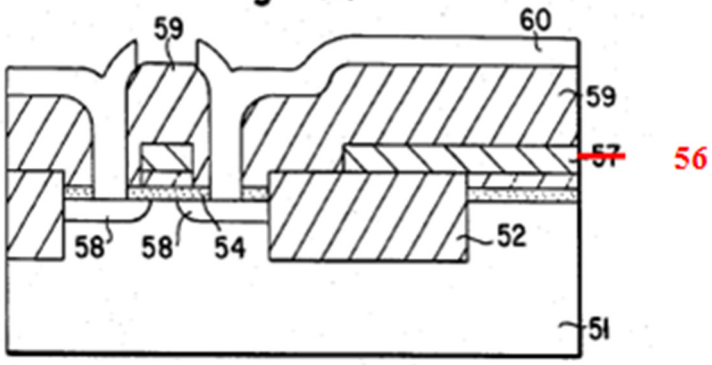



Exhibit 1010, 7:40-42 (Correcting typo in Figure 5(c); Element 57 should be 56).

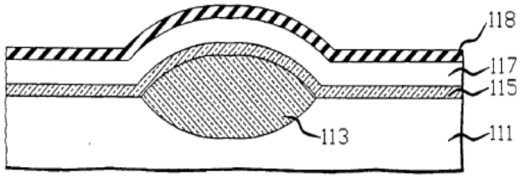
173. As a result, as seen in Fig. 5(b) and 5(c), raised trench isolation **52** does not have a gate electrode **55** on top of it, but instead has only conductive wiring **56** ("molybdenum silicide ($MoSi_2$) layer **56**") on top of it. No L-shaped sidewalls are associated with the conductive wiring.

174. There is no gate electrode on top of the raised trench isolation because the trench isolation was formed by inserting it through gate electrode layer **55**. Only the wiring layer **56** rests on the raised trench isolation and acts as an interconnection. (Layer **59** is an insulation layer).

**Overview Of Why The References Are Not Combinable**

175. For purposes of illustration, shown below, side-by-side, are the "beginnings" and "near beginnings" of the fabrication processes of both *Lee* (Fig. 11) and *Noble* (Fig. 9) respectively.[17]

FIG. 11



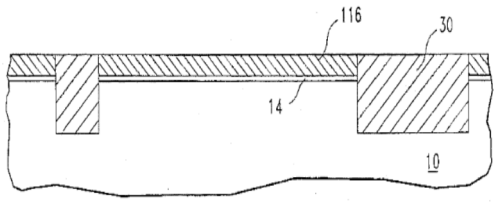




FIG. 9

176. *Lee* begins by first forming the LOCOS isolation **113** by oxidizing the surface of the substrate **111** to form the football shaped isolation. It then teaches

[17] *Lee* is shown, but *Lowrey* likewise forms its LOCOS isolation before layering.

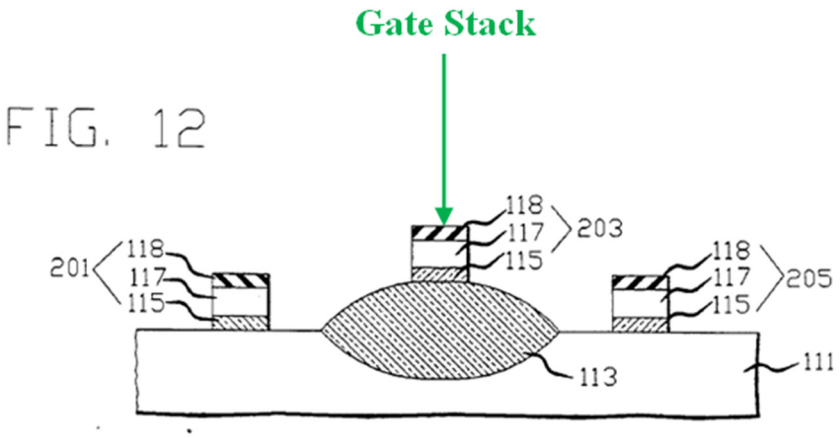
applying layers **115**, **117** and **118**. First isolation formation, followed by gate stack layering.

177. *Noble* follows just the opposite sequence. *Noble* first applies gate stack layers **14** and **116**, then forms an opening at a location through the layers, and then etches a groove (or trench) in substrate **10**. The groove is then filled with oxide material up to the level of layer **116**, after which excess material is removed in a planarizing process. First gate stack layering, then isolation formation.

178. In both cases, the layers form the gate electrodes, but because the layers in both patents serve different functions, the configurations of the resulting device structures will be considerably different. This difference in the early stages influences everything that follows. The question then becomes, in taking the trench isolation out of *Noble* and putting it into *Lee*, how and when this would be done, and most importantly, what would the final structure look like? Petitioner never addresses this.

179. Because layer **116** of *Noble*, which forms the gate electrode goes up to the edges of, but not over trench isolation **30**, the final structure of *Noble* cannot have a gate electrode over the trench isolation. Conversely, gate electrode layer **117** of *Lee* does go over its LOCOS isolation such that after etching, there will be a gate electrode on top of the LOCOS isolation – this is part of *Lee*'s invention.

180. Consequently, the final structures will differ substantially in that *Lee* will have a gate layer stack on its LOCOS isolation, while *Noble* will have no gate layer stack on its trench isolation. This difference is shown below.



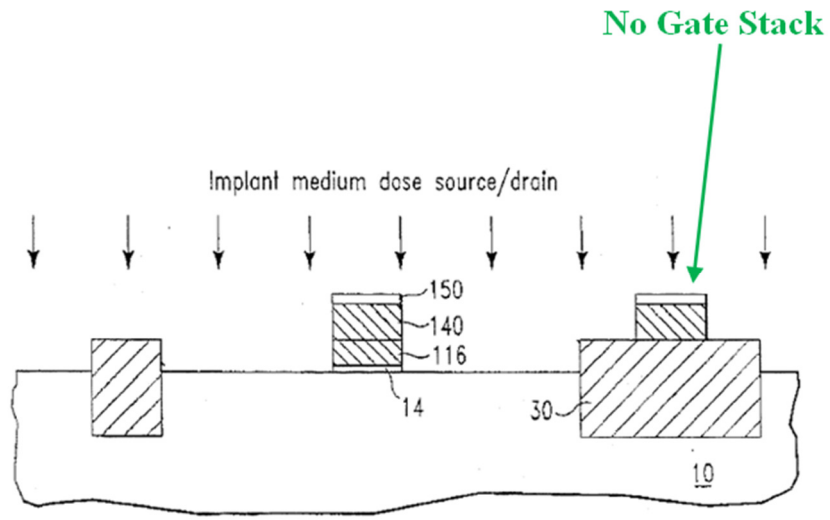




FIG. 11

181. The gate-or-no gate question is significant since the gate **117** of *Lee* is used to form the interconnect on top of what would somehow be a trench isolation, but this cannot be because the trench isolation of *Noble* was formed without a gate

electrode on top of it (as in *Lee*). To get a gate electrode on top of such a trench isolation would mean that a second gate electrode would have to be deposited on top of the previously-deposited first gate electrode. This would render the device inoperative.

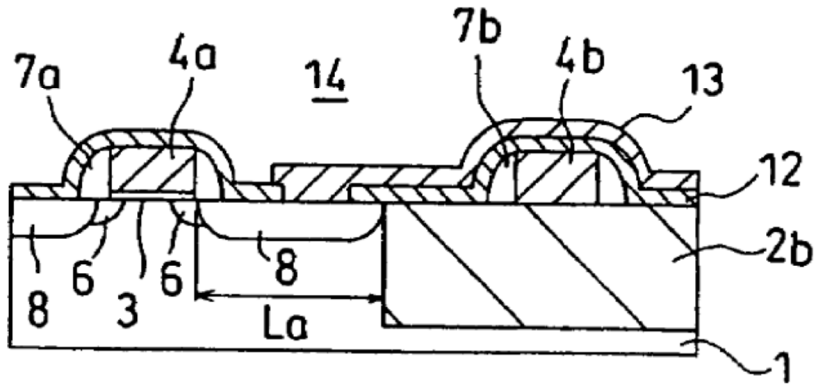
182. Conversely, if a trench isolation (not taught by *Noble*) is formed in *Lee* without previously-deposited layers on the substrate, and before layers **115**, **117** and **118** of *Lee* are applied, the resulting trench isolation would not be raised above the surface of the substrate. Such a trench is not taught by *Noble* (or *Ogawa*) and would be highly undesirable.[18] Accordingly, a POSITA considering any of the combinations proposed by Petitioner, would not proceed in this manner.

183. Petitioner cites to (prior art) Fig. 17 of the '174 patent numerous times (see '1246 Petition, pp. 1, 7, 10, 23, 31, 33-34, 36, 40, 43, 48, 57-58, 60, 63, 66; '1247 Petition, pp. 1, 7, 10, 22, 30, 33-35, 40, 42, 47, 55-56, 58-59). But other than selectively pointing to specific features of it, no attempt is ever made to explain how any of these features would be incorporated into or integrated with the devices of the other *Lee*, *Lowrey*, *Noble*, or *Ogawa.* Figure 17 shows a level trench isolation, and Petitioner gives no explanation as to how it is to be made, or how its

[18] *Noble* gives a strong warning with respect to a level trench or recessed trench isolation, including the "wrap-around effect" and "Corner Parasitic Device".

teachings would be integrated into *Lee*, *Lowrey*, *Noble*, or *Ogawa*. Yet further, when forming the trench isolation so that it is not raised as in Fig. 17, the resulting device is missing multiple elements of claim 1 – including the first L-shaped sidewalls and the second L-shaped sidewalls (see Figure 17). Figure 17 is shown below:

FIG. 17
PRIOR ART




184. Petitioner also fails to point out that Fig. 17 is described by the '174 as prior art that suffered from alignment problem rendering it undesirable to a POSITA.

185. In sum, a POSITA would and could not have simply combined *Lee* or *Lowrey* with *Noble* or *Ogawa* to arrive at the claimed invention, and Petitioner never says how it would be done (neither by a pictorial nor narrative process flow description).

**Combination: *Lee* & *Noble***

The Initial Processing Sequence Of *Noble* Is Opposite From *Lee*

186. As explained earlier, *Lee* forms the LOCOS isolation field oxide ***before*** depositing the gate dielectric and gate conductor film. The first step of *Noble* is the deposition of the thin gate dielectric film **14** ("gate dielectric") and the gate conductor **116** ("gate conductor") on substrate **10**. It is only thereafter, that the raised shallow trench isolation (STI) **30** ("raised STI") is formed so as to define and surround the active area. The STI process concludes with a planarization step (*e.g.* CMP) that leaves the Si wafer (substrate **10**) surface planarized or flat as shown in *Noble's* Fig. 9, reproduced below:

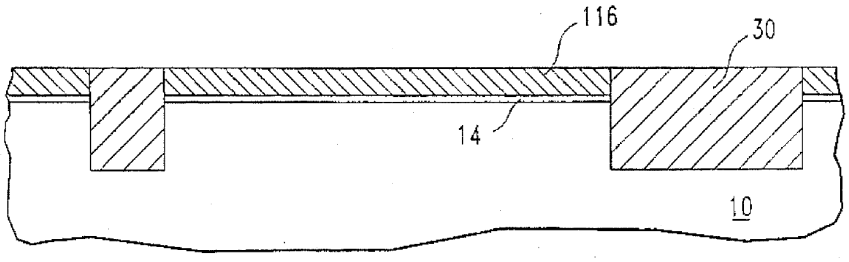



FIG. 9

187. In summary, as noted above, *Noble* forms the raised STI isolation feature only ***after*** depositing the gate dielectric film and gate conductor film.

188. *Noble* states:

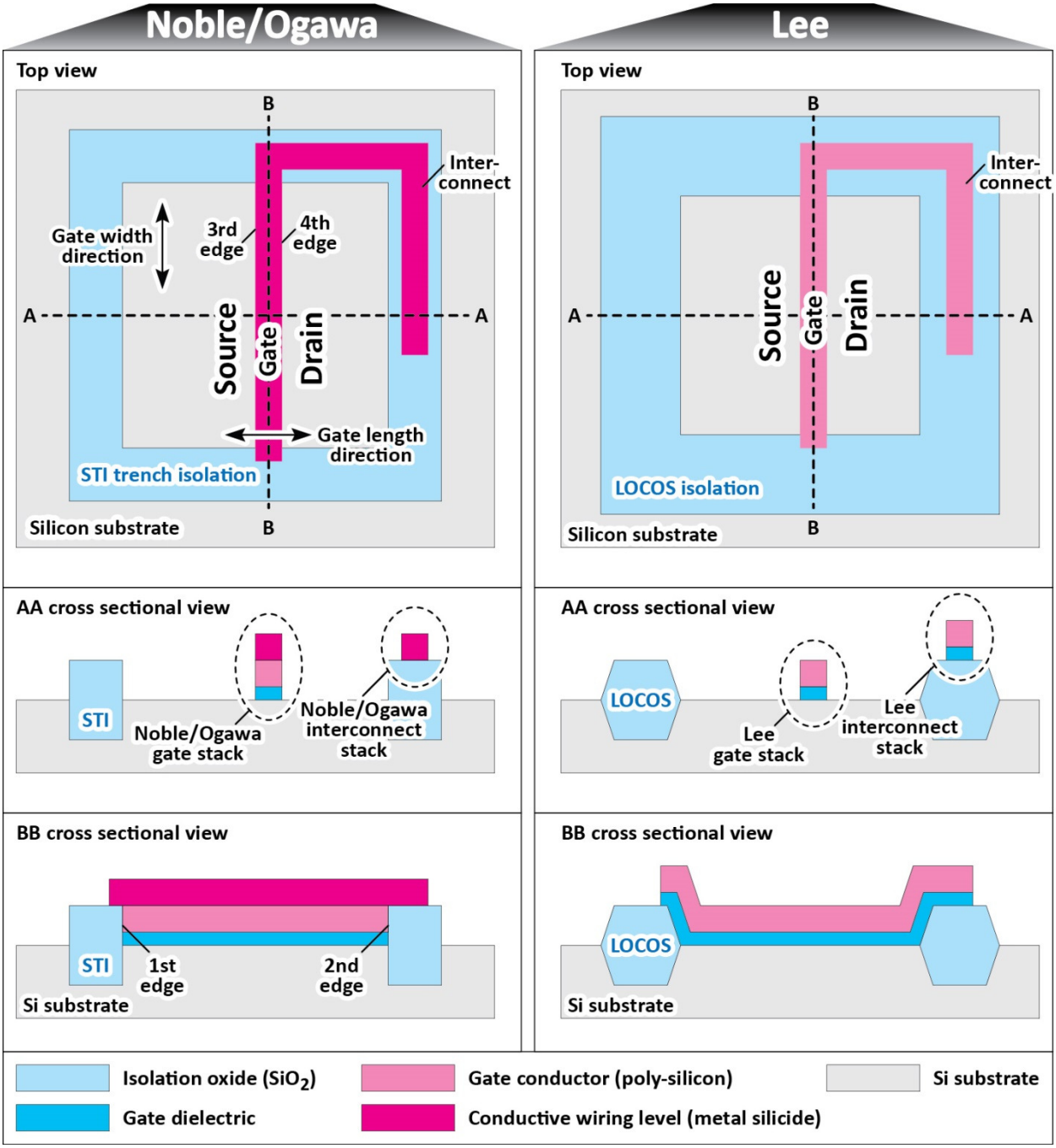
> These and other objects of the invention are accomplished by a semiconductor structure comprising a

transistor with a gate comprising an individual segment of gate conductor on thin dielectric. The gate conductor is substantially coextensive with the thin dielectric. The gate conductor has a top surface having opposed first and second edges and opposed third and fourth edges. Raised isolation bounds the first and second edges of the gate conductor. A source is self-aligned to the third edge and a drain is self-aligned to the fourth edge. A conductive wiring level is in contact with the top surface.

Another aspect of the invention provides a method of forming an FET comprising the steps of providing a substrate having a gate stack comprising a layer of gate dielectric and a layer of gate conductor, the gate stack having a top surface; removing first portions of the gate stack and etching a trench in the substrate thereby exposed for raised isolation; depositing insulator and planarizing to the top surface of the gate stack; removing second portions of the gate stack for source/drain regions and to expose sidewalls of the gate stack adjacent the source/drain regions.

Exhibit 1015, 2:47-3:3 (underscore added).

189. The above-quoted description is depicted below.




190. The above depiction shows the *Noble* and *Ogawa* structures on the left in contrast to the *Lee* structure on the right.

191. The gate conductor in *Noble* has 3rd and 4th edges that are aligned with the source and drain, respectively, as shown above ("A source diffusion is

self-aligned to the third edge and a drain diffusion is self-aligned to the fourth edge." Exhibit 1015, Abstract).

192. The gate conductor in *Noble* has 1st and 2nd edges that are bounded by the raised trench isolation, as shown above ("Raised isolation bounds the first and second edges of the gate conductor." Exhibit 1015, 2:53-54). As a consequence of the process, the two gate ends along the gate width direction ("first and second [gate] edges") are aligned with the raised STI; this is because the STI trench etching defines the end of the gate electrode (along the gate width direction).

193. In contrast, *Lee's* gate conductor cannot be bounded by the isolation structure (neither LOCOS nor STI) because the gate conductor is deposited subsequent to the isolation structure (i.e. there is no self-alignment between the gate electrode and the isolation structure) and also because the gate conductor has the additional purpose of serving as an interconnect conductor. This dual purpose of the gate conductor in *Lee* is different from *Noble* who has different structures for the gate conductor and the interconnect structure.

194. *Noble* additionally explains why this process sequence was chosen:

> It is another object of the present invention to prevent the gate conductor from wrapping around the trench corner. It is another object of this invention to avoid gate dielectric thinning

> adjacent the corner. It is another object of this invention to avoid sharpening of the corner.

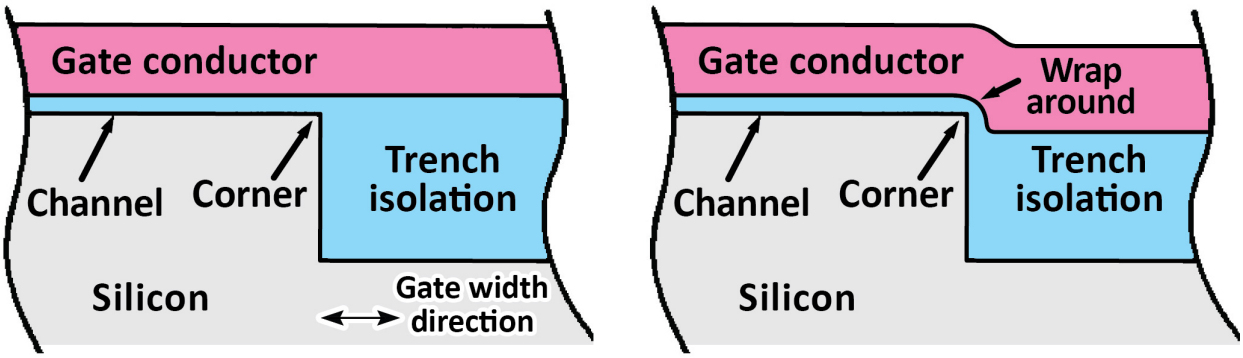
Exhibit 1015, 2:30-35 (underscore added).

195. That is, *Noble* specifically utilizes a process sequence contrary to that of *Lee* to attain the above-recited benefits. *Noble* explicitly cautions about deleterious effects that have plagued prior-art trench isolation structures:

> Parasitic leakage paths have been created by the proximity of a semiconductor device to an edge or corner of either type of trench. In one leakage mechanism [...] the parasitic leakage path results from an enhancement of the gate electric field near the trench corner [...] in a worst case scenario for corner field enhancement, the gate conductor wraps around the trench corner. This happens when the oxide fill in the isolation trench is recessed below the silicon surface [...] Thus, a parallel path for current conduction is formed [...] the corner device can even dominate [...] Furthermore, there exists concern that the enhanced electric fields due to field crowding at the corner impact dielectric integrity. [...] This corner leakage problem has commonly been controlled with an increased threshold tailor implant dose, but this can degrade device performance. Thus, alternate schemes for controlling the corner are needed.

(Exhibit 1015, 1:20-2:4, underscore added).

196. The corner at the edge of the trench isolation is illustrated in the left-hand-side figure below (adapted from Exhibit 2022):




(a) after Bryant, 1993, Exhibit 2022, page 413 (b) Gate-wrap-around problem

197. The gate-wrap-around problem occurs when the trench isolation is recessed with respect to the Si surface so that the gate conductor wraps around the Si corner as indicated in the right-hand-side figure above. The corner is a spatial non-uniformity that creates high electric fields and leakage current paths that are deleterious to device operation.

198. *Noble* points out problems that are associated with a trench isolation when the oxide surface is level or lower than the Si substrate surface. Several technical articles (Exhibit 2022, pgs. 412-413; Exhibit 2023, p. 1110; Exhibit 2024, pgs. 636-638; Exhibit 2025, p. 358C) point out the problems associated with level and recessed trench isolation including the gate wrap-around parasitic device and corner parasitic device. *Noble*'s and *Ogawa*'s transistor structure overcomes this problem by bounding the gate stack by the trench isolation thereby preventing the gate stack to "wrap around" the Si corner.

*Lee* And *Noble* Processes Are Not Compatible

199. Petitioner contends that it would have been trivial and obvious to a POSITA to follow the *Lee* process while substituting *Lee's* LOCOS isolation with *Noble's* trench isolation. To the contrary, a POSITA would not have been motivated to proceed in the manner asserted by Petitioner and in fact would have found Petitioner's *Lee-Noble* combination non-functional for the following reasons:

200. ***First***, it is not possible to follow *Lee's* process by simply substituting *Noble's* trench isolation for *Lee's* LOCOS isolation. *Lee* *starts* with LOCOS isolation formation *followed* by gate dielectric and gate conductor formation, while *Noble* *starts* with gate dielectric and gate conductor formation *followed* by trench formation. *Noble* specifically relies on the pre-existence of gate dielectric and gate conductor when forming the trench isolation. Therefore, *Lee's* subsequent deposition of gate dielectric and gate conductor could only be applied on top of *Noble's* pre-existing structure, thereby making the *Lee-Noble* combination devices inoperative.

201. ***Second***, it is not possible to simply start with *Noble's* trench isolation without first forming the gate dielectric and gate conductor because *Noble's* trench isolation formation relies on the availability of the gate dielectric and gate conductor. Thus, it would undermine the *Noble* process to go directly to trench

isolation formation, and leave out the initial formation of the gate dielectric and gate conductor. Accordingly, it would not be possible to simply substitute the trench isolation in *Noble* for the LOCOS isolation of *Lee*, as Petitioner contends.

202. ***Third***, assuming, *arguendo*, that Petitioner (without having disclosed the actual processing sequence it envisions) would follow *Lee* for the deposition of the gate dielectric and gate conductor *instead* of the gate dielectric and gate conductor of *Noble*, in such case the interconnect could not be deposited simultaneously with the gate conductor as *Lee* contemplates. That is, *Noble*, due to its raised trench isolation, exhibits a distinct height difference between the gate stack (consisting of elements **14**, **116**, **140**, and **150**) and interconnect stack (consisting of elements **140** and **150**). This is apparent in *Noble* Fig. 11, shown below (with colors, annotation, and numerals **140** and **150** of interconnect added for clarity):

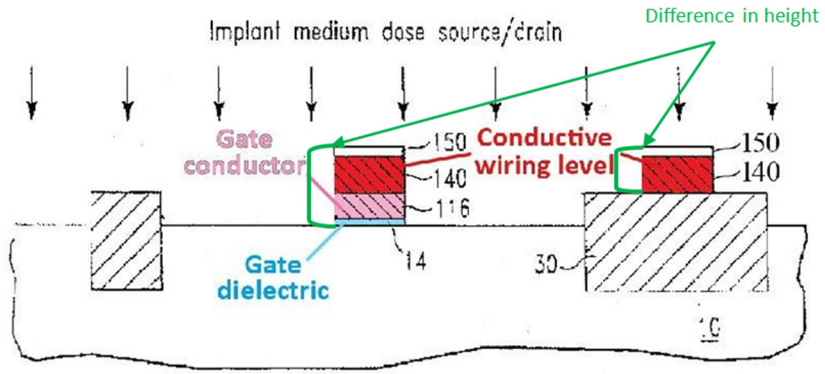
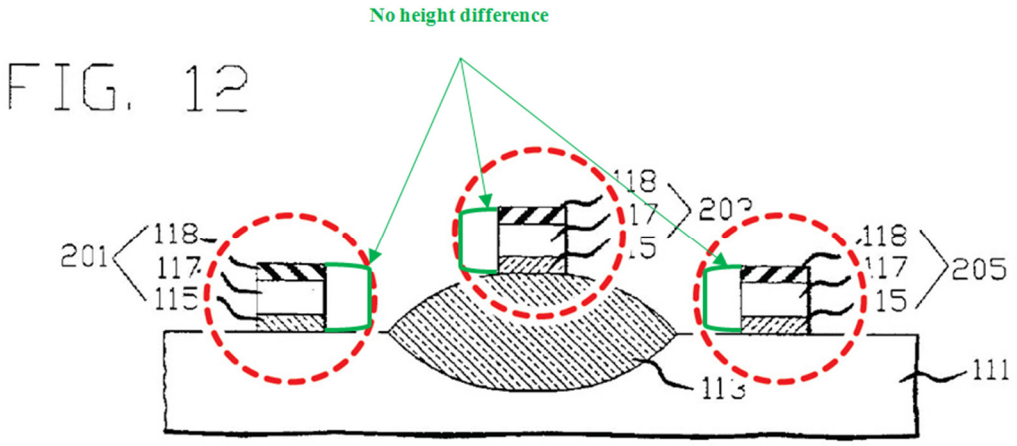



FIG. 11

203. In stark contrast to *Noble*, *Lee* employs the same element for the gate conductor and interconnect conductor. This is apparent from *Lee* Fig. 12, reproduced below, showing "gates **201**" and "runner **203**" consisting of the identical layer sequence **115**, **117**, **118** (*see* red dashed circles).




204. *Lee* teaches the use of the same structural features for elements serving different purposes. Thus, *Lee* explicitly teaches the use of the same elements for the gate conductor and interconnect conductor, while *Noble* employs different conductors. Using different structures contradicts the teaching of *Lee*. Using different conductors for the gate and the interconnection, which is the key starting point of *Noble* as a precedent to forming the raised trench isolation, would result in a gate stack and interconnect stack having different heights because the interconnect would lack the gate conductor and gate oxide, which is present in the gate stack.

205. To somehow re-fabricate *Lee* in the *Noble* trench fabrication sequence would completely destroy the *Lee* structure and undermine its design because *Lee's* design would lose its hallmark feature of using the same layer stack for the gate and interconnect stack as indicated by the red dashed circles in the image above.

206. Adding to the inconsistency, due to the dielectric cap **118** ("protective nitride layer **118**") on top of the gate stacks of *Lee* Fig. 15, there would be no way that a conductive wiring layer could electrically contact the gate electrode because the dielectric cap will insulate and thus prevent such contact. The resulting device would become non-functional for its intended purpose.

207. According to *Lee*:

> The presence of a protective nitride layer **118** together with nitride layer **121** which flanks runner **203** prevents electrical contact between patterned layer **170** and the conductive polysilicon heart **117'** of runner **203**.

Exhibit 1002, 7:44-47

208. There is no need for a separate interconnect stack in *Lee*: The gate conductive layer **117** serves as gate stack *and* also as the interconnect stack (gate runner) thereby elegantly connecting gates with interconnects.

209. Petitioner points to Figure 11 of *Noble* to make the un-depicted *Lee/Noble* combination, as showing "a conductive wiring level **140** which extends over STI **30** to interconnect transistors or cells, as shown in Fig. 11." '1246

Petition, p. 42. The interconnection shown in Figure 11 is between the STI interconnect **30** and the gate electrode. Petitioner presumably would suggest that a conductive wiring layer such as that of *Noble* could be added to connect the (proposed) *Noble* trench isolation to *Lee*'s gate stacks **201** and **205**.

210. However, *Lee*'s gate stacks **201** and **205** (Fig. 13) are totally encapsulated such that there would be no use in extending a conductive wiring layer to them as shown in *Noble*.

211. I conclude that Petitioner has chosen not to explain how the features of the devices would be combined and implemented so as to avoid illustrating the inoperability of the reference combination.

212. A POSITA would have understood the above reasoning and thus would not have been motivated to combine the two very different disclosures of *Lee* and *Noble*. Because the fabrication processes are incompatible, and because the combination would be non-functional, there would be no reason to combine the references. Moreover, to the extent that Dr. Banerjee is suggesting that a POSITA would have combined certain portions of *Lee* with certain portions of *Noble* in such a manner that it would have rendered the claims of the '174 patent obvious, he seems to be conveniently picking and choosing elements from each reference in order to obtain a device that has all of the elements of the claims of the '174 patent, and not focusing on how a POSITA actually would have combined the references,

if at all (and as stated above, they would not). A POSITA would understand that a Si IC device must be fabricated by a functioning and reasoned sequence of fabrication steps. In the absence of such sequence (Petitioner provided neither pictorial nor narrative process sequence), a Si IC device having specific elements becomes meaningless.

213. It appears that Kuo-Hua Lee and Chih-Yuan Lu, two of the inventors on *Lee*, were aware that trench isolation could be used in semiconductor devices to separate active areas before the filing of *Lee*. In particular, U.S. Patent No. 4,952,524 (Exhibit 2021) identifies Lee and Yu as inventors on a patent that is directed toward the use of trench isolation in a semiconductor device. For example, the '524 patent describes the disclosed invention as relating to "integrated circuits with trenches for inter-device isolation." Exhibit 2021, 1:8-9. If it were obvious to substitute the LOCOS isolation in the process of *Lee* with trench isolation, as Dr. Banerjee suggests, then I would expect that the inventors of *Lee*—who were aware of trench isolation—to have identified trench isolation as an alternative to LOCOS isolation in *Lee*. They did not do that.

214. Moreover, *Lee* in view of *Noble* would not disclose "a gate insulating film formed over the active area." As noted above, the claimed "active area" is surrounded by trench isolation in each of the claims. However, *Lee* does not disclose the claimed active area, and as discussed above, it would not have been

obvious to combine *Lee* and *Noble* to obtain an active area surrounded by trench isolation. Because "the active area" of claim 1 would not be disclosed by *Lee* in view of *Noble*, they cannot disclose "a gate insulating film formed over the active area."

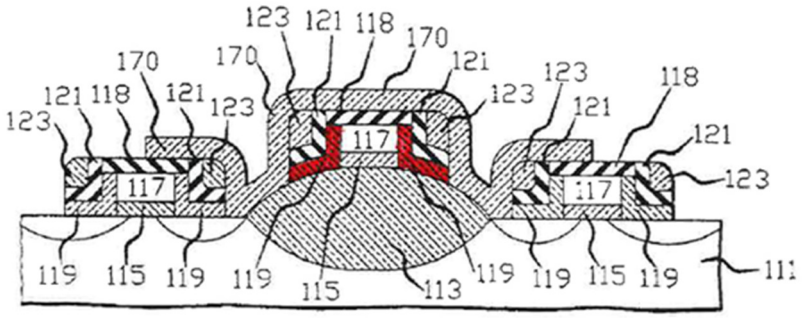
No L-Shaped Second Sidewalls

215. Entirely apart from the "first" L-shaped sidewalls in *Lee* on the gate electrodes over the active area are, what the '174 patent refers to as "second" L-shaped sidewalls – the sidewalls formed over the side surfaces of the interconnection on top of the trench isolation. Exhibit 1001, Claim 1.

216. *Lee's* layers **115**, **117**, and **118** are "typically formed during initial steps of semiconductor fabrication." Exhibit 1002, 6:53-56. *Lee's* "L-shaped" sidewalls are formed by anisotropically etching layers **119**, **121**, and **123** shown in Fig. 13. Exhibit 1002, 7:13-16.

217. What Petitioner has chosen to characterize as "second L-shaped sidewalls in *Lee*" are shown below:

FIG. 15




218. These "second" L-shaped sidewalls on the LOCOS isolation serve a different purpose than the sidewalls on each of the gate electrodes over the active areas. Bearing in mind that *Lee* has a gate conductor **117**, which *Lee* refers to as a "gate runner," in both the active areas as well as on the LOCOS isolation, *Lee* explains the special purpose of these "second" sidewalls:

219. At least one spacer together with the dielectric layer serves to insulate the runner so that local conductive interconnection may extend over the runner without risk of shorting.

220. Thus, the purpose of the "second" sidewalls on the LOCOS is to insulate the gate conductor **117** sitting on top of the LOCOS so that a local interconnection (*Lee*'s "overlying conductive layer **170**") can go over the gate runner without shorting.

221. However, if the trench isolation of *Noble* is substituted for the LOCOS isolation of *Lee*, the necessary result is that there will be no gate runner on

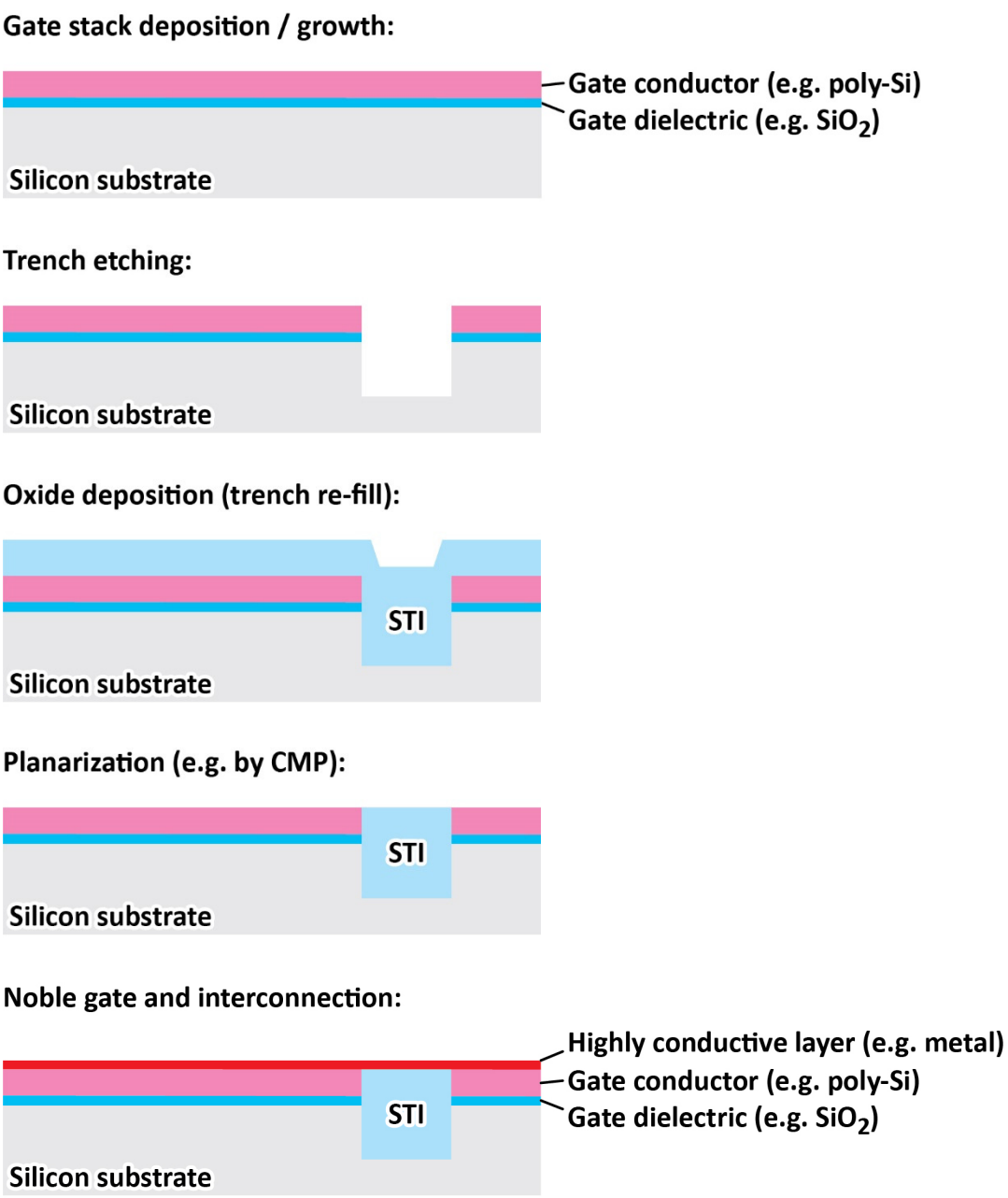
the trench isolation, and therefore no need for the second sidewalls on top of the trench isolation – there is no shorting to be prevented.[19]

222. A POSITA would not have formed the "second" L-shaped sidewalls on the trench isolation of *Noble* without the benefit of hindsight. *Lee* has nothing to do with the interconnection **140** on top of the trench isolation of *Noble*.

223. Without guidance, it is hard to know exactly how Petitioner believes a combination of the *Lee* and *Noble* devices would look. However, just looking at the trench fabrication process of *Noble*, the following steps would take place:

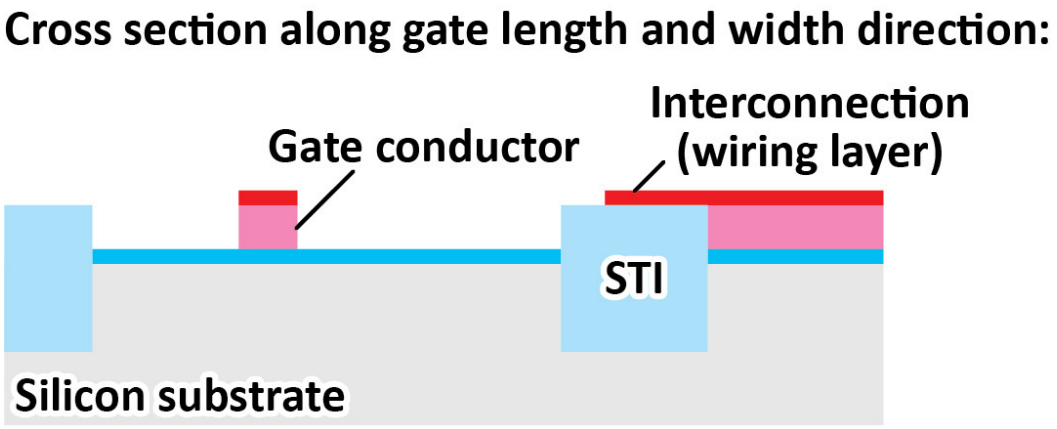
[19] *Noble* and *Ogawa* do not contemplate a local interconnect that crosses over the interconnect.

**Process sequence forming the *Noble* gate stack and interconnect:**



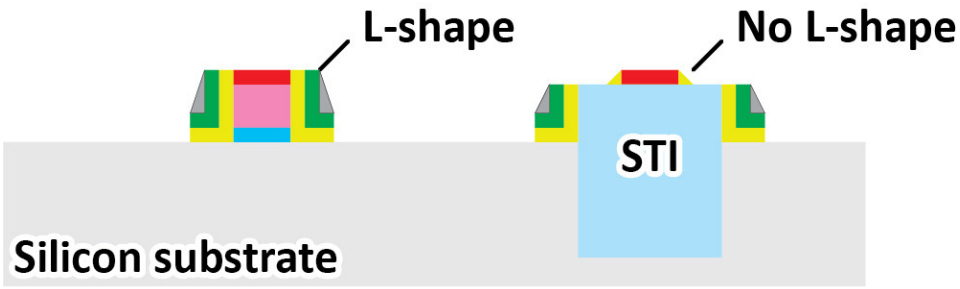

224. As shown above, *Noble* teaches first applying a gate dielectric and gate conductor, then forming the trench isolation, after which a highly conductive

layer is applied. The highly conductive layer extends across the gate stack and the interconnection.

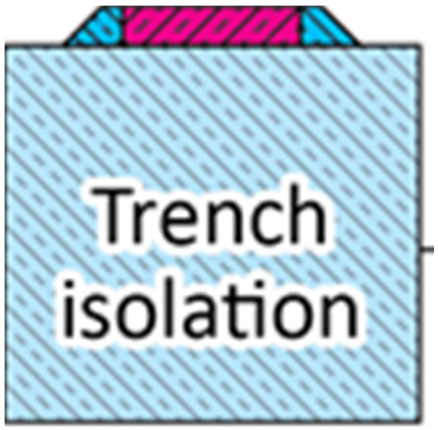



225. After photolithographic patterning and etching, due to the height of the STI, it is seen that the lower two layers (blue-colored gate insulator and pink-colored gate conductor) are part of the gate stack, but they are not part of the interconnection on the STI (and are otherwise etched away).

226. Then, as per *Lee*, the sidewall layers are provided and then anisotropically etched to provide the structure below:



227. After anisotropic etching of the modified *Lee* device, it is evident that the interconnection (red) is of such low height relative to the gate stack[20] that there is little opportunity for forming an L-shaped sidewall at the interconnect. Instead, what forms is likely not much more than a nub or blob having no distinguishable shape. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall). The following image is how the wiring layer on top of the interconnection of Figure 14 of *Lee* might look like if a trench isolation as per *Noble* were substituted for the LOCOS isolation of *Lee*.




228. Claim 1 of the '174 patent requires a "second" L-shaped sidewall. Patent Owner has provided the Board with the Court's definition, namely

[20] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.

"sidewalls that substantially resemble a capital 'L' or its mirror image." Once Petitioner has proposed that the trench isolation of *Noble* be substituted for the LOCOS isolation of *Lee*, it was incumbent upon Petitioner to then proceed to illustrate what such a substitution would look like, including what the interconnect on top of the trench – and its sidewalls would look like.

229. Importing the trench isolation from *Noble* or *Ogawa* into *Lee* has not only the effect of contradicting the design philosophies of *Lee* and both *Noble* and *Ogawa*, but it also results in a structure intended by none of the three patents and which does not meet the terms of claim 1.

Summary

230. Petitioner has failed to provide the actual process sequence it is contemplating. To properly establish obviousness, disclosure of the fabrication sequence is necessary. If Petitioner would have provided an actual process sequence (either pictorial or narrative) based on *Lee* as modified by the trench isolation of *Noble*, it would have become apparent to the POSITA that Petitioner's contemplated process would either (i) not be able to modify *Lee* by incorporating *Noble's* trench isolation without significantly deviating from the teachings of *Lee* and *Noble* in manner never suggested by Petitioner, or (ii) result in a non-functioning device.

231. Stated differently, in the cases of both *Lee* and *Noble*, the formation of the LOCOS isolation and trench isolation is intrinsically bound to the formation of the gate stack and interconnect stack, and in each case the respective formation process dictates the respective structures and formation process sequence. Petitioner's proposed substitution would have required considering only the two different *abstract* isolation structures (LOCOS isolation vs. trench isolation) while disregarding the gate layer stack and interconnect layer stack, something a POSITA would not have done. A POSITA would understand that a Si IC device must be fabricated by a functioning and reasoned sequence of fabrication steps. In the absence of such sequence (Petitioner provided neither pictorial nor narrative process sequence), a Si IC device having specific elements becomes meaningless.

232. Petitioner was required to address the consequences of altering the sequence of gate/interconnect/isolation formation and Petitioner has not done so. The gate and interconnect conductors associated with both types of isolation are integral to the isolation fabrication module, gate fabrication module, and interconnect fabrication module and dismantling these modules would unfavorably disrupt the entire fabrication sequence.

233. Yet further, as noted above, combining *Lee* with *Noble* results in *Lee*'s dielectric caps ("protective nitride layer **118**") completely insulating the gate stack from any conductive wiring layer that *Noble* requires ("a conductive wiring

level **140**"). If the wiring layer is eliminated, there would be no sidewalls at all on top of the trench.

*Lee-Noble* Rejection Fails On Further Grounds

Silicidation[21] Of *Lee*

234. If *Noble's* trench isolation were to be substituted for the LOCOS isolation of *Lee*, Petitioner simply never explains how the silicidation of *Lee* could be accomplished in Figs. 14 and 15 given the difference in how the structures of *Lee* and *Noble* are formed.

235. In connection with *Lee*'s Figure 14 (a precursor to Figure 15), *Lee* discloses that silicide layers can be formed "over source/drain regions **300**, **301**, and **302**." Exhibit 1002, 7:22-25. But *Lee* does not illustrate where source/drain regions **300**, **301** and **302** are located in Figure 14 (or any other figure). Moreover, in Figure 14, four source/drain regions are shown, which do not align with the three regions **300**, **301** and **302** identified in the text.

[21] The word "silicidation" describes the process of forming a metal silicide. "Salicidation" means "Self-Aligned Silicidation" and thus is a specific variant of the silicidation process. At the present time, silicidation and salicidation are common processes in the Si IC industry. In this report, I use the term "silicidation" throughout.

236. In my opinion, it would not make sense to use silicide in three out of the four source/drain regions. Instead, for example, because the exposed portions of the source/drain regions closest to the LOCOS isolation in Figure 14 are much smaller than the exposed portions of the source/drain region farthest from the LOCOS isolation in Figure 14, the inventors of *Lee* might have meant that only those two regions are intended to have silicide on them. In other words, a silicide layer would be formed on one side of the gate electrode, and not on both sides of the gate electrode, while the claim requires silicide layers formed on both sides of the L-shaped sidewalls. This is because the smaller exposed area of the source/drain region in Figure 14 of ~~*Noble*~~ Lee would have a smaller contact region than the other source/drain regions, and so the lower resistance that would be provided by the silicide would be required for the source/drain regions closer to the isolation region than would be required for the other source/drain regions. Accordingly, *Lee* does not clearly disclose silicide layers formed on the sides of the first L-shaped sidewalls.

237. As noted, Petitioner relies upon the configuration of Fig. 15 throughout, but points to Fig. 9 ('1246 Petition, p. 39) to teach the claimed silicide layers, which are not shown in Fig. 15. To reinforce their reliance on Fig. 15, they point to small red dots added to Fig. 15, ('1246 Petition, p. 40), because the specification states "[I]n the structure of Figure 14, silicidation of source/drain

regions 'may also be performed in a manner analogous to that depicted in FIG. 9.'" But if *Noble's* trench isolation were to be substituted for the LOCOS isolation of *Lee*, Petitioner simply never explains how this silicidation could be accomplished given the difference in how the structures of *Lee* and *Noble* are formed.

Conclusions regarding the *Lee-Noble* combination

238. Petitioner has consciously avoided recitation of a fabrication processing sequence (pictorial or narrative) based on *Lee* and *Noble*.

239. The fundamental premise of Petitioner is to just drop in the trench isolation of *Noble* instead of using the LOCOS isolation of *Lee*. There would have been no motivation for the POSITA to make such a substitution unless a complete re-design and re-engineering of the combined fabrication processes would be done first to demonstrate the feasibility of such combination. Petitioner has not proposed or provided such re-design and re-engineering of a fabrication process.

240. Indeed, following *Lee* and then using, instead of *Lee*'s LOCOS isolation, *Noble*'s trench isolation would result in a non-functioning IC device.

241. Given the fabrication processes in *Lee* and *Noble*, a POSITA would conclude that the disclosed processing sequences cannot be combined in a way which would suggest or obviate the '174 patent as disclosed in its claims.

242. A POSITA would have needed to develop a novel undisclosed process that would substantially deviate from both *Noble* and *Lee*. Such novel process (i)

would not have been obvious to a POSITA and (ii) has not been described by Petitioner.

**Petitioner Fails To Meet Its Burden To Establish That *Lee* In Combination With *Noble* Renders At Least Claim 1 Unpatentable**

243. Claim 1 specifically recites a "trench isolation" which is absent from *Lee*. A POSITA would have no motivation to substitute the raised trench isolation of *Noble* for the LOCOS isolation of *Lee* for the following reasons:

i. Formation of the *Noble* trench isolation requires the prior deposition of two layers **14** and **116** which would be incompatible with the process contemplated by *Lee*.

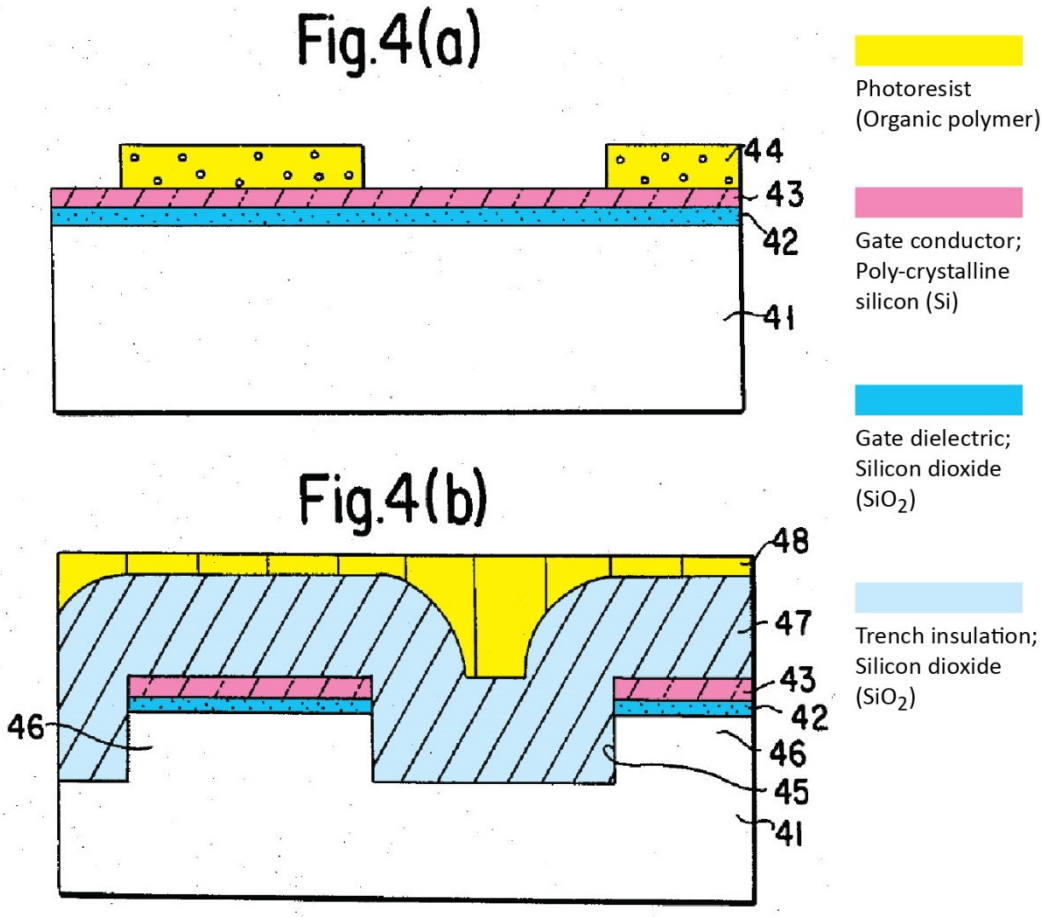
ii. No L-shaped sidewalls on the interconnect: Given the absence of a single gate conductor and gate runner in a combination of *Lee* and *Noble*, the result would be a device that has substantially different structures for the gate stack and interconnect stack that was not shown to have second L-shaped sidewalls.

iii. No first silicide layer. As pointed out above, the disclosure of silicide layers in *Lee* is absent or, at best, ambiguous.

**Combination: *Lee* & *Ogawa***

Initial Processing Sequence of *Ogawa* Is Opposite From *Lee*

244. As explained earlier, *Lee* forms the LOCOS isolation ***before*** depositing the gate dielectric and gate conductor film. In contrast, *Ogawa* discloses a different sequence of the initial processing steps of an Si IC fabrication sequence. The initial steps are shown in *Ogawa*'s Figure 4(a) and (b) reproduced below in a colorized version.



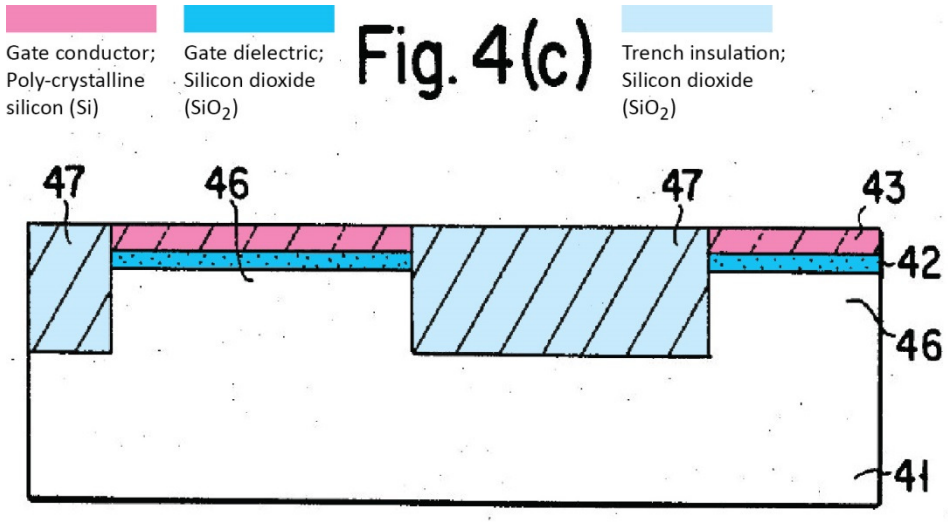

245. The first step, shown in Figure 4(a), is the deposition of the thin gate dielectric film **42** ("silicon dioxide layer") and the gate conductor **43**

("polycrystalline silicon (Si) layer"). *Ogawa*, 5:57-61. It is only thereafter, that the trench isolation (buried insulating layer **47**) is formed. *Ogawa* states:

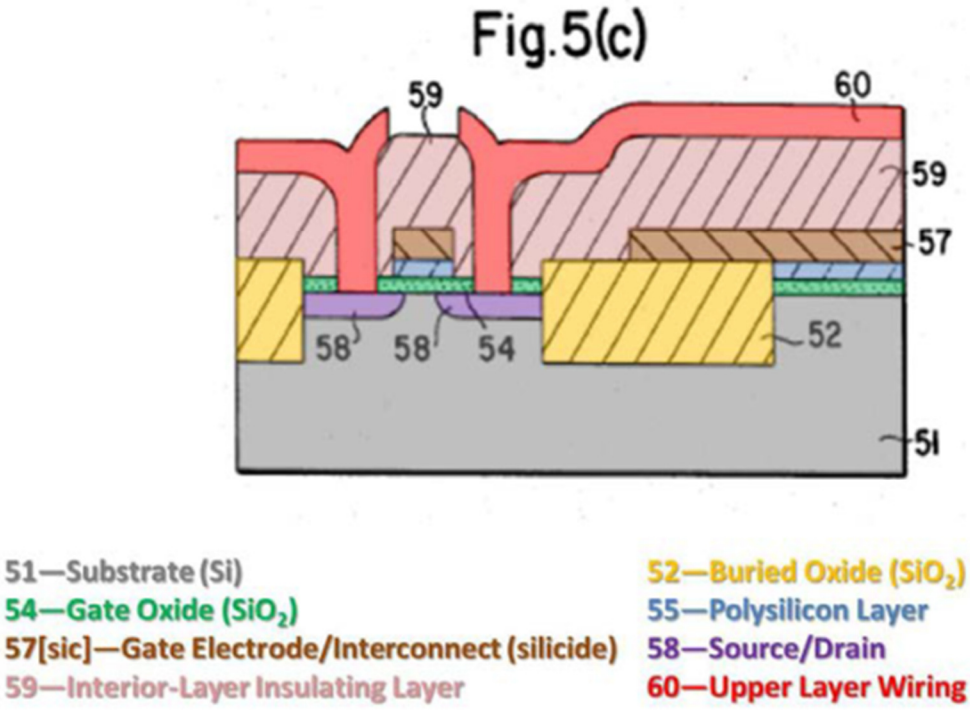
> A photoresist layer **44** is produced on the surface of polycrystalline silicon (Si) layer **43**, before a patterning process is applied to the photoresist layer **44** for the purpose of producing grooves along the area corresponding to the area in which a buried insulating layer is produced.

Exhibit 1010, 6:9-14 (emphasis added).

246. The STI process concludes with a planarization step that supposedly leaves the wafer surface planarized or flat as shown in *Ogawa* Fig. 4(c), reproduced below in a colorized version:




247. Petitioner relies upon *Ogawa's* Fig. 5(c), which shows a raised trench isolation **52**. ('1246 Petition, p. 21). Petitioner never addresses how trench isolation **52** is formed.




248. Substrate **41** (renumbered as **51**), including trench isolation **47** (renumbered as **52**), is then illustrated in Figs. 5(a) – 5(c) shown below:

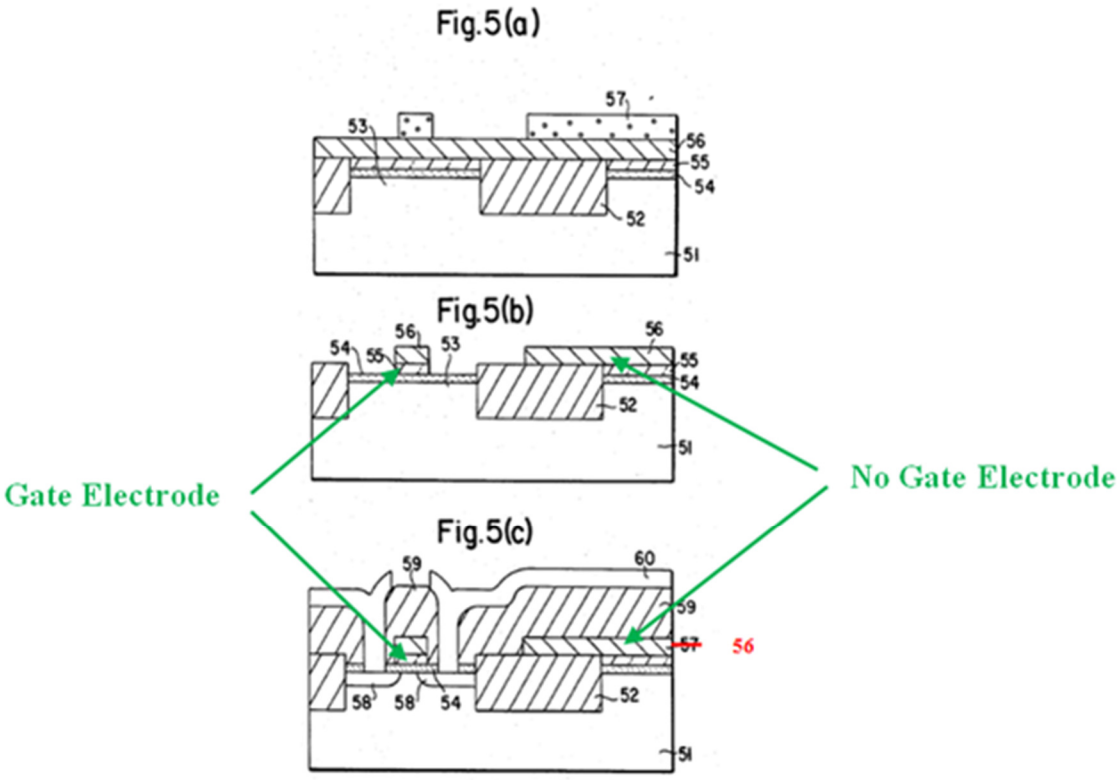



Exhibit 1010, 7:40-42.[22]

249. As a result, as seen in Fig. 5(b) and (c) raised trench isolation **52** does not have gate electrode **55** extend on top of it, but instead has only wiring layer **56** on top of it. No L-shaped sidewalls are disclosed.

250. There is no gate electrode on top of the raised trench isolation because the trench isolation was formed by depositing it through gate electrode layer

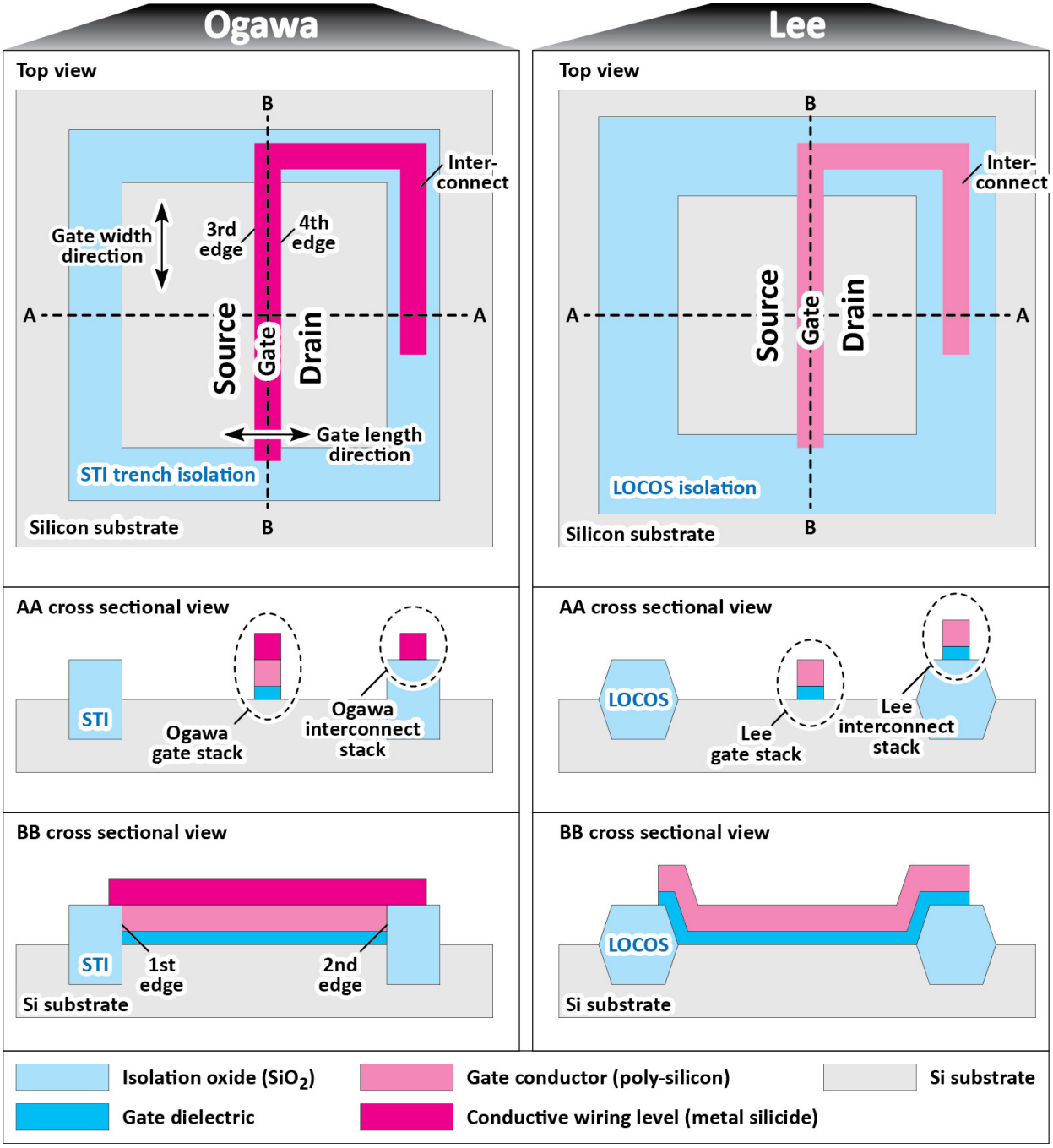
[22] Correcting typo in Fig. 5(c). Element **57** should be **56**.

**55**. Only the conductive wiring layer **56** rests on the raised trench isolation and acts as the interconnection to adjacent gate stacks.[23]

251. The method used by *Ogawa* in 1982 (the *Ogawa* filing date) to planarize the trench isolation is an unreliable etching technique, which a POSITA would have dismissed by the time of the invention.

252. In summary, *Ogawa* forms the raised STI isolation feature only ***after*** depositing the gate dielectric film and gate conductor film. In this respect, both secondary references, *Ogawa* and *Noble* are alike. The illustration below shows the *Noble/Ogawa* structure on the left and contrasts it to the *Lee* structure on the right.

[23] Layers **59** and **60** are not relevant to this discussion. Although *Ogawa* does not call **56** "conductive wiring level" (but instead "molybdenum silicide ($MoSi_2$) layer **56**"), **56** is called "conductive wiring level" in the present Declaration for convenience.

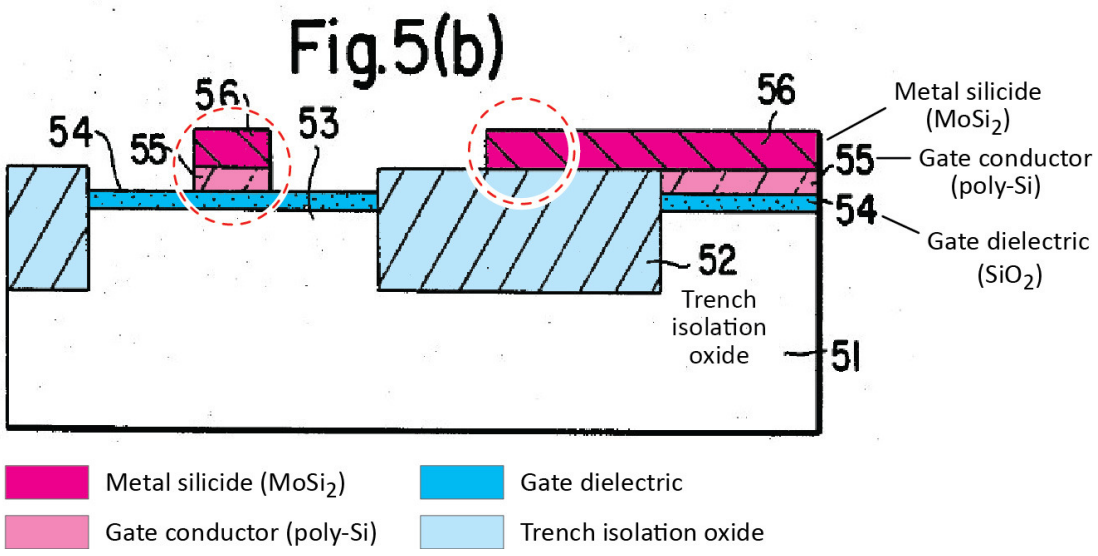



253. *Ogawa's* gate conductor is, along the gate length direction, aligned with the source and drain, as shown in the illustration above. *Ogawa's* gate conductor, along the gate width direction, is bound by the raised trench isolation,

as shown in the illustration above; this is because the trench etching ("grooves") defines the end of the gate electrode (along the gate width direction).

254. In contrast, *Lee's* gate conductor cannot be bound by the isolation structure (neither LOCOS nor STI) because the gate conductor is deposited subsequent to the isolation structure (i.e. there is no self-alignment between the gate electrode and the isolation structure) and also because the gate conductor has the additional purpose of serving as an interconnect conductor.

255. This dual purpose of the gate conductor in *Lee* is different from *Ogawa* who has different structural elements for the gate conductor and the interconnect structure as shown by the red dashed circles in the figure below (Exhibit 1010, Figure 5(b)).



256. The trench formation process of *Ogawa* involves a trench isolation **52**, which is necessarily surrounded by layers **54** and **55**. There are no L-shaped spacers.

257. There is no gate electrode on top of the trench isolation **52** because of the way that the trench is formed, such that if this technique for trench isolation formation were used, there would be no gate electrode on top of the trench isolation, that is, the interconnection stack and gate stack would be different.

258. With the gate stack not being used for the interconnect stack, and given the different heights of the gate stack and interconnect stack, there is no way of knowing whether an L-shaped sidewall on the interconnection would form as claimed. The petition fails to address this issue.

259. Yet further, in the event the trench isolation of *Ogawa* were somehow substituted for the LOCOS isolation of *Lee*, the conductive wiring layer **56** of *Ogawa* could not function to contact the gate electrode's conductors of *Lee* because the dielectric caps **118** of *Lee* on top of the gate stacks would insulate against any such contact.

260. I find it very noteworthy that the claim limitation, "an interconnection formed on the trench isolation," has received virtually no attention in either the '1246 Petition (pp. 78-79) or the corresponding Banerjee Declaration (¶220).

*Lee* And *Ogawa* Processes Are Not Compatible

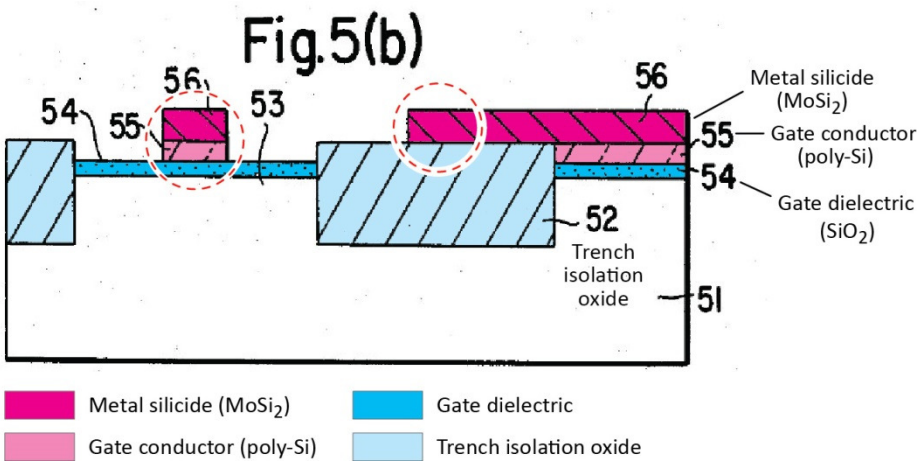
261. ***First***, it is not possible to perform *Lee*'s process by simply substituting *Ogawa*'s trench isolation for *Lee*'s LOCOS isolation. *Lee* starts with LOCOS formation followed by gate dielectric and gate conductor formation, while *Ogawa* starts with gate dielectric and gate conductor formation followed by trench formation.

262. *Ogawa* relies on the availability of gate dielectric and gate conductor when forming the trench isolation. Therefore, *Lee*'s subsequent deposition of gate dielectric and gate conductor could only be applied on top of *Ogawa*'s pre-existing structure, thereby making the *Lee-Ogawa* combination devices non-functional.

263. ***Second***, it is not possible to simply start with *Ogawa*'s trench isolation without first forming the gate dielectric and gate conductor because *Ogawa*'s trench isolation formation relies on the availability of the gate dielectric and gate conductor. Thus, it would completely undermine the *Ogawa* process to proceed directly to trench formation, and leave out the initial formation of the gate dielectric and gate conductor. Accordingly, it would not be possible to simply substitute trench isolation for LOCOS isolation, as Petitioner contends.

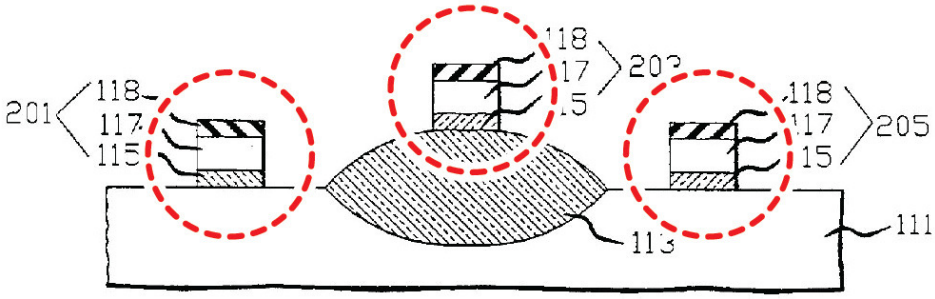
264. ***Third***, assuming, *arguendo*, that Petitioner (without having disclosed the actual processing sequence it envisions) would follow *Lee* for the deposition of the gate dielectric and gate conductor instead of the gate dielectric and gate

conductor of *Ogawa*, in such case the interconnect could not be deposited simultaneously with the gate conductor as *Lee* contemplates. As a consequence, *Ogawa*, due to its raised trench isolation, exhibits a distinct height difference between the gate (consisting of element **54**, **55** and **56**) and interconnect (consisting of elements **56**). This is apparent in *Ogawa* Fig. 5(b), shown below, where the gate and interconnect are marked with red-colored dashed circles (colors and annotation added for clarity).




265. In stark contrast to *Ogawa*, *Lee* employs the same element for the gate conductor and interconnect conductor. This is apparent from *Lee*'s Fig. 12, reproduced below, showing "gates **201**" and "runner **203**" consisting of the identical layer sequence **115**, **117**, **118** (see red-colored dashed circles). *Lee's* process teaches the use of the same structural features for elements serving different purposes.

FIG. 12




266. Adding to the inconsistency, due to the dielectric cap **118** ("protective nitride layer **118**") on top of the gate stacks of *Lee* Fig. 15, there would be no way that a conductive wiring layer could electrically contact the gate electrode because the dielectric cap will insulate and thus prevent such contact. The resulting device would become non-functional for its intended purpose.

267. *Lee* explicitly teaches the use of the same elements for the gate conductor and interconnect conductor, while *Ogawa* employs different conductors. Using different structures for these elements disregards the teachings of *Lee*. In addition, the use of different conductors, which is a key starting point of *Ogawa* as a precedent to forming the trench isolation, would result in a gate stack and interconnect stack having different heights.

268. To fabricate "L-shaped" features on structures having different heights would require re-modification of *Lee's* sidewall fabrication module if the "L-shaped" sidewall claim limitations of the claim are to be met. It is unclear how

Petitioner contemplates fabrication of the same feature using such disparate elements.[24]

269. Finally, *Lee* would completely lose its identity because it would lose the hallmark feature of using the same layer stack for different elements, i.e. the gate and interconnect (as indicated by the red dashed circles in the image above).

270. Stated differently, in the cases of both *Lee* and *Ogawa*, the formation of the LOCOS isolation and trench isolation is intrinsically bound to the formation of the gate stack and interconnect stack, and in each case the respective formation process dictates the respective structures and formation process sequence.

271. As a strictly technical matter, it was incumbent upon Petitioner to go beyond considering only the two different isolation structures (LOCOS isolation vs. trench isolation) in the abstract and to also take into account the gate layer stack and interconnect layer stack – this Petitioner did not do.

272. Indeed, Petitioner was fundamentally required to address the consequences of altering the sequence of gate/interconnect/isolation formation.

[24] The '174 patent has a *single* height (vertical length) of the gate stack and interconnect stack. *Ogawa* has *two* different heights (vertical length) of the gate stack and interconnect stack, thereby making an L-shaped sidewall formation process more complicated and less predictable in the case of *Ogawa*.

The gate and interconnect conductors associated with both types of isolation are integral to the isolation fabrication module, gate fabrication module, and interconnect fabrication module and dismantling these modules would unfavorably disrupt the entire fabrication sequence.

273. If the trench isolation of *Ogawa* is substituted for the LOCOS isolation of *Lee*, the necessary result is that there will be no gate runner on the trench isolation, and therefore no need for the second sidewalls on top of the trench isolation – there is no shorting to be prevented. [25]

274. A POSITA would not have thought to form the "second" L-shaped sidewalls on the trench isolation of *Ogawa* without the benefit of hindsight. *Lee* has nothing to do with the interconnection 56 on top of the trench isolation of *Ogawa*.

No L-Shaped Second Sidewalls

275. Without guidance, it is hard to know exactly how Petitioner believes a combination of the *Lee* and *Ogawa* devices would look. However, just looking at the trench fabrication process of *Ogawa* the following steps would take place:

[25] *Noble* and *Ogawa* do not contemplate a local interconnect that crosses over the interconnect.

**Process sequence forming the *Ogawa* gate stack and interconnect:**

---

**Gate stack deposition / growth:**


**Silicon substrate**

**Trench etching:**

**Silicon substrate**

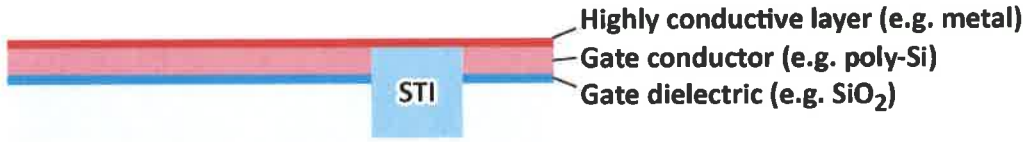
**Oxide deposition (trench re-fill):**


**Silicon substrate**

**Planarization ~~(e.g. by CMP):~~**


**Silicon substrate**

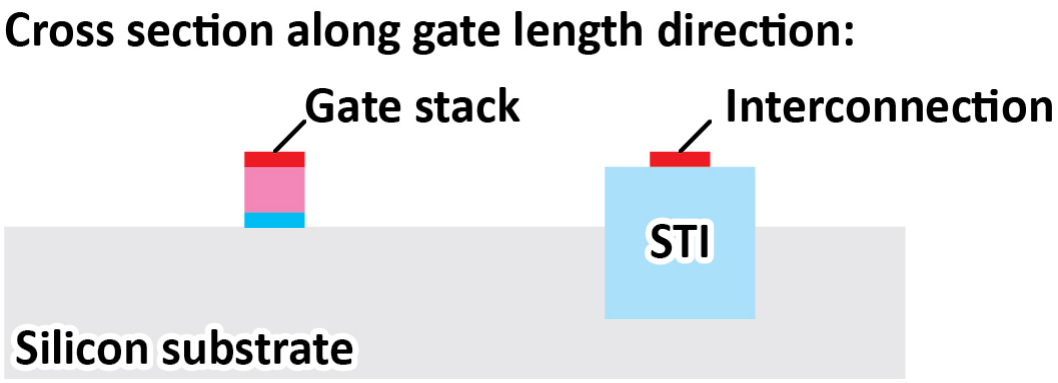
**Noble gate and interconnection:**




**Silicon substrate**

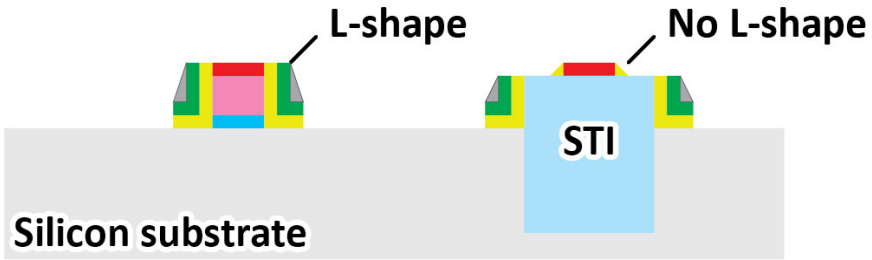
276. As shown above, *Ogawa* teaches first applying a gate dielectric and gate conductor, followed by trench isolation formation, after which a highly conductive layer is applied. Only the highly conductive layer (shown in red)

extends across the gate stack and onto the trench isolation thereby forming the interconnection.




277. After etching, due to the height of the STI, it is seen that the lower two layers (blue-colored gate dielectric and pink-colored gate conductor) are part of the gate stack, but they do not extend above the STI and are otherwise patterned and etched away.

278. Then, as per *Lee,* dual or triple sidewall layers are applied, and then these layers are anisotropically etched to provide the structure below:

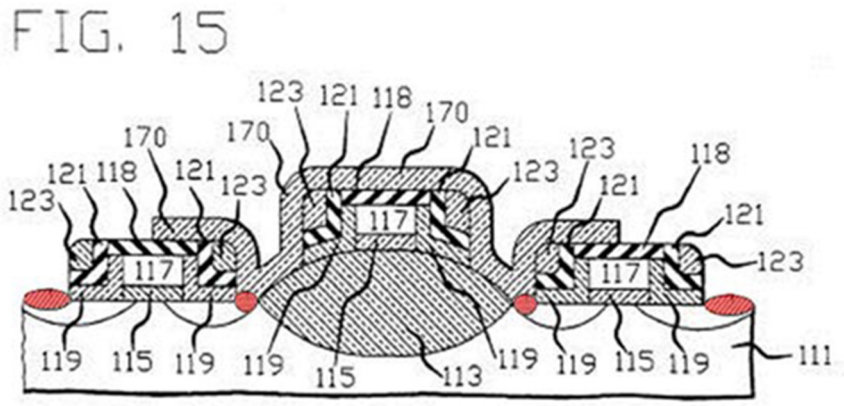


279. After anisotropic etching of the modified *Lee* device, it is seen that the interconnection is of such low height relative to the gate stack[26] that there is little opportunity for something resembling an L-shape to form and what forms is likely not much more than a nub or blob having no distinguishable shape. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall). This is how Figure 14 of *Lee* might look if a trench as per *Ogawa* were substituted for the LOCOS of *Lee*:


Petitioner's Proposed Silicide "Layer" Is Portrayed To Be A Small Diameter Circular Element (Wire or Cylinder) That Runs Along the Gate Width Of The Device

[26] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.

280. Petitioner's Annotated Fig. 15 (reproduced below) shows red-colored pinpoint spots of indeterminate size or dimension. These spots would run in a line (wire or cylinder) along the width of the device.[27] A line is not a "layer". It is simply impossible to know what the dimensions of the proposed element would be. But even had they been shown, there would be no way to know whether the line would be a "layer.":




281. Thus, *Lee* as it *might* be modified by *Noble* fails to teach "first silicide layers formed on regions located on the sides of the L-shaped sidewalls within the active area."

[27] In the image below, the left-right direction is called the "gate length" direction. The direction orthogonal to the page plane is called the "gate width" direction.

282. Likewise, *Lee* as it *might* be modified by *Ogawa* fails to teach "first silicide layers formed on regions located on the sides of the L-shaped sidewalls within the active area."

Conclusions Regarding The *Lee-Ogawa* Combination

283. The fundamental premise of Petitioner is to just substitute *Ogawa*'s trench isolation for *Lee*'s LOCOS isolation. Such substitution without substantial undescribed re-engineering is not possible because it would render the Si IC device non-functional and the fabrication process unworkable. Furthermore, the method used by *Ogawa* to planarize the trench isolation was an unreliable etching technique.

284. Petitioner has consciously avoided detailing a fabrication processing sequence based on *Lee* and *Ogawa*. Given the fabrication processes in *Lee* and *Ogawa*, a POSITA would conclude that the disclosed processing sequences cannot be combined in a way which would suggest or obviate the claims of the '174 patent as disclosed in its claims.

285. A POSITA would need to develop a novel undisclosed process that would substantially deviate from *Ogawa* and *Lee*. Such novel undisclosed process (i) would not have been obvious to a POSITA and (ii) has not been described by Petitioner. As such, there would have been no motivation to modify *Lee* by substituting trench isolation of *Ogawa* for the LOCOS isolation of *Lee*.

**Petitioner Fails To Meet Its Burden To Establish That *Lee* In Combination With *Ogawa* Renders At Least Claim 1 Unpatentable**

286. Claim 1 specifically recites a "trench isolation" which is absent from *Lee*. A POSITA would have no motivation to substitute the raised trench isolation of *Ogawa* for the LOCOS isolation of *Lee* for the following reasons:

i. The gate stack and interconnection stack contemplated by *Lee* would be non-functional once the trench isolation has been formed according to *Ogawa*.

ii. Formation of the *Ogawa* trench requires the prior deposition of two layers **54** and **55,** which would be incompatible with the layers (gate dielectric and gate conductor) contemplated in *Lee*.

iii. Given the absence of a gate conductor (runner) in a combination of *Lee* and *Ogawa* would result in a device that has not been shown to have second L-shaped sidewalls.

iv. No L-shaped sidewalls on the interconnect: Given the absence of a combined single gate conductor and gate runner in a combination of *Lee* and *Ogawa*, the result would be a device that has substantially different structures for the gate stack and interconnect stack that was not shown to have second L-shaped sidewalls.

v. No first silicide layer. As pointed out above, the disclosure of silicide layers in *Lee* is absent or, at best, ambiguous.

Conclusions Regarding Claim 1

287. To the extent that Petitioner is picking and choosing elements from *Noble/Ogawa* for inclusion in *Lee*, the combination is pure hindsight.

288. *Lee* is not combinable with *Noble/Ogawa* because these references form their isolation element relative to the gate layer stack in opposite sequences which cannot be adapted to one another. If combined in some way, however, it has not been shown how the transplanted trench isolation with its accompanying surrounding gate layer stack would impact the remaining *Lee* structure.

289. The trench of *Noble/Ogawa* is formed such that only a conductive wiring layer forms the interconnect on top of the trench isolation. But a conductive wiring layer **140** extending from the top of such a trench isolation in *Lee* to an adjacent gate stack, as *Noble/Ogawa* proposes, would serve no purpose, and render the device useless since such a wiring layer would not be able to electrically contact *Lee*'s encapsulated gate stack.

290. Finally, the result of such a combination would result in an interconnection which has not been shown to substantially resemble a capital "L" or the mirror image thereof.

Dependent Claims

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 2 And 6 Obvious

291. Claims 2 and 6 are patentable for the reasons stated in connection with claim 1. Additionally, it is noted that *Ogawa* doesn't address second L-shaped sidewalls at all, whereas *Noble*'s "second" sidewalls are not L-shaped and are not made of silicon nitride.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 3 And 15 Obvious

292. Claim 3 recites a first protection oxide film between the gate electrode and the first L-shaped sidewalls. Claim 15 recites that the first protection layer is a CVD oxide film. *Lee* has silicon dioxide in between the gate electrode and the first L-shaped sidewalls in Fig. 15; however, if a trench isolation were to be formed in *Lee* as per *Noble* or *Ogawa*, there is no way of knowing whether the resulting second sidewalls (on the trench isolation) would be L-shaped or what they would be made of. Without knowing what the combined structure would actually look like, there is no way of knowing whether there would be a protective oxide formed between the gate electrode and the second L-shaped sidewalls and Petitioner has not shown that it would.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Either Claim 5 And 16 Obvious

293. *Lee* in combination with *Noble/Ogawa* would not render claim 5 obvious because *Lee* in combination with *Noble/Ogawa* would not teach "source/drain regions formed on both sides of the gate electrode within the active area, wherein the first silicide layers are formed on the source/drain regions."

294. The only embodiment of *Lee* that shows a silicide layer formed on regions located on the sides of the gate electrode within an active area is the embodiment shown in Figures 9 and 10. However, that embodiment does not include an interconnection, as is required by claim 1. On the other hand, the only embodiment of *Lee* that includes an interconnection is the embodiment shown in Figure 15, but that embodiment does not include silicide layers located on the sides of the gate electrode. The spots (circles) shown by Petitioner are not layers but lines (cylinders) or wires, which extend along the LOCOS isolation. A line (cylinder) of undefined dimension is not a "layer".

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 7, 17, And 18 Obvious

295. Claim 7 recites that second protection oxide films formed between the interconnection and the second L-shaped sidewalls. Claims 17 and 18 depend from claim 7. Once again, there would not be an interconnection having second L-shaped sidewalls, such that there would not be second protection oxide films

formed between the interconnection and the second L-shaped sidewalls if *Lee* is combined with *Noble* or *Ogawa*.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 9 Obvious

296. *Lee* in combination with *Noble/Ogawa* would not render claim 9 obvious because *Lee* in combination with *Noble/Ogawa* would not teach a device wherein "the trench isolation has an upper surface higher than the surface of the active area."

297. According to Claim 1, the "first silicide layers are formed on regions [...] within the active area." *Noble* shows silicide layers next to a raised trench, but these layers are at the level of the upper surface of the trench isolation – the upper surface of the trench isolation is, therefore, not higher than the surface of the active area.

298. *Noble* explains that the raised source/drain region shown in Figure 13 is advantageous because it results in reduced leakage and low resistance. Exhibit 1015, 6:26-29. Thus, if a POSITA were to implement *Noble*'s STI in *Lee* (and they would not, as discussed above), the POSITA would also use the raised source/drain regions disclosed in *Noble*, and thus, would have the heightened active area (under the understanding of "active area" that would be necessary for the silicide layers in *Noble* to be formed within the active area). Thus, the trench isolation would not have an upper surface higher than the surface of the active area.

299. To the extent that the Board relies on the prior art as teaching a level trench to be combined with *Lee*, claim 9 clearly distinguishes in claiming a raised trench.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 10 Obvious

300. *Lee* in combination with *Noble/Ogawa* would not render claim 10 obvious because *Lee* in combination with *Noble/Ogawa* would not teach "a lower portion of the interconnection provided on the upper surface of the trench isolation is located higher than the surface of the active area."

301. *Lee* does not disclose trench isolation, and it would not have been obvious to use the shallow trench isolation of *Noble* in the *Lee* device.

302. Petitioner never asserts how and where the trench isolation of *Noble* will be inserted into *Lee*, it is thus impossible to know what the relative heights of the various components would be.

303. In addition, to the extent that *Noble*'s active area extends to the top of the silicide layers on the raised source/drain regions (as is necessarily the case to argue invalidity of claim 1), then the surface of the active area and the lower portion of the interconnection are at the same height, contrary to the requirement of claim 10. *Noble* explains that the raised source/drain region shown in Fig. 13 is advantageous because it results in reduced leakage and low resistance. Exhibit

1015, 6:26-29. Thus, if a POSITA were to implement *Noble*'s STI in *Lee* (and they would not, as discussed above), the POSITA would also use the raised source/drain regions disclosed in *Noble*, and thus, would have the heightened active area (under the understanding of "active area" that would be necessary for the silicide layers in *Noble* to be formed within the active area). Thus, the bottom of the interconnection (on the trench isolation) would not be higher than the surface of the active area.

304. To the extent that the Board relies on the prior art as teaching a level trench to be combined with *Lee*, claim 10 clearly distinguishes in claiming a raised trench.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 11 and 12 Obvious

305. Petitioner points to *Lee* as teaching an interconnector formed of the same material as the gate electrode, but fails to take into account what the structure of the device would be if the trench isolations of *Noble* and *Ogawa* were substituted.

306. *Lee* in combination with *Noble/Ogawa* would not render claims 11 and 12 obvious because *Lee* in combination with *Noble/Ogawa* would not teach "the interconnection is composed of the same material as the gate electrode" or that "the gate electrode and the interconnection have at least a polysilicon film".

307. *Lee* teaches forming the LOCOS isolation before layering the gate electrode. When forming the raised STI in *Noble/Ogawa*, *Noble/Ogawa* requires that the material for the gate electrode be deposited before the STI is formed, using the gate electrode as a rim (upper edge) to determine when to stop planarizing the wafer. Exhibit 1010, 6:16-22, 7:31-49; Exhibit 1015, 5:55-57. Since the gate electrode is formed before the STI, the gate electrode cannot be formed on the STI. Instead, another deposition used to form conductive wiring level **140** (*Noble*) **56** (*Ogawa*) on top of both the gate electrode and the STI (this is performed to form the interconnection). Exhibit 1015, 5:57-66; Exhibit 1010, 7:49-56. The wiring layer **140** is formed of metal or a metal silicide or heavily doped poly-silicon. Metals such as tungsten, molybdenum, titanium, or aluminum are suitable. Exhibit 1015, 5:61-65. The wiring layer **56** of *Ogawa* is molybdenum silicide. Exhibit 1010, 7:49-56. Thus, if a POSITA were to use the STI of *Noble* or *Ogawa* in the device of *Lee* (and they would not), the conductive wiring layers of *Noble* and *Ogawa* would not be "composed of the same material" and not have "at least a polysilicon film".

308. Petitioner points to *Lee* as teaching this feature, but fails to address whether this feature would still be present if *Lee* is combined with *Noble* and *Ogawa*.

*Lee* In Combination With *Noble/Ogawa* Would Not Render Claim 14 Obvious

309. *Lee* in combination with *Noble/Ogawa* would not render claim 14 obvious because *Lee* in combination with *Noble/Ogawa* would not teach "the first and second L-shaped sidewalls are made of the same insulating film." Neither *Noble* nor *Ogawa* discloses L-shaped sidewalls, since the sidewalls of *Noble* include a single structure shaped like a quarter circle (or ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. Exhibit 1015, Figs. 12-13. That is to say, *Noble* does not disclose a sidewall that is substantially shaped like a capital letter "L" or its mirror image. *Ogawa* teaches no sidewalls at all.

310. Given that the combined device would not have the gate conductor on top of the trench isolation, it would be unclear if there would be second L-shaped sidewalls in *Lee*.

311. Finally, if there were any second sidewalls at all on top of the trench isolation of *Lee* (combined device), they would be certainly different from the first L-shaped sidewalls.

Summary Of Argument

*Lee* and *Noble/Ogawa*

312. As a matter of law Petitioner has not met its burden of establishing invalidity by explaining how the prior art would be combined to arrive at the claimed invention, as well as providing a definite resulting structure which meets the claim language.

313. *Lee* discloses a device which has LOCOS isolation, and not trench isolation. Petitioner had the burden of establishing how, when in the fabrication process, and where, the trench isolation of *Noble/Ogawa* would be substituted for *Lee*'s LOCOS isolation. Petitioner has not done so.

314. The fabrication process sequence of the LOCOS isolation of *Lee* is opposite to the fabrication processes of the trench isolation of *Noble/Ogawa* with respect to the sequence of the gate layer stack and isolation feature (LOCOS and trench isolation). The opposite isolation fabrication process sequence will directly impact subsequent fabrication steps and ultimately the final device structure.

315. Petitioner had the burden of establishing what the final structure of the interconnection (including second sidewalls) on top of the trench isolation will be once it is substituted into *Lee* so that this combined structure can be compared to the interconnection of claim 1. Petitioner has not done so.

316. Specifically, assuming that the Petitioner intends the substitution of the *Noble/Ogawa* trench isolations into the device of *Lee* in place of the LOCOS isolation, Petitioner has not explained whether the structure on top of the

interconnection will contain a gate conductor (runner) and gate insulator, and if it does contain a gate runner what its purpose would be given the encapsulation of *Lee*'s gate stack.

317. Petitioner had the burden of establishing that in the final structure which they contemplate (but do not disclose) a POSITA would have found it obvious to provide second L-shaped sidewalls. They have not done so.

318. Specifically, if there is no gate conductor and no gate insulator on top of the isolation trench, Petitioner has not shown whether and how second L-shaped sidewalls would be formed on the conductive wiring interconnection on top of the trench isolation. Absent second L-shaped sidewalls of claim 1, as well as all the dependent claims, these claims are not invalid.

319. Petitioner has not shown whether and why a POSITA would extend a conductive wiring level as per *Noble* or *Ogawa* from the interconnection of *Lee* to the adjacent gate stack of *Lee* since the gate stack of *Lee* is fully insulated such that the conductive wiring level would be insulated from the gate electrode.

320. Petitioner has not shown the structure of the interconnection on top of the trench isolation Petitioner would insert into *Lee*, and as such it is not possible to know whether the material of the interconnection on top of the trench isolation would be the same as that of the gate electrode (claim 11). Accordingly, Petitioner has not met its burden and claim 11 is not invalid.

321. Petitioner has not shown the structure of the interconnection on top of the trench isolation which Petitioner would insert into *Lee*, and as such it is not possible to know whether both the material of the interconnection on top of the trench isolation as well as the gate conductor would have "at least a polysilicon film" (claim 12).

322. Petitioner has not shown the structure of the interconnection on top of the trench isolation Petitioner would insert into *Lee*, and as such it is not possible to know whether a second protection oxide film is formed between the interconnection and the second L-shaped sidewalls (claim 7) or whether those films would be L-shaped (claim 18). Petitioner has not shown the final device configuration, absent which each of these claims has not been shown to be invalid.

**Combination: *Lowrey* & *Noble***

*Lowrey* Is Not Compatible With Trench Isolation

323. *Lowrey* does not teach "a trench isolation surrounding an active area of a semiconductor substrate," since *Lowrey* teaches the use of LOCOS isolation for isolation instead of trench isolation. The patent discloses processing N-channel and P-channel devices separately in order to reduce the number of photomasking steps required to complete the CMOS circuitry. Exhibit 1017, Abstract.

324. The Petition asserts that *Lowrey* teaches every limitation of the challenged claims except trench isolation, and that a POSITA would have

understood that combing the teachings of *Lowrey* and *Noble* would have been a simple matter of replacing *Lowrey's* LOCOS with *Noble*'s STI ('1247 Petition, pp. 21-22). However, the Petition completely omits any explanation of how the proposed combination would actually be fabricated. Petitioner proposes to simply replace *Lowrey's* LOCOS isolation with *Noble's* trench isolation without explaining how it could be accomplished.

325. The proposed substitution of trench isolation for LOCOS isolation fails to give due consideration to the complexity, interconnectedness, and constraints of the Si IC fabrication process.

326. A LOCOS isolation is formed by using a very different process sequence than the process sequence used to form an STI (as I discussed in the section comparing LOCOS isolation with trench isolation). To produce an operative device, their very different respective fabrication processes must be merged, integrated, and made compatible with the fabrication processes preceding and succeeding the LOCOS / STI isolation process module.

327. Petitioner does not describe how and when *Noble's* STI can be substituted for *Lowrey's* LOCOS isolation. It would have been apparent to a POSITA at the time of invention that the incompatible process sequences for forming the STI disclosed in *Noble* (or *Ogawa*) would not have been substitutable for the LOCOS isolation of *Lowrey*, and as such, there would have been no

motivation for the POSITA to substitute the LOCOS isolation of *Lowrey* with the STI of *Noble* (or *Ogawa*).

328. Furthermore, even if such a combination were imagined (Petitioner never shows what it would actually look like):

i) *Lowrey*, upon which Petitioner relies to teach L-shaped sidewalls does not teach sidewalls which are L-shaped in its final device; and

ii) Substitution of trench isolation for the LOCOS isolation of *Lowrey* would result in a device having no gate conductor electrode or gate insulation on top of the raised trench isolation; there would be only a conductive wiring interconnection which has not been shown to be of sufficient height to result in the claimed "second L-shaped sidewalls."[28]

329. This incompatibility and unworkability negates any motivation to modify *Lowrey* by replacing its LOCOS isolation with *Noble's* STI. This lack of motivation renders *Lowrey* ineffective as the starting point of a validity challenge of the claims of the '174 patent.

[28] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.

The Initial Processing Sequence Of *Lowrey*

330. *Lowrey* Figures 1-4 illustrate the first, second and third photomasking steps. Exhibit 1017, 7:57-8:30. These photomasking steps are undertaken before LOCOS oxidation takes place. That is, the LOCOS isolation in *Lowrey* is not done at the beginning of the fabrication process (or "near the very beginning" of the process as Dr. Banerjee suggests in paragraph 93 of his declaration).[29] As a result of these initial steps, a non-planar surface (shown below) is formed on the substrate.

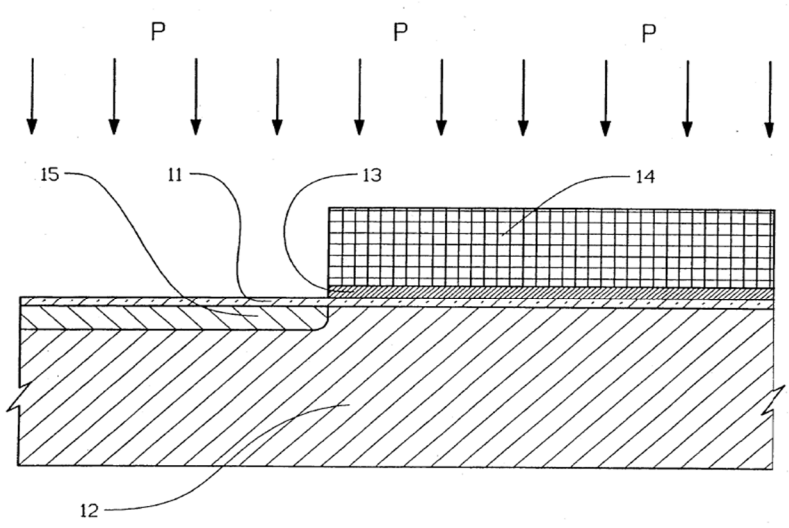



FIG. 1

331. In *Lowrey* Figure 1 (above),

> a first pad oxide layer **11** is grown on lightly-doped P-type silicon substrate **12**. A first silicon nitride layer **13** is then deposited on top of first pad oxide layer **11**, following which a

[29] However, the LOCOS isolation is applied before the gate electrode layer.

first photomask **14** is used to expose only those regions on substrate **12** that are to receive a first phosphorus implant. The phosphorus implant creates N-well regions **15**.

Exhibit 1017, 7:57-63.

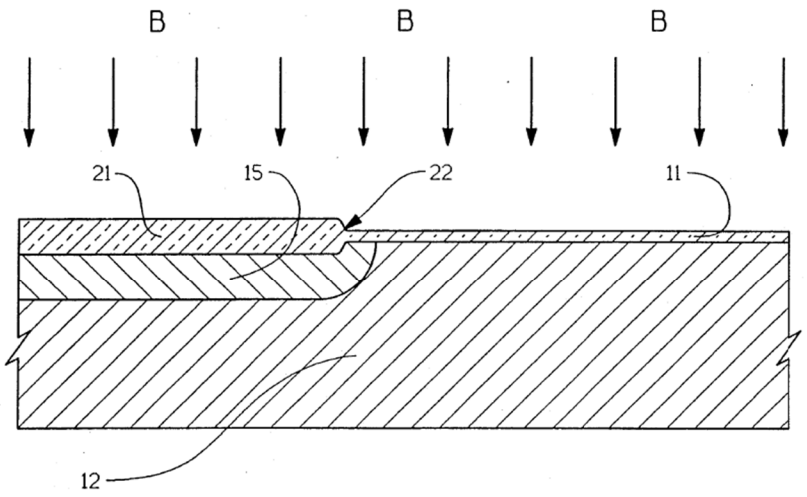



FIG. 2

332. In *Lowrey* Figure 2 (above),

following the stripping of the first photomask, a silicon dioxide masking layer **21** is grown in an oxidizing environment. The first pad oxide layer **11** acts to relieve stresses in the bird's beak region **22** at the edge of masking layer **21** during the oxide growth step.

Exhibit 1017, 7:65-8:2.

Following the stripping of first silicon nitride layer **13**, the wafer is exposed to an optional boron adjustment implant which optimizes the concentration of P-type charge carriers in the

substrate regions outside the N-well where N-channel devices will be created.

Exhibit 1017, 8:2-7.

Next, the phosphorus atoms implanted in the N-well regions **15** and the boron atoms outside the N-well from the optional adjustment implant are driven into the substrate during a high-temperature step.

Exhibit 1017, 8:9-12.

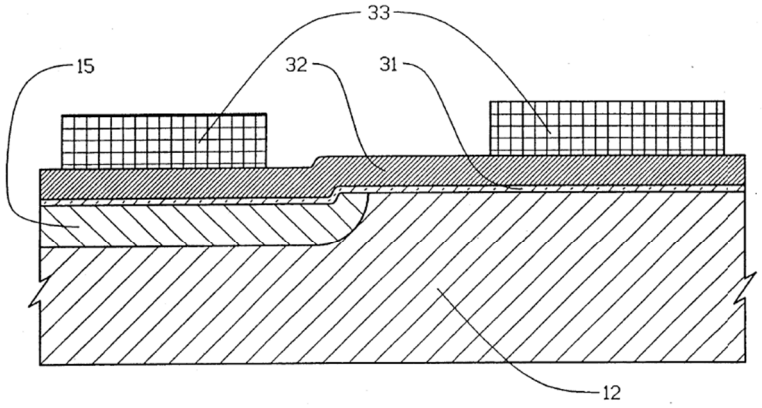



FIG. 3

333. In *Lowrey* Figure 3 (above),

following the stripping of silicon dioxide masking layer **21** and first pad oxide layer **11**, a second pad oxide layer **31** is grown on the surface of the entire wafer. This is followed by the deposition of a second silicon nitride layer **32**. A second photomask **33** defines active areas for both P-channel devices (those that will be constructed in the N-well) and N-channel devices.

Exhibit 1017, 8:13-20.

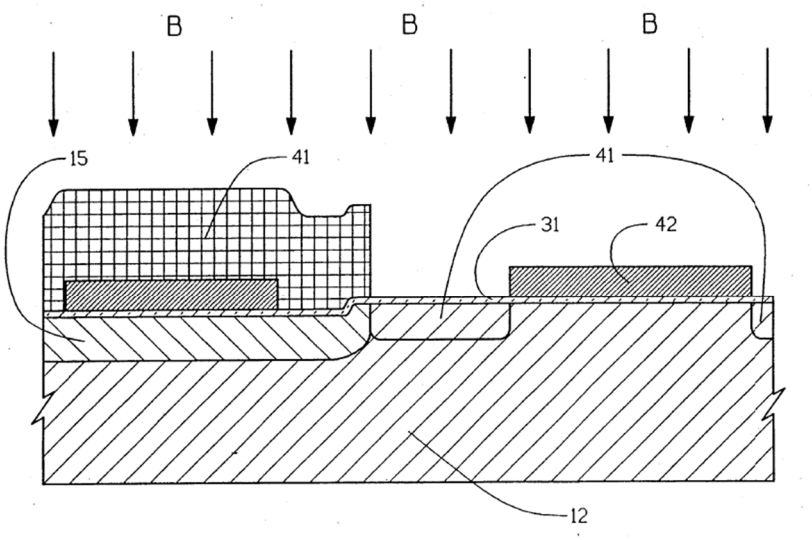



FIG. 4

334. In *Lowrey* Figure 4 (above),

> following the etching of second nitride layer **32**, the N-well regions are covered with a third photomask **41**. The wafer is then subjected to a field isolation boron implant. During this step, boron atoms are implanted only in the N-channel field regions. Third photomask prevents the implantation of boron in the N-well field regions and the N-channel active area nitride mask **42** (a remnant of nitride layer **32**) prevents the implantation of born into the future N-channel active areas.

Exhibit 1017, 8:21-30.

335. Referring to Figure 5, *Lowrey* states:

> following the stripping of third photomask **41** and growth of field oxide regions **51** using the conventional LOCOS oxidation process, second nitride layer **32** is stripped, as is second pad oxide layer **31**. A layer of sacrificial oxide is then grown to

eliminate the "white ribbon" effect in active areas that resulted from field oxidation. Following an unmasked VT implant which adjusts transistor threshold voltage, the sacrificial oxide layer is stripped and a gate oxide layer **52** is grown. Alternatively, second pad oxide layer **31** may be left intact in order to serve as transistor gate oxide in both N-channel and P-channel regions. A polysilicon layer **53** is blanket deposited and then doped with phosphorus to render it conductive. A fourth photomask **55** is used to cover or blanket polysilicon layer **53** in the P-channel regions and to define N-channel transistor gates **56** and N-channel interconnects **57**. The etch of polysilicon layer **53**, which follows the fourth photomasking step, also removes a small amount of the exposed portions of field oxide regions **51** and gate oxide layer **52** (or second pad oxide layer **31** if it is used as gate oxide).

Exhibit 1017, 8:31-52.

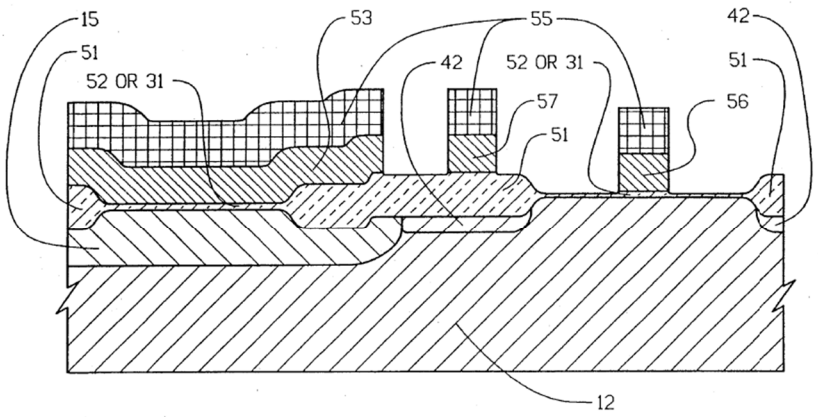



FIG. 5

336. As shown in Figures 4 and 5, before and after the LOCOS regions have been grown, there is a non-planar surface topology extending across the entire wafer including raised and recessed regions on the wafer surface.

Trench Isolation Is Incompatible With *Lowrey*

337. At the point of growing the field oxide region **51** in the *Lowrey* process, the wafer structure is built up to such a point that fabricating a trench isolation would destroy at least a part of the structure already built up in *Lowrey* during previous steps. This is because *Lowrey*'s surface topology prior to LOCOS field oxide formation is non-planar as shown in *Lowrey*'s Figure 4.

338. The STI process has three major steps: (i) trench etching; (ii) refilling the trench (and coating the entire wafer) with an insulator (typically by deposition of CVD $SiO_2$), and (iii) planarization of the wafer (e.g. by CMP). Planarization has the effect of flattening the topology of the wafer by removing the excess $SiO_2$ from the wafer.

339. *Lowrey* Figure 4 shows that the "third photomask **41"** (photoresist mask) and the "N-channel active area nitride mask **42**" are used to limit the area of the "field isolation boron implant" (note that the "field isolation boron implant" is mislabeled as **41**).

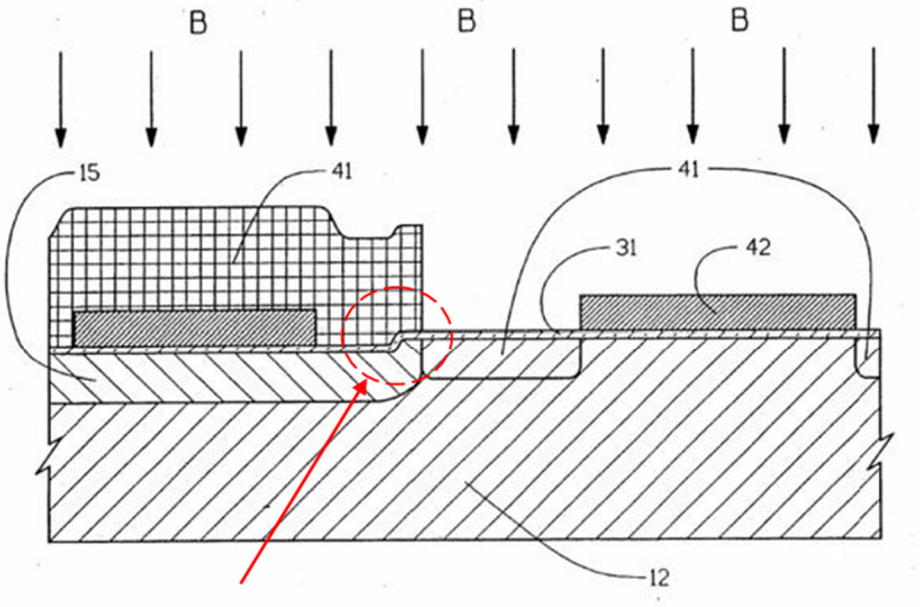



FIG. 4

340. The wafer at this stage has a non-planar modulated surface topology; specifically, there is a ***step*** on the Si surface (located slightly to the left of the center of the image). Subsequently, the photoresist mask **41** is removed and the area not covered by the $Si_3N_4$ mask is thermally oxidized using the LOCOS process. *Lowrey's* Figure 5 shows the completed LOCOS isolation ($SiO_2$) ("field oxide regions **51**"). The LOCOS isolation ($SiO_2$) conformably coats the non-planar surface of the wafer thereby reproducing the step on top of the "field oxide regions **51**".

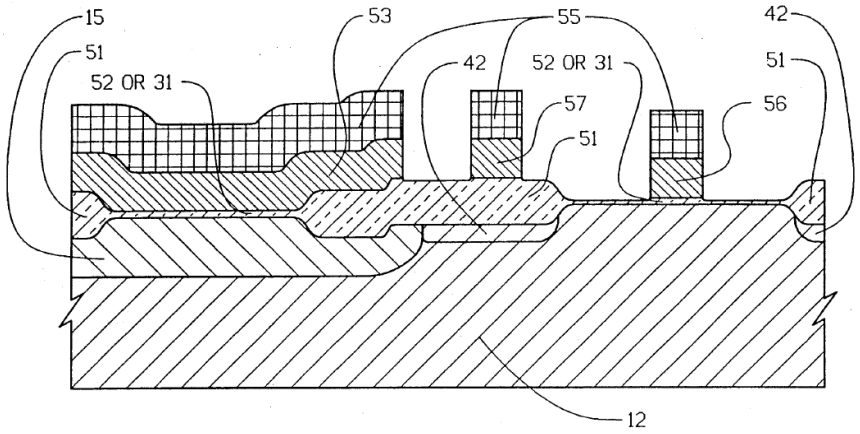



FIG. 5

341. If trench isolation were performed instead of LOCOS isolation multiple issues arise:

342. *First*, the wafer surface area on which the trench would be etched is non-planar. As a result, the bottom of the trench would be non-planar. This in turn would result in a non-uniformity of the trench causing non-uniformities of the electric field in the Si under the STI that would in turn result in the enhancement of leakage currents.

343. *Second*, since the STI process would conclude with the required planarization, the planarization would either (i) *leave unwanted* insulation material ($SiO_2$) in recessed areas of the Si wafer ("valleys") or (ii) *remove wanted* material from raised areas of the Si wafer ("hilltops"). This is illustrated in *Lowrey*'s colorized and annotated Figure 4, shown below, in which two planarization surfaces are assumed as indicated by the two red dashed lines. In one case,

unwanted material is left on the wafer surface (**green region**). In the other case, wanted material is removed from the wafer (**blue region**). Neither scenario is acceptable.

344. A third alternative would be to do both, leave unwanted material *and* remove wanted material, which would also be unacceptable.

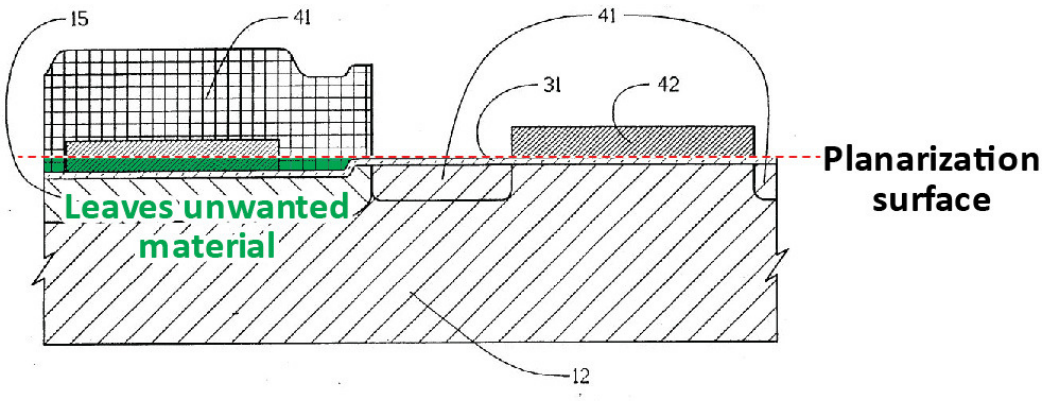



FIG. 4

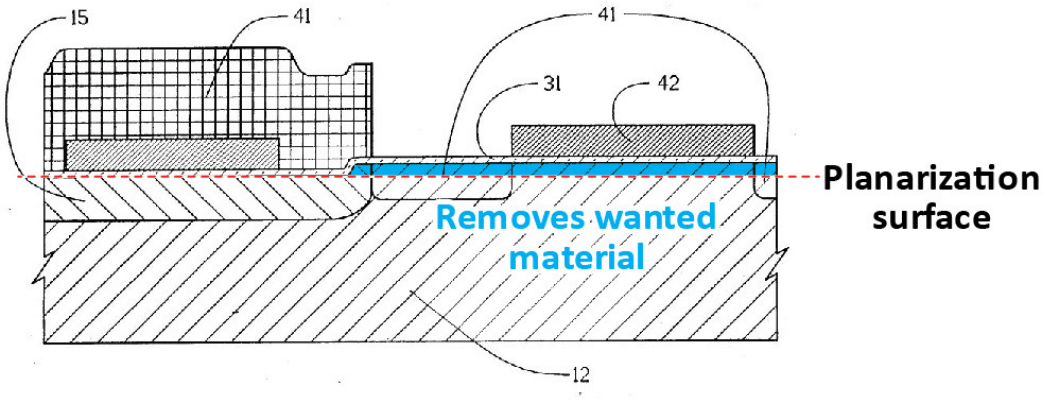
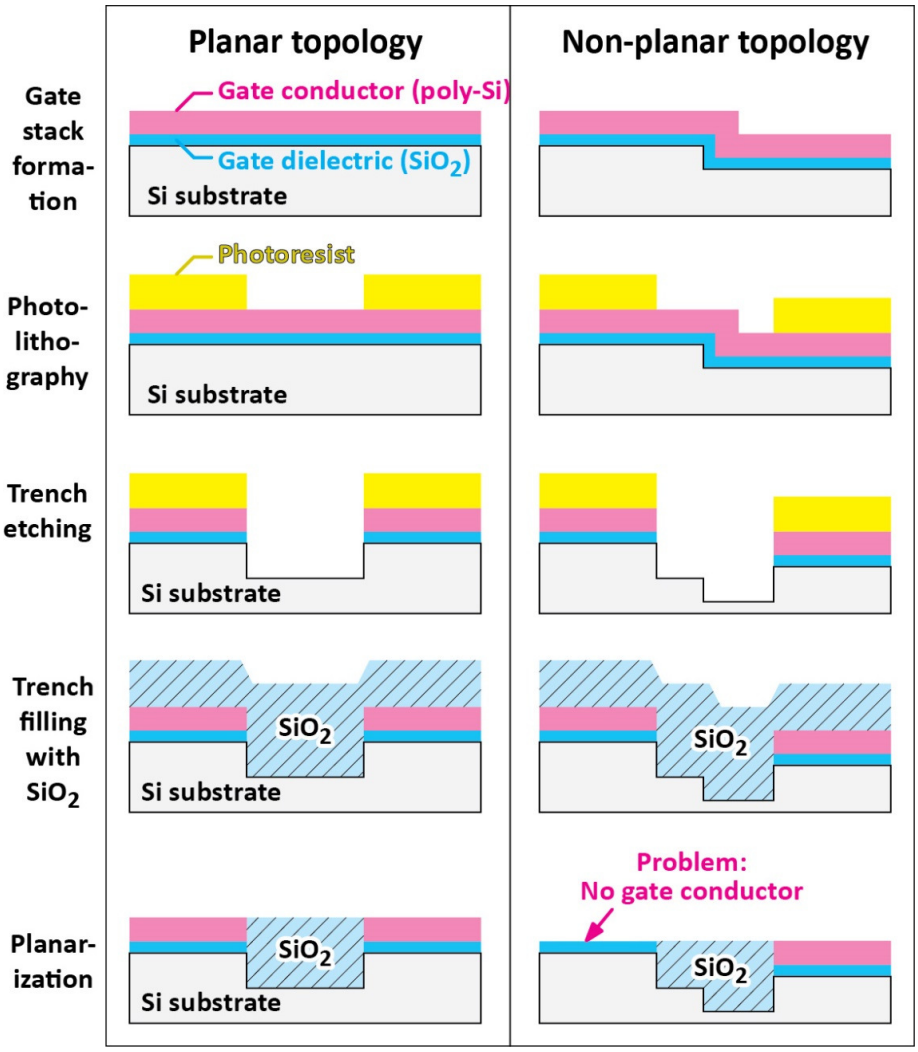



FIG. 4

345. Thus, if a trench were etched, and then filled with $SiO_2$, the "overflowing $SiO_2$" would fill valleys (i) where it could not be removed (by CMP) without (ii) removing wanted material in other places (by CMP). That is, the CMP

process planarizes a Si wafer in its entirety and the local and selective removal of material is not an option. The resulting dilemma is not addressed by Petitioner.

346. The schematic figure below shows the formation of trench isolation on a wafer having (i) planar surface topology (left-hand side column) and (ii) non-planar surface topology (right-hand side column). The steps indicated are gate stack formation, photolithography, trench etching, trench refilling with silicon dioxide, and planarization.



347. The figure above schematically shows the problem that arises when forming a trench isolation feature on a wafer having non-planar surface topology: Due to the non-planar starting topology, the gate conductor partially vanishes during planarization (see bottom figure at right). Such destruction of the gate conductor is not acceptable.

348. Leaving unwanted oxide on the wafer may mask certain areas and create unwanted electrical discontinuities (open circuits) thereby rendering the wafer non-functional. Alternatively, removing wanted material from the wafer can cause layers to be removed (or modified) that are required for the proper functioning of the IC device. A POSITA would find either scenario unacceptable.

349. Consequently, Petitioner has not born its burden of persuasion justifying any motivation for the POSITA to have substituted STI for LOCOS isolation in *Lowrey* given the non-planar topology of *Lowrey*. A POSITA would not make such a substitution and if done nevertheless, a non-functional IC device would result.

*Lowrey* Cannot Be Combined With *Noble*

350. *Noble* discloses a MOSFET with raised shallow trench isolation ("STI") self-aligned to the gate stack along the gate width direction. The gate conductor has first and second edges bounded by raised isolation structures (*e.g.,* STI). A source is self-aligned to the third edge and a drain diffusion is self-aligned

to the fourth edge of the gate electrode. Exhibit 1015, Abstract, 2:54-56. The process of forming the trench isolation is described in the summary of the invention wherein it is specifically stated that a gate dielectric layer and a gate conductor layer are ***first*** deposited wherein the first portion of the gate stack is removed to allow for etching of a trench. Exhibit 1015, 2:58-63.

351. *Noble* points out a multitude of problems associated with forming the trench isolation prior to depositing the gate dielectric and conductor ("wrap-around effect," "parasitic leakage paths," "corner parasitic device," "sub-threshold leakage current," "corner leakage problem," and "degrade device performance") Exhibit 1015; 1:20-2:4. Accordingly, *Noble* discloses the deposition of the gate dielectric layer and gate conductor layer ***before*** the trench formation. This sequence is evident from *Noble*'s Figure 10, shown below and inherent to the process design and engineering of *Noble*. A POSITA would have no reason whatsoever to ignore *Noble*'s teaching. Indeed, a trench isolation formation without the pre-deposited gate structure (gate dielectric plus gate conductor) would substantially deviate from the teaching of *Noble* and thus be unacceptable.

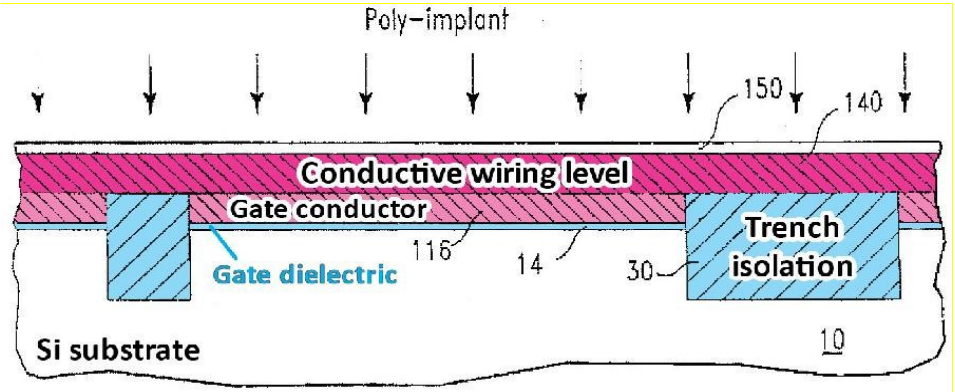


FIG. 10

352. *Noble* was preoccupied with the problems associated with forming the trench isolation prior to laying down the gate conductor and so *Noble* discloses deposition of the gate dielectric layer and gate conductor layer before forming the STI. This sequence is part and parcel of the process design and engineering of *Noble*, and a POSITA would have absolutely no reason whatsoever to ignore it since the trench isolation that would be formed without these pre-deposited structures would be unacceptable. Thus, *Noble* expressly teaches away from using the approach of *Lowrey* with respect to the sequence of gate stack formation.

353. Furthermore, as explained earlier, *Noble* deposits the gate dielectric and gate conductor film ***before*** forming the STI. The first step of *Noble* is the deposition (or growth) of the thin gate dielectric film **14** ("gate dielectric") and the gate conductor **116** ("gate conductor") on substrate **10**. It is only thereafter, that the raised shallow trench isolation (STI) **30** ("raised STI") is formed so as to define and surround the active area. The STI process concludes with a planarization step

(*e.g.* CMP) that leaves the Si wafer (substrate **10**) surface planarized or flat as shown in *Noble*'s Fig. 9, reproduced below:

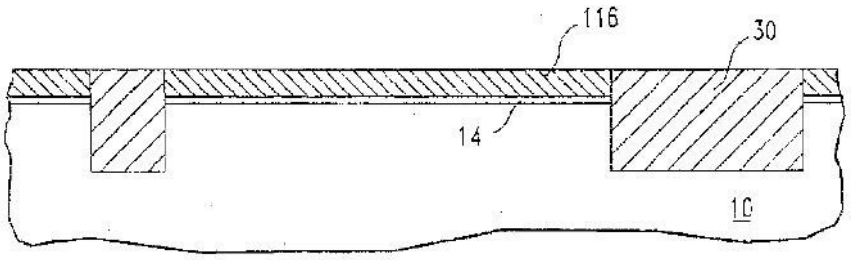



FIG. 9

354. In summary, as noted above, *Noble* forms the raised STI isolation feature only ***after*** depositing the gate dielectric film and gate conductor film.

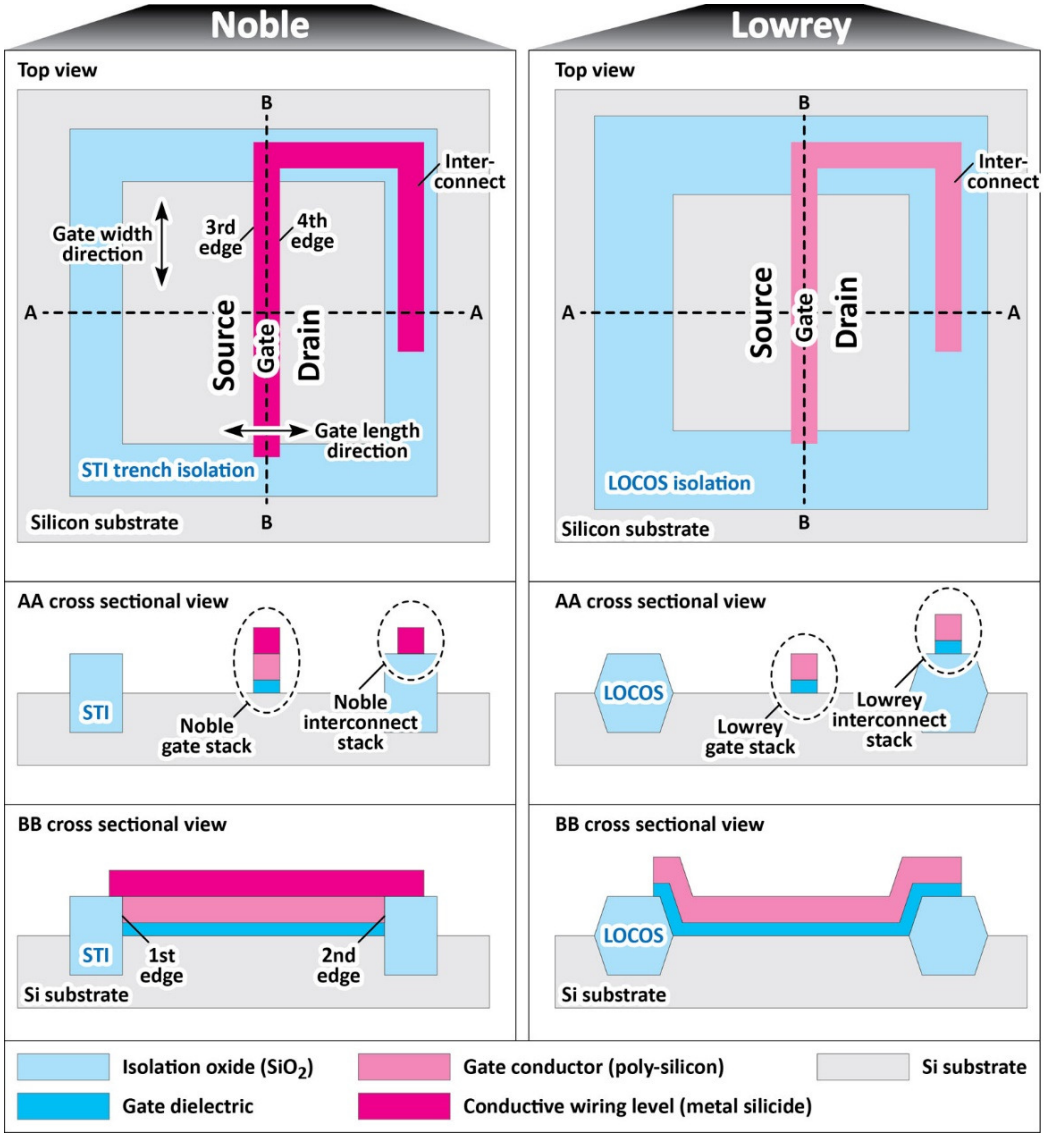
355. *Noble* states:

> These and other objects of the invention are accomplished by a semiconductor structure comprising a transistor with a gate comprising an individual segment of gate conductor on thin dielectric. The gate conductor is substantially coextensive with the thin dielectric. The gate conductor has a top surface having opposed first and second edges and opposed third and fourth edges. Raised isolation bounds the first and second edges of the gate conductor. A source is self-aligned to the third edge and a drain is self-aligned to the fourth edge. A conductive wiring level is in contact with the top surface.
>
> Another aspect of the invention provides a method of forming an FET comprising the steps of providing a substrate having a gate stack comprising a layer of gate dielectric and a layer of gate conductor, the gate stack having a top surface;

removing first portions of the gate stack and etching a trench in the substrate thereby exposed for raised isolation; depositing insulator and planarizing to the top surface of the gate stack; removing second portions of the gate stack for source/drain regions and to expose sidewalls of the gate stack adjacent the source/drain regions.

Exhibit 1015, 2:47-3:3 (underscore added).

356. The above-quoted description is depicted below.



The above depiction shows the *Noble* structure on the left in contrast to *Lowrey* structure on the right.

357. The gate conductor in *Noble* has 3rd and 4th edges that are aligned with the source and drain, respectively, as shown above ("A source diffusion is self-aligned to the third edge and a drain diffusion is self-aligned to the fourth edge.") Exhibit 1015, Abstract.

358. The gate conductor in *Noble* has 1st and 2nd edges that are bounded by the raised trench isolation, as shown above ("Raised isolation bounds the first and second edges of the gate conductor.") Exhibit 1015, 2:53-54. As a consequence of the process, the two gate ends along the gate width direction ("first and second [gate] edges") are aligned with the raised STI; this is because the STI trench etching defines the end of the gate electrode (along the gate width direction).

359. In contrast, *Lowrey*'s gate conductor cannot be bounded by the isolation structure (neither LOCOS nor STI) because the gate conductor is deposited subsequent to the isolation structure (i.e. there is no self-alignment between the gate electrode and the isolation structure) and also because the gate conductor has the additional purpose of serving as a interconnect conductor. This dual purpose of the gate conductor in *Lowrey* is different from *Noble* who has different structures for the gate conductor and the interconnect conductor

(*Lowrey*'s dual-purpose structures are marked by dashed circles in an annotated version of *Lowrey*'s Figure 8, shown below).

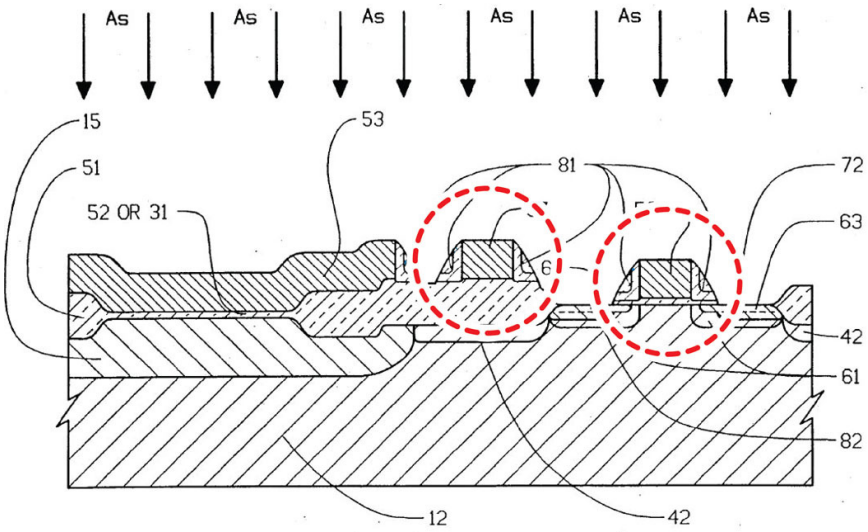



FIG. 8

360. *Noble* additionally explains why this process sequence was chosen:

> It is another object of the present invention to prevent the gate conductor from wrapping around the trench corner. It is another object of this invention to avoid gate dielectric thinning adjacent the corner. It is another object of this invention to avoid sharpening of the corner.

Exhibit 1015, 2:30-35 (underscore added).

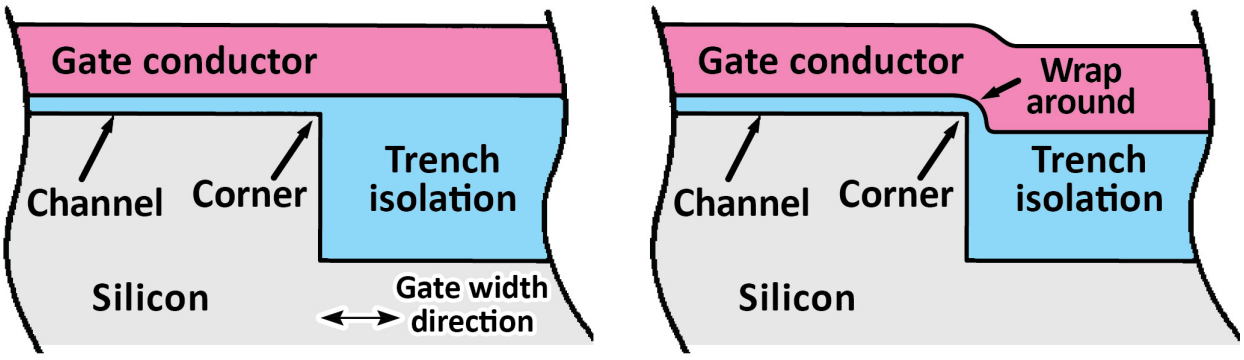
361. That is, *Noble* specifically utilizes a process sequence contrary to that of *Lowrey* to attain the above-recited benefits. *Noble* explicitly cautions about deleterious effects that have plagued prior-art trench isolation structures:

> Parasitic leakage paths have been created by the proximity of a semiconductor device to an edge or corner of either type of

> trench. In one leakage mechanism [...] the parasitic leakage path results from an enhancement of the gate electric field near the trench corner [...] in a worst case scenario for corner field enhancement, the gate conductor wraps around the trench corner. This happens when the oxide fill in the isolation trench is recessed below the silicon surface [...] Thus, a parallel path for current conduction is formed [...] the corner device can even dominate [...] Furthermore, there exists concern that the enhanced electric fields due to field crowding at the corner impact dielectric integrity. [...] This corner leakage problem has commonly been controlled with an increased threshold tailor implant dose, but this can degrade device performance. Thus, alternate schemes for controlling the corner are needed.

Exhibit 1015, 1:20-2:22 (emphasis added).

362. The corner at the edge of the trench isolation is illustrated in the left hand-side figure below (adapted from Exhibit 2022):




(a) after Bryant, 1993, Exhibit 2022, page 413 (b) Gate-wrap-around problem

363. The gate-wrap-around problem occurs when the trench isolation is recessed with respect to the Si surface so that the gate conductor wraps around the

Si corner as indicated in the right-hand-side figure above. The corner is a spatial non-uniformity that creates high electric fields and leakage current paths that are deleterious to device operation. *See* Exhibits 2022 and 2023.

364. A POSITA would have taken into account the multitude of warnings expressed by *Noble*. Thus, a POSITA would not have simply taken the STI from *Noble* and used it in the structure formed through the processes of *Lowrey*. Instead, a POSITA would have seen that the processes in *Lowrey*, in which the gate electrode is necessarily deposited ***after*** the LOCOS isolation is formed, are incompatible with the very purpose of the approach used in *Noble*.

365. Moreover, a POSITA would have found a *Lowrey-Noble* combination non-functional for the following reasons:

366. ***First***, it is not possible to follow *Lowrey*'s process by simply substituting *Noble*'s trench isolation for *Lowrey*'s LOCOS isolation. *Lowrey* ***starts*** with LOCOS isolation[30] formation ***followed*** by gate dielectric and gate conductor formation, while *Noble* ***starts*** with gate dielectric and gate conductor formation ***followed*** by trench isolation formation. *Noble* specifically relies on the pre-existence of gate dielectric and gate conductor when forming the trench isolation. Therefore, *Lowrey*'s subsequent deposition of gate dielectric and gate conductor

[30] Note that *Lowrey* has several steps, specifically three photomasking steps, that precede LOCOS formation. These initial steps preceding the LOCOS formation create a nonplanar surface topology.

could only be applied on top of *Noble*'s pre-existing structure, thereby making the *Lowrey-Noble* combination devices inoperative.

367. ***Second***, it is not possible to simply start with *Noble*'s trench isolation without first forming the gate dielectric and gate conductor because *Noble*'s trench isolation formation relies on the availability of the gate dielectric and gate conductor. Thus, it would undermine the *Noble* process to go directly to trench isolation formation, and leave out the initial formation of the gate dielectric and gate conductor. Accordingly, it would not be possible to simply substitute the trench isolation in Noble for the LOCOS isolation of *Lowrey*.

368. *Noble* specifically relies on the pre-existence of gate dielectric and gate conductor when forming the trench isolation. Therefore, *Lowrey's* subsequent deposition of gate dielectric and gate conductor could only be applied on top of *Noble's* pre-existing structure, thereby making the *Lowrey-Noble* combination devices inoperative.

369. ***Third***, if a POSITA were to use *Noble*'s approach – deposition of the gate dielectric and gate conductor of *Noble instead* of the gate dielectric and gate conductor of *Lowrey* – the interconnect conductor could not be deposited simultaneously with the gate conductor as *Lowrey* contemplates. That is, *Noble*, due to its raised trench isolation, exhibits a distinct height difference between the gate (consisting of elements **14**, **116**, **140**, and **150**) and interconnect (consisting of

elements **140** and **150**). This is apparent in *Noble* Fig. 11, shown below (with colors, annotation, and numerals **140** and **150** of interconnect added for clarity):

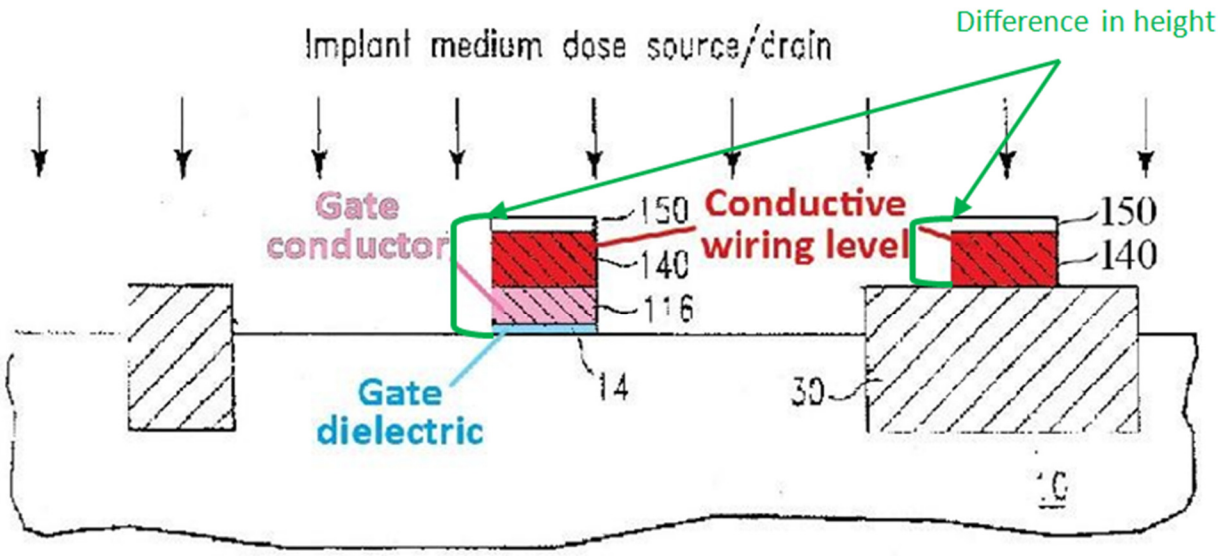
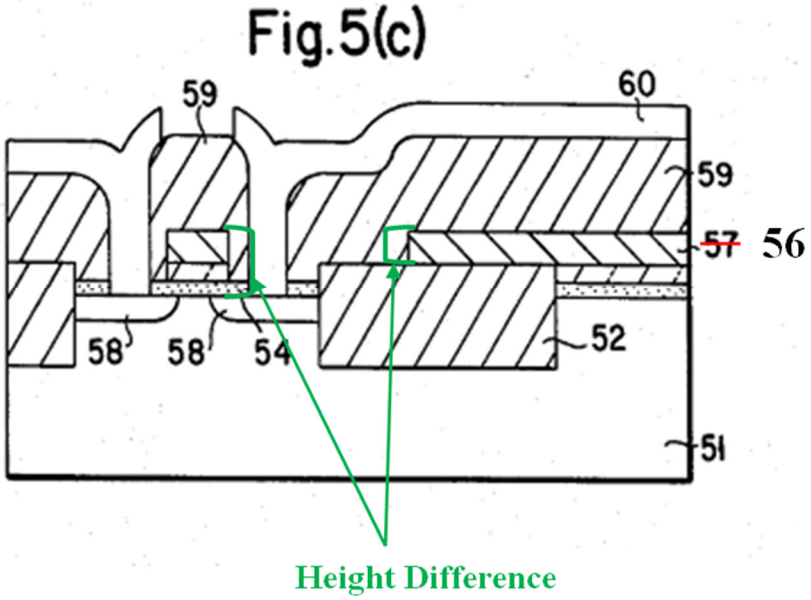



FIG. 11

370. The same relative height difference is apparent in Fig. 5(c) below[31]:




[31] Correcting typo in Figure 5(c). Element 57 should be 56.

371. In stark contrast to *Noble*, *Lowrey* employs the same element for the gate conductor and interconnect conductor. This is apparent from *Lowrey*'s disclosure that the polysilicon used to form the gate electrode and the interconnect is deposited in a single process and then that single structure is etched:

> ***A polysilicon layer 53 is blanket deposited*** and then doped with phosphorus to render it conductive. ***A fourth photomask 55 is used to cover or blanket polysilicon layer 53 in the P-channel regions and to define N-channel transistor gates 56 and N-channel interconnects 57***. The etch of polysilicon layer 53, which follows the fourth photomasking step, also removes a small amount of the exposed portions of field oxide regions 51 and gate oxide layer 52 (or second pad oxide layer 31 if it is used as gate oxide).

Exhibit 1017, 8:42-52 (emphasis added).

372. *Lowrey*'s process teaches the use of the same structural features for elements serving different purposes. Thus, *Lowrey* explicitly teaches the use of the same elements for the gate conductor and interconnect conductor, while *Noble* employs different structures. Using different structures contradicts the teaching of *Lowrey* and thus a POSITA would not look to *Noble*'s shallow trench isolation when implementing *Lowrey*'s device, as *Noble* teaches away from *Lowrey*'s structure. Using different conductors for the gate and the interconnection, which is

the key starting point of *Noble* as a precedent to forming the raised trench isolation, would result in a gate stack and interconnect stack having different heights.

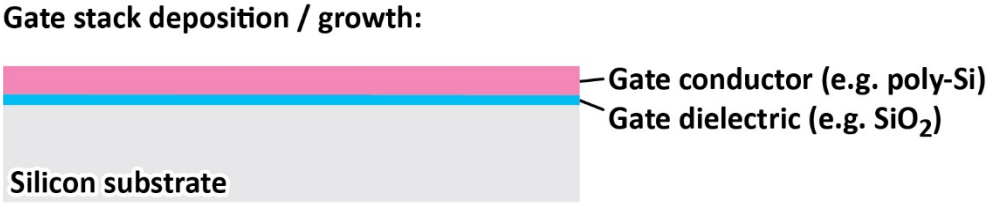
373. To somehow re-fabricate the structure disclosed in *Lowrey* by using the *Noble* trench fabrication sequence would destroy the *Lowrey* structure (because of *Lowrey*'s topology problem) and undermine its design (because *Lowrey*'s design would lose its hallmark feature of using the same layer stack for the gate and interconnect stack as indicated by the red dashed circles in the annotated Figure 8 of *Lowrey*, shown above).

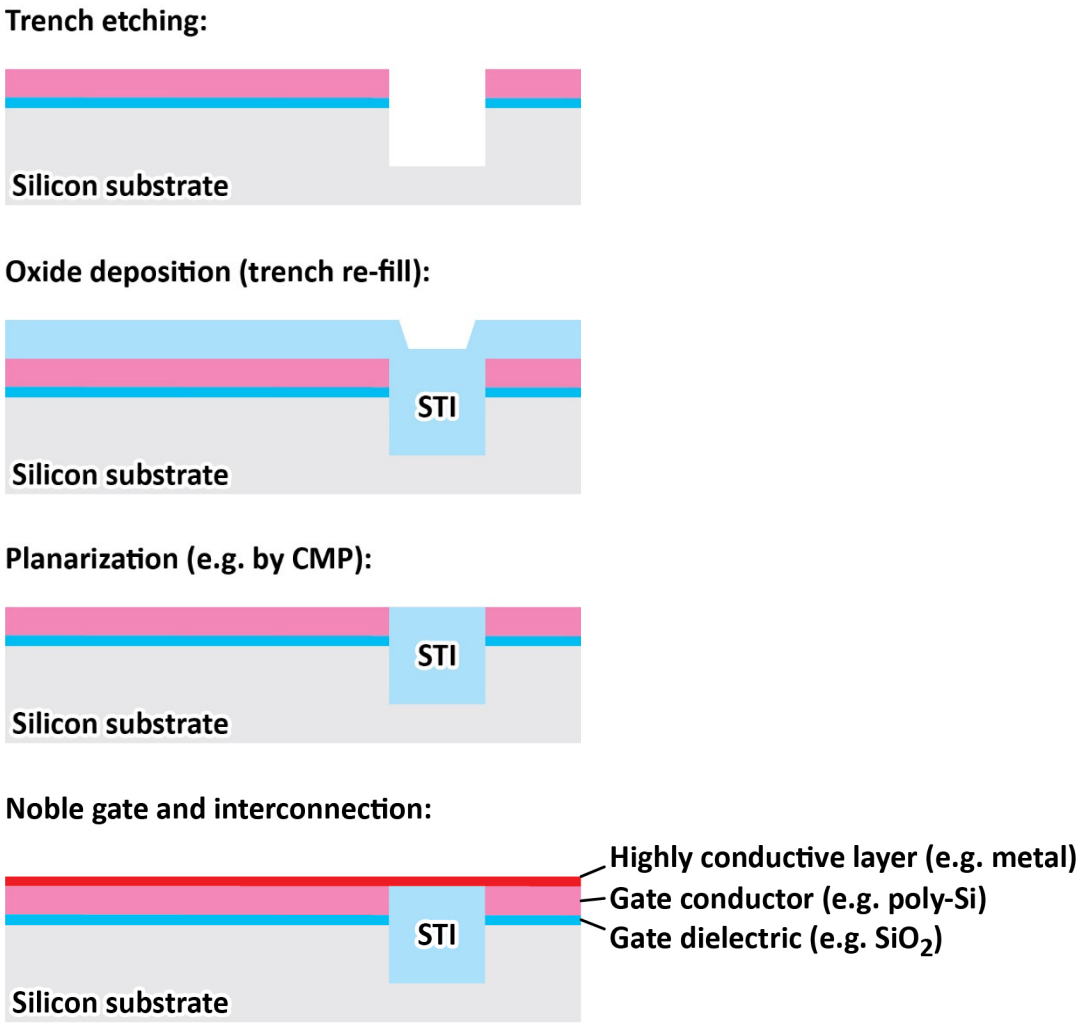
No Second L-Shaped Sidewalls

374. Without guidance, it is impossible to know exactly what Petitioner believes a combination of the *Lowrey* and *Noble* devices would look like. However, just looking at the trench fabrication process of *Noble* (which Petitioner wishes to employ), the following steps would take place:

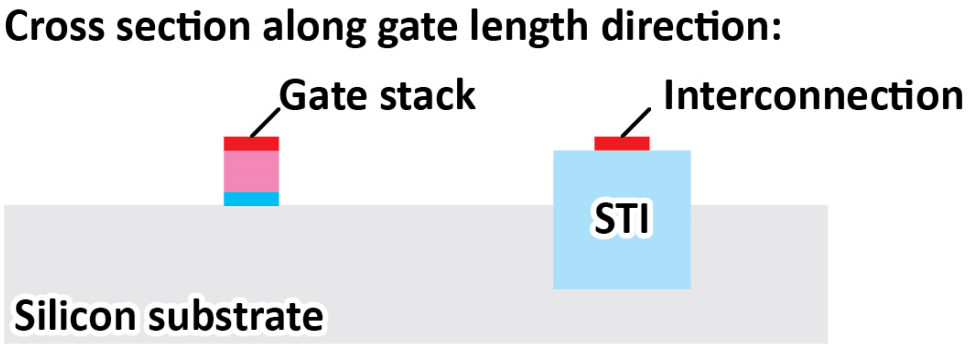
**Process sequence forming the *Noble* gate stack and interconnect:**

---



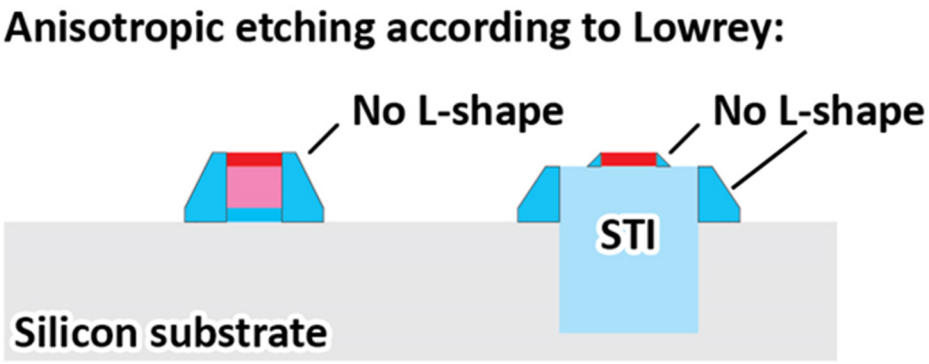



375. As shown above, *Noble* teaches first applying a gate dielectric and gate conductor, after which a highly conductive layer is applied. The highly conductive layer extends across the gate stack and the interconnection.

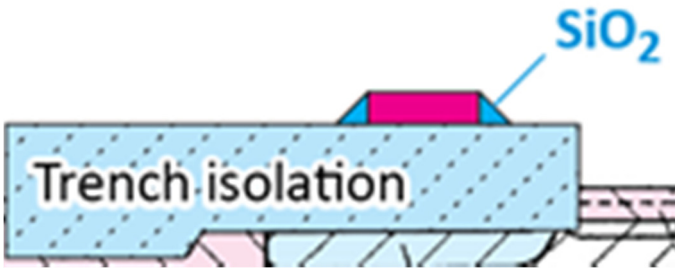



376. After photolithographic patterning and etching, due to the height of the STI, it is seen that the lower two layers (blue-colored gate dielectric and pink-colored gate conductor) are part of the gate stack, but they do not extend above the STI and are otherwise etched away.

377. Then, as per *Lowrey*, two sidewall layers **62** and **71** are applied and then anisotropically etched to provide the structure below:



378. After anisotropic etching of the modified *Lowrey* device, it is seen that the interconnection is of such low height relative to the gate stack[32] that there is little opportunity for something resembling an L-shape to form and what forms is likely not much more than a nub or blob having no distinguishable shape. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall). This is how the trench of Figure 14 of *Lowrey* would likely look if a trench isolation as per *Noble* were substituted for the LOCOS of *Lowrey*:




379. Claim 1 requires a "second" L-shaped sidewall. As shown above, the $SiO_2$ sidewalls on the interconnection would appear as small nubs or blobs.

380. In addition, neither *Lowrey* nor *Noble* discloses L-shaped sidewalls, and thus, the combination would not disclose "first L-shaped sidewalls formed

[32] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.

over the side surfaces of the gate electrode" or "second L-shaped sidewalls formed over the side surfaces of the interconnection."

381. The sidewalls of *Noble* include a single structure shaped like a quarter circle (or quarter ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. That is to say, *Noble* does not disclose a sidewall that is substantially shaped like a capital letter "L" or its mirror image.

382. The sidewalls of *Lowrey* also include a single structure shaped like a quarter circle (or ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. Although the figures in *Lowrey* show that the sidewalls have two structures, this is a result of illustrative convenience for the inventors of *Lowrey* in illustrating their invention, and not what is actually in the structure in *Lowrey*.

383. In particular, *Lowrey* describes the formation of the sidewalls as follows. A "mini-spacer oxide layer **62**" is formed by a thermal oxidation or chemical vapor deposition (CVD). Exhibit 1017, 8:58-62. The purpose of the mini-spacer oxide layer **62** is to subsequently create lightly-doped n-type source/drain regions **63** that are offset from the vertical boundaries of punch-through implant regions **61** by the mini-spacer oxide layer **62**. Exhibit 1017, 8:62-9:2. After the lightly-doped n-type source/drain regions **63** are formed, a "first spacer oxide layer **71**" is formed: "Referring now to FIG. 7, all circuitry is blanketed with a first

spacer oxide layer **71** by one of various techniques (e.g., chemical vapor deposition)." Exhibit 1017, 9:3-5.

384. Layer **62** is made of "oxide" (e.g. thermal oxidation) and layer **71** is also made of "oxide" (e.g. chemical vapor deposition), where "oxide" refers to silicon dioxide or $SiO_2$. That is, both layers, **62** and **71**, are made of the same material, "oxide". Subsequently, the two layers are subjected to an anisotropic etch to form a single sidewall spacer **81**:

> Referring now to FIG. 8, first spacer oxide layer **71** and mini-spacer oxide layer **62** are etched with a first anisotropic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers **81** for N-channel transistor gates **56**, N-channel interconnects **57** and the portion of polysilicon layer **53** which blankets the P-channel regions."

Exhibit 1017, 9:6-12.

385. The fact that both layers, **62** and **71** are made of the same material, "oxide", is significant. Given that layers **62** and **71** are made of the same material means that they are indistinguishable. That is, a microscopic assessment technique such as scanning electron microscopy (SEM) in 1995 would show the two layers as an indistinguishable entity (Exhibits 2026 - 2030)[33] so that layer **62**, which Dr.

[33] References both pre- and post- 1995 are supplied to show the common usage of this technique.

Banerjee contends would be L-shaped, would not substantially resemble a capital letter L (or its mirror image). This is because layer **62** cannot be contrasted or distinguished from layer **71**. Indeed, *Lowrey* discloses that these layers **62** and **71** combine to form sidewall spacer **81**. Exhibit 1017, 9:6-12.

386. A necessary condition for a feature to substantially resemble a capital L is that it is distinguishable from surrounding features. Given that layer **62** is chemically indistinguishable from layer **71**, its physical appearance is indistinguishable from layer **71** as well. *See* sidewall spacer **81** (pink) depicted Fig. 8 below:

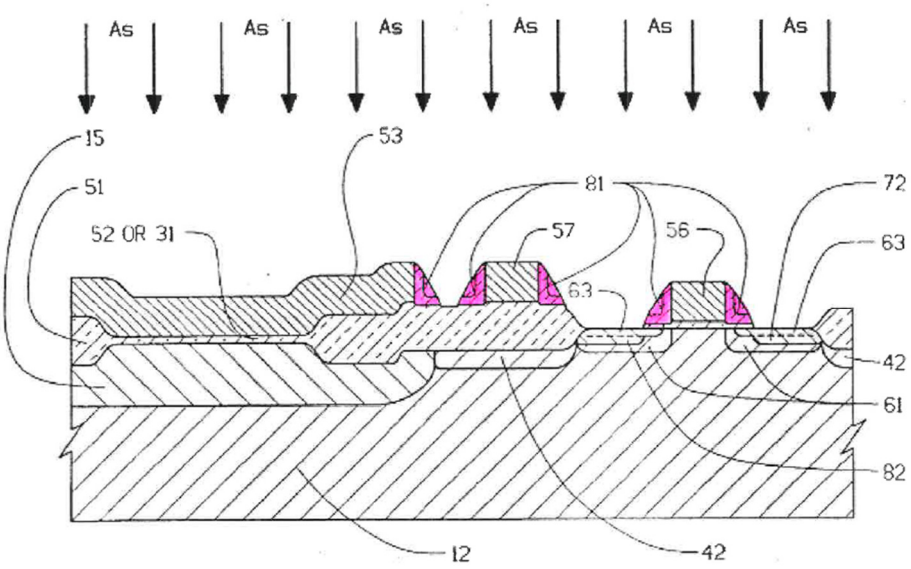



FIG. 8

Conclusions Regarding The *Lowrey-Noble* Combination

387. For these reasons, a POSITA would not have been motivated to combine the two very different disclosures of *Lowrey* and *Noble*. Because the fabrication processes are incompatible, and because the combination would be non-functional, there would be no reason to combine the references.

388. Moreover, to the extent that Dr. Banerjee is suggesting that a POSITA would have combined certain portions of *Lowrey* with certain portions of *Noble* in such a manner that it would render the claims of the '174 patent obvious, he seems to be conveniently picking and choosing elements from each reference in order to obtain a device that has all of the elements of the claims of the '174 patent, and not focusing on how a POSITA actually would have combined the references, if at all (and as stated above, they would not).

389. Moreover, it appears that Tyler Lowrey, the lead inventor on *Lowrey*, was aware that trench isolation could be used in semiconductor devices to separate active areas before the filing of *Lowrey*. In particular, WIPO Publication No. WO9005377, published on May 17, 1990 (before the filing date of *Lowrey*) (Exhibit 2031), identifies Tyler Lowrey as an inventor on a PCT patent application that is directed toward the use of trench isolation in a semiconductor device. For example, the WIPO publication refers to trench isolation as a possible approach in semiconductor devices, noting that it has its advantages and disadvantages.

Exhibit 2031, 2:23-28. If it were obvious to substitute the LOCOS isolation of *Lowrey* with trench isolation, as Dr. Banerjee suggests, then I would expect that the inventors on *Lowrey*—who were aware of trench isolation—to have identified trench isolation as an alternative to LOCOS isolation in *Lowrey*.

Petitioner Fails To Meet Its Burden To Establish That *Lowrey* In Combination With *Noble* Renders At Least Claim 1 Unpatentable

390. Claim 1 specifically recites a "trench isolation" which is absent from *Lowrey*. A POSITA would have no motivation to substitute the raised trench isolation of *Noble* for the LOCOS isolation of *Lowrey* for the following reasons:

i. The trench isolation of *Noble* cannot be substituted for the LOCOS isolation of *Lowrey* because such a substitution would involve planarizing a pre-existing device structure (that has a non-planar surface topology) in a way which a POSITA would not have been motivated to do.

ii. Formation of the *Noble* trench requires the prior deposition of two layers **14** and **116** which would be incompatible with the layers already present in *Lowrey*.

iii. *Lowrey* exhibits no capital "L" shaped sidewalls on the interconnection or the gate electrode because the two applied layers

result in what resembles a single layer 81, which contains no sidewall resembling a capital "L" or its mirror image.

iv. There would be no reason to maintain L-shaped sidewalls on the device of *Lowrey* in Figure 8.Combination of *Lowrey* with *Noble* would result in a device having no capital L-shaped sidewalls on the interconnection, but would merely have nubs or blobs instead. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall).

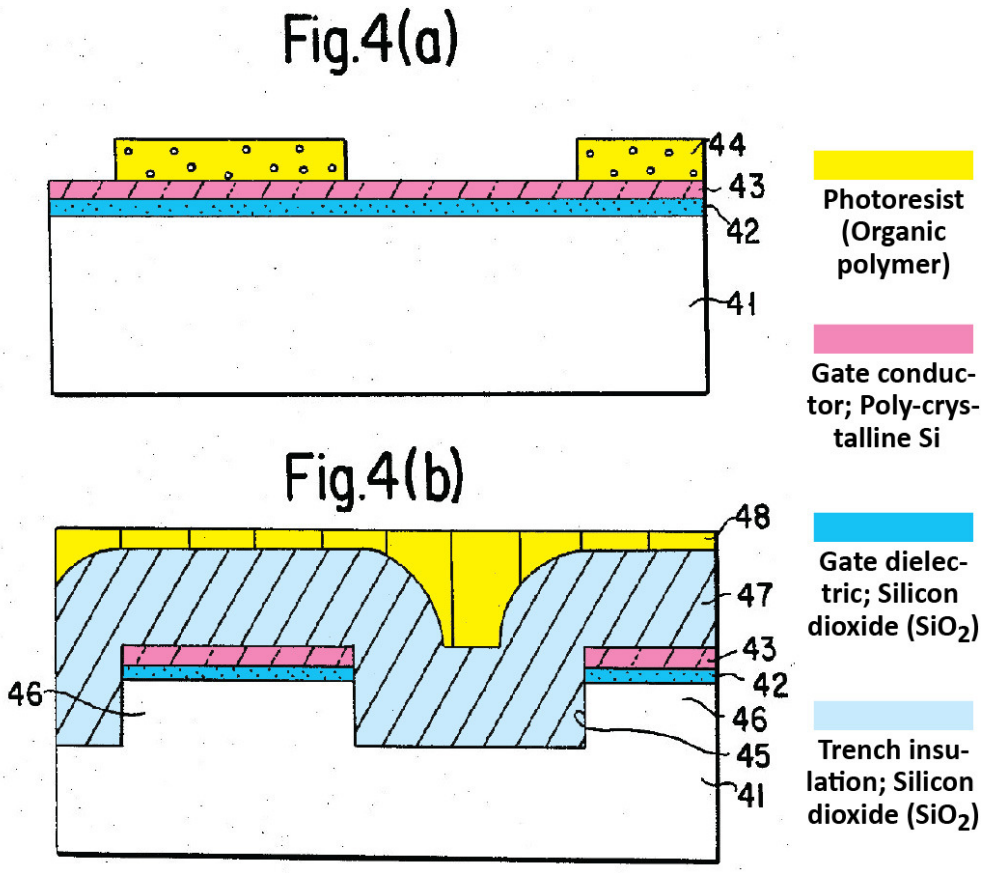
**Combination: *Lowrey* And *Ogawa***

391. Petitioner has additionally asserted that the challenged claims are unpatentable under 35 U.S.C. §103 based upon *Lowrey* and *Ogawa.* Generally speaking, the combination of *Lowrey* and *Ogawa* would not have rendered any of the challenged claims obvious for the same reasons the combination of *Lowrey* and *Noble* would not have rendered any of the challenged claims obvious. It is important to note that once again the Petition fails to describe how the teachings or fabrication processes of *Lowrey* and *Ogawa* could be combined. A POSITA would understand that a Si IC device must be fabricated by a functioning and reasoned sequence of fabrication steps. In the absence of such sequence (Petitioner provided

neither pictorial nor narrative process sequence), a Si IC device having specific elements becomes meaningless.

Initial Processing Sequence Of *Ogawa*

392. *Ogawa* discloses the initial processing steps of a Si IC fabrication sequence. The initial steps are shown in *Ogawa's* Figures 4(a) and (b) reproduced below (colorized):




393. The first step, shown in *Ogawa's* Figure 4(a), is the deposition of the thin gate dielectric film **42** ("silicon dioxide layer") and the gate conductor **43**

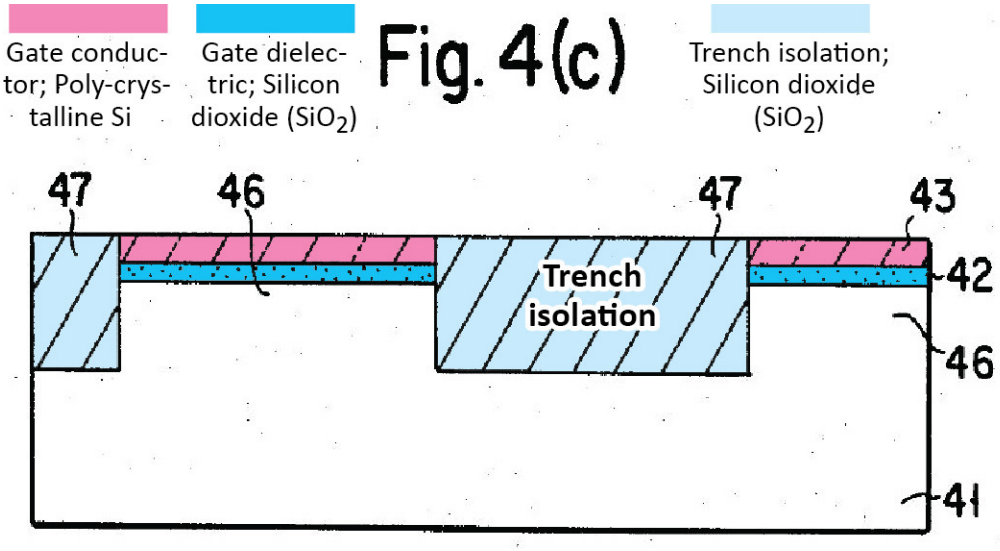
("polycrystalline silicon (Si) layer"). Exhibit 1010, 5:57-61. It is only thereafter, that the trench isolation (buried insulating layer **47**) is formed.

394. *Ogawa* states:

> A photoresist layer **44** is produced on the surface of polycrystalline silicon (Si) layer **43**, before a patterning process is applied to the photoresist layer **44** for the purpose of producing grooves along the area corresponding to the area in which a buried insulating layer is produced.

Exhibit 1010, Column 6:9-14, (emphasis added).

395. The STI process[34] concludes with a planarization step that leaves the wafer surface planarized or flat as shown in *Ogawa's* Figure 4(c), reproduced below (colorized).




[34] Although *Ogawa* does not use the term "STI", I use it here for convenience and consistency.

396. In summary, *Ogawa* forms the raised STI isolation feature only ***after*** depositing the gate dielectric film and gate conductor film. In this respect, both secondary references, *Ogawa* and *Noble* are alike.

The Petition Fails To Describe How *Lowrey* Could Be Combined With *Ogawa* To Render The Challenged Claims Unpatentable

397. The asserted combination of *Lowrey* and *Ogawa,* generally speaking, suffers from the same deficiencies as *Lowrey* in combination with *Noble*. Petitioner's superficial and technologically unwarranted approach fails to analyze the processes that would be required to merge *Lowrey* and *Ogawa*. Substantively, there has been absolutely no description of how the processes of *Lowrey* would allow for the introduction of a trench isolation, or if this could even be achieved. Indeed, it is clear that Petitioner's basic premise, i.e., to simply substitute *Ogawa's* trench isolation for *Lowrey's* LOCOS isolation, would not work.[35]

398. Petitioner contends that it would have been simple and obvious to a POSITA to follow the *Lowrey* process while substituting *Ogawa's* trench isolation for *Lowrey's* LOCOS isolation. Dr. Banerjee states:

[35] A POSITA would understand that a Si IC device must be fabricated by a functioning and reasoned sequence of fabrication steps. In the absence of such sequence (Petitioner provided neither pictorial nor narrative process sequence), a Si IC device having specific elements becomes meaningless.

> A person of ordinary skill in the art would have understood that combining the processes of *Lowrey* and *Ogawa* would have been a simple matter of replacing the LOCOS oxidation in *Lowrey* with the trench isolation of *Ogawa*. (*Schuegraf* at 2:20–22.) A person of ordinary skill in the art would have understood that replacing *Lowrey's* LOCOS with *Ogawa's* STI would have been entirely compatible and had no impact on the processes used for gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims. LOCOS and STI are both methods for forming insulating materials in the same locations of the substrate to perform the same function. They are both performed near the very beginning in device processing, and how the isolation regions are formed would not affect *Lowrey's* processes or the resultant device structures.

Exhibit 1004, ¶173.

399. ***First***, *Schuegraf* merely discloses that "Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type and is often considered an alternative to LOCOS isolation." (Exhibit 1009, 2:20-22; Petition, p. 23-24). Merely asserting that STI is an alternative to LOCOS does not provide any guidance on the difficulties and challenges encountered when making the STI-for-LOCOS substitution into the midst of a pre-existing fabrication process, such as

*Lowrey*.[36] As for the remainder of the above-quoted paragraph, no support is provided for the conclusions. This mistaken and unsupported assertion seems to be the entire basis for the asserted combination.

400. The incompatibility and unworkability of the references negates any motivation to modify *Lowrey* by replacing *Lowrey*'s LOCOS isolation with *Ogawa's* trench isolation. This lack of motivation renders *Lowrey* ineffective as the starting point of a validity challenge of the claims of the '174 patent.

401. ***Second***, it is not possible to simply start with *Ogawa's* trench isolation without first forming the gate dielectric and gate conductor because *Ogawa's* trench isolation formation relies on the availability of the gate dielectric and gate conductor. Thus, it would undermine the *Ogawa* process to go directly to trench isolation formation, and leave out the initial formation of the gate dielectric and gate conductor. Furthermore, the method used by *Ogawa* to planarize the trench isolation was an unreliable etching technique. Accordingly, it would not be possible to simply substitute the trench isolation in *Ogawa* for the LOCOS isolation of *Lowrey*, as Petitioner contends.

402. ***Third***, assuming, *arguendo*, that Petitioner (without having disclosed the actual processing sequence it envisions) would follow *Lowery* for the deposition of the gate dielectric and gate conductor *instead* of the gate dielectric

[36] In *Lowrey*, the LOCOS isolation is formed after three photomasking steps.

and gate conductor of *Ogawa*, in such case the interconnect could not be deposited simultaneously with the gate conductor as *Lowrey* contemplates.

403. *Lowrey's* process teaches the use of the same structural features for elements serving different purposes. That is, *Lowrey* explicitly teaches the use of the same elements for the gate conductor and interconnect conductor, while *Ogawa* employs different elements. Using different elements contradicts the teaching of *Lowrey*. Using different conductors for the gate and the interconnection, which is the key starting point of *Ogawa* as a precedent to forming the raised trench isolation, would result in a gate stack and interconnect stack having different heights because the interconnect would lack the gate conductor, which is present in the gate stack.

404. To somehow re-fabricate *Lowrey* in the *Ogawa* trench fabrication sequence would completely destroy the *Lowrey* structure and undermine its design because *Lowrey's* design would lose its hallmark feature of using the same layer stack for the gate and interconnect stack as indicated by the red dashed circles in the image below.

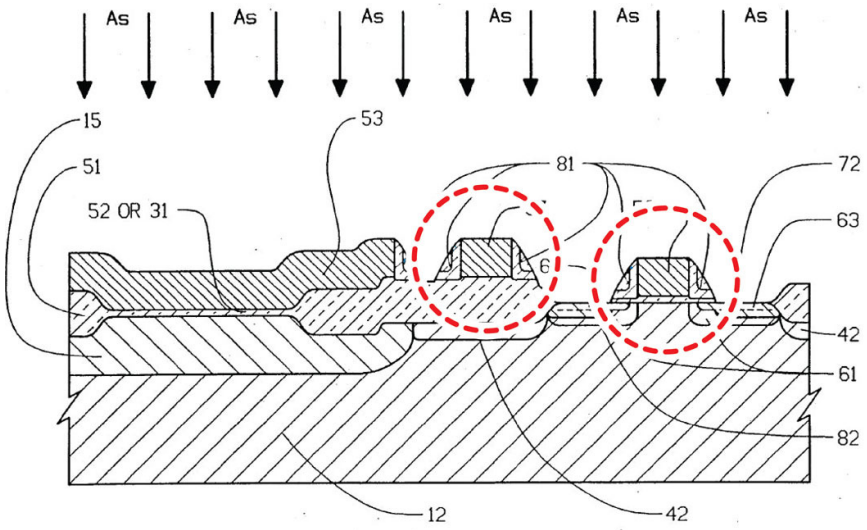



FIG. 8

405. For these reasons, a POSITA would not have been motivated to combine the two very different disclosures of *Lowrey* and *Ogawa*. Because the fabrication processes are incompatible, and because the combination would be non-functional, there would be no reason to combine the references. Moreover, to the extent that Dr. Banerjee is suggesting that a POSITA would have combined certain portions of *Lowrey* with certain portions of *Ogawa* in such a manner that it would render the claims of the '174 patent obvious, he seems to be conveniently picking and choosing elements from each reference in order to obtain a device that has all of the elements of the claims of the '174 patent, and not focusing on how a POSITA actually would have combined the references, if at all (and as stated above, they would not).

406. Tyler Lowrey, the lead inventor on *Lowrey*, was aware that trench isolation could be used in semiconductor devices to separate active areas before the filing of *Lowrey*. See paragraph 389.

*Lowrey* And *Ogawa* Do Not Suggest L-Shaped Sidewalls

407. Neither *Lowrey* nor *Ogawa* discloses L-shaped sidewalls, and thus, the combination would not disclose "first L-shaped sidewalls formed over the side surfaces of the gate electrode" or "second L-shaped sidewalls formed over the side surfaces of the interconnection." The sidewalls of *Ogawa* include a single structure shaped like a quarter circle (or ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. Ogawa discloses no sidewalls.

408. The sidewalls of *Lowrey* also include a single structure shaped like a quarter circle (or quarter ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. Although the figures in *Lowrey* show that the sidewalls have two structures, this is a result of convenience for the inventors of *Lowrey* in illustrating their invention, and not what is actually in the structure in *Lowrey*. In particular, *Lowrey* describes the formation of the sidewalls as follows. A "mini-spacer oxide layer **62**" is formed by a thermal oxidation or chemical vapor deposition (CVD). Exhibit 1017, 8:58-62. The purpose of the mini-spacer oxide layer **62** is to subsequently create lightly-doped n-type source/drain

regions **63** that are offset from the vertical boundaries of punch-through implant regions **61** by the mini-spacer oxide layer **62**. Exhibit 1017, 8:62-9:2. After the lightly-doped n-type source/drain regions **63** are formed, a "first spacer oxide layer **71**" is formed: "Referring now to FIG. 7, all circuitry is blanketed with a first spacer oxide layer **71** by one of various techniques (e.g., chemical vapor deposition)." Exhibit 1017, 9:3-5.

409. Note that layer **62** is made of "oxide" (e.g. thermal oxidation) and layer **71** is also made of "oxide" (e.g. chemical vapor deposition), where "oxide" refers to silicon dioxide or $SiO_2$. That is, both layers, **62** and **71**, are made of the same material, "oxide" and together form sidewall spacer **81**. Subsequently, the two layers are subjected to an anisotropic etch:

> Referring now to FIG. 8, first spacer oxide layer **71** and mini-spacer oxide layer **62** are etched with a first anisotropic etch, then optionally etched once again with a first isotropic etch to form a first set of sidewall spacers **81** for N-channel transistor gates **56**, N-channel interconnects 57 and the portion of polysilicon layer **53** which blankets the P-channel regions."

Exhibit 1017, 9:6-12.

410. The fact that both layers, **62** and **71** are made of the same material, "oxide", is significant. Given that layers **62** and **71** are made of the same material means that they are indistinguishable. That is, a microscopic assessment technique

such as scanning electron microscopy (SEM) in 1995 would show the two layers as an indistinguishable entity (Exhibits 2026 - 2030)[37] so that layer **62**, which Dr. Banerjee contends would be L-shaped, would not have the appearance of a capital letter L (or its mirror image). This is because layer **62** cannot be contrasted or distinguished from layer **71**. This is shown in *Lowrey*, which refers to the single element sidewall spacer **81**. Exhibit 1017, 9:6-12, Fig. 8.

411. A necessary condition for a feature to appear L-shaped is that it is distinguishable from surrounding features. Given that layer **62** is chemically indistinguishable from layer **71**, its physical appearance is indistinguishable from layer **71** as well. *See* sidewall spacer **81** depicted in *Lowrey* Fig. 8.

Summary

412. Petitioner has failed to provide the actual process sequence it is contemplating, i.e. Petitioner provided neither pictorial nor narrative process sequence. To properly establish obviousness, disclosure of the sequence is necessary. If Petitioner would have provided an actual process sequence based on *Lowrey* as modified by the trench isolation of *Ogawa*, it would become apparent to the POSITA that Petitioner's contemplated process would either (i) not be able to

[37] References both pre- and post- 1995 are supplied to show the common usage of this technique.

modify *Lowrey* by incorporating *Ogawa's* trench isolation without significantly deviating from the teachings of *Lowrey* and *Ogawa* in manner never suggested by Petitioner, or (ii) result in a non-functioning device.

413. Stated differently, in the cases of both *Lowrey* and *Ogawa*, the formation of the LOCOS isolation and trench isolation is intrinsically bound to the formation of the gate stack and interconnect stack, and in each case the respective formation process dictates the respective structures and formation process sequence. Petitioner's proposed substitution would have required considering only the two different *abstract* isolation structures (LOCOS isolation vs. trench isolation) while disregarding the gate layer stack and interconnect layer stack, something a POSITA would not have done.

414. Petitioner was required to address the consequences of altering the sequence of gate/interconnect/isolation formation and Petitioner has not done so. The gate and interconnect conductors associated with both types of isolation are integral to the isolation fabrication module, gate fabrication module, and interconnect fabrication module and dismantling these modules would unfavorably disrupt the entire fabrication sequence.

Petitioner Fails To Meets Its Burden To Establish That A POSITA Would Combine *Lowrey* with *Ogawa*

415. Without guidance, it is difficult or impossible to know exactly how Petitioner believes a combination of the *Lowrey* and *Ogawa* devices would look. However, just looking at the trench fabrication process of *Ogawa* the following steps would take place:

**Process sequence forming the *Ogawa* gate stack and interconnect:**

---

**Gate stack deposition / growth:**


**Silicon substrate**

**Trench etching:**

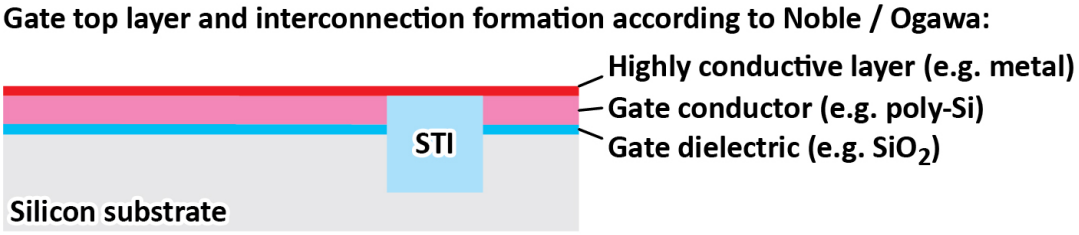
**Silicon substrate**

**Oxide deposition (trench re-fill):**

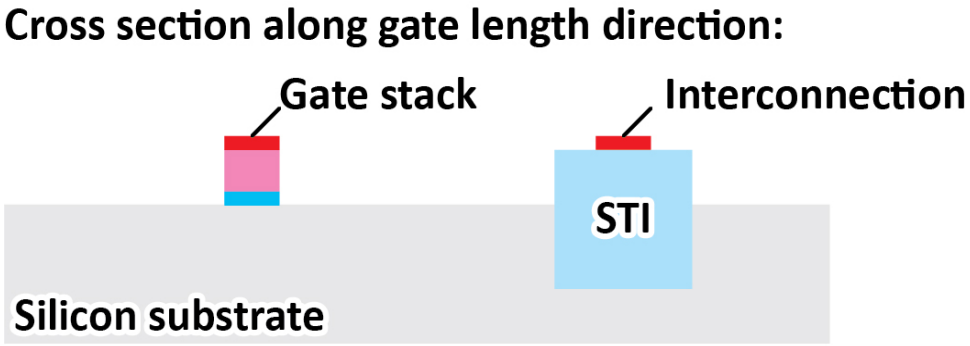

**Silicon substrate**

**Planarization ~~(e.g. by CMP):~~**


**Silicon substrate**

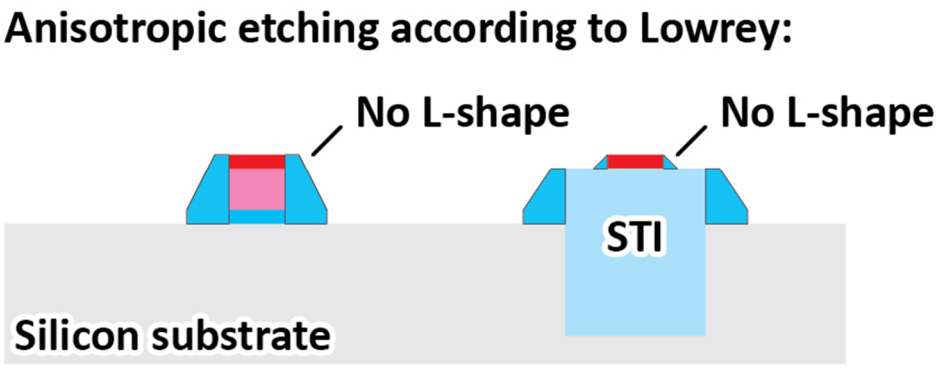



416. As shown above, *Ogawa* teaches first applying a gate dielectric and gate conductor, after which a highly conductive layer is applied. The highly conductive layer extends across the gate stack and the interconnection.



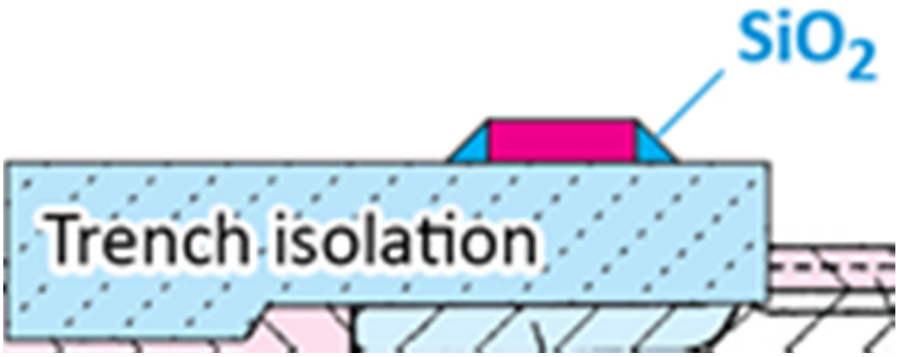

417. After etching, due to the height of the STI, it is seen that the lower two layers (blue-colored gate dielectric and pink-colored gate conductor) are part of the gate stack, but they do not extend above the STI and are otherwise etched away.

418. Then, as per *Lowrey,* the layers (**62** and **71**) are anisotropically etched to provide the structure below:




419. After anisotropic etching of the modified *Lowrey* device, it is seen that the interconnection is of such low height relative to the gate stack[38] that there is little opportunity for something resembling an L-shape to form and what forms is likely not much more than a nub or blob having no distinguishable shape. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall). This is how Figure 14 of *Lowrey* would likely look if a trench isolation as per *Ogawa* were substituted for the LOCOS isolation of *Lowrey*.

[38] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.




Conclusions Regarding The *Lowrey-Ogawa* Combination

420. For the above reasons, including the topology problem of *Lowrey*, a POSITA would not have been motivated to combine the two very different disclosures of *Lowrey* and *Ogawa*. Because the fabrication processes are incompatible, and because the combination would be non-functional, there would be no reason to combine the references. Moreover, to the extent that Dr. Banerjee is suggesting that a POSITA would have combined certain portions of *Lowrey* with certain portions of *Ogawa* in such a manner that it would render the claims of the '174 patent obvious, he seems to be conveniently picking and choosing elements from each reference in order to obtain a device that has all of the elements of the claims of the '174 patent, and not focusing on how a POSITA actually would have combined the references, if at all (and as stated above, they would not).

421. A POSITA would understand that a Si IC device must be fabricated by a functioning and reasoned sequence of fabrication steps. In the absence of such sequence (Petitioner provided neither pictorial nor narrative process sequence), a Si IC device having specific elements becomes meaningless.

422. Moreover, it appears that Tyler Lowrey, the lead inventor on *Lowrey*, was aware that trench isolation could be used in semiconductor devices to separate active areas before the filing of *Lowrey*. See paragraph 389.

423. The *Lowrey-Ogawa* combination is in my opinion insufficient to render the claims unpatentable because the POSITA would immediately recognize that *Lowrey* has a structure which is incompatible with the trench isolation of *Ogawa*. At the point where *Lowrey*'s LOCOS would be formed, substituting *Ogawa's* trench isolation requires planarization which will disrupt *Lowrey's* topology and render it non-functional. Conversely, the layers which would be necessary to form *Ogawa's* trench isolation would be incompatible with the pre-existing non-planar topology of *Lowrey*.

**Petitioner Fails To Meet Its Burden To Establish That *Lowrey* In Combination With *Ogawa* Renders At Least Claim 1 Unpatentable**

424. Claim 1 specifically recites a "trench isolation" which is absent from *Lowrey*. A POSITA would have no motivation to substitute the raised trench isolation of *Ogawa* for the LOCOS isolation of *Lowrey* for the following reasons:

i. The trench isolation of *Ogawa* cannot be substituted for the LOCOS isolation of *Lowrey* because such a substitution would involve planarizing a pre-existing device structure (having a non-planar topology) in a way which a POSITA would not have been motivated to do.

ii. Formation of the *Ogawa* trench isolation requires the prior deposition of two layers **14** and **116** which would be incompatible with the corresponding layers (gate dielectric layer and gate conductor layer) to be deposited in *Lowrey*.

Nothing Suggests That L-Shaped Sidewalls Would Form On The Interconnection

425. *Lowrey* has no L-shaped sidewalls on either the interconnection or anywhere else, and neither does *Noble/Ogawa*.

426. If one were to speculate on what Dr. Banerjee contemplated as the process for "importing" an STI into the device of *Lowrey*, even if Dr. Banerjee were correct that the sidewall **81** includes an L-shaped sidewall (he is not), Petitioner has not shown that the resulting structure would contain second "L-shaped sidewalls formed over the side surfaces of the interconnection." The reason is that the process of importing the trench isolation of *Noble/Ogawa* inherently requires that the gate insulation and gate conductor be applied first, and then have a

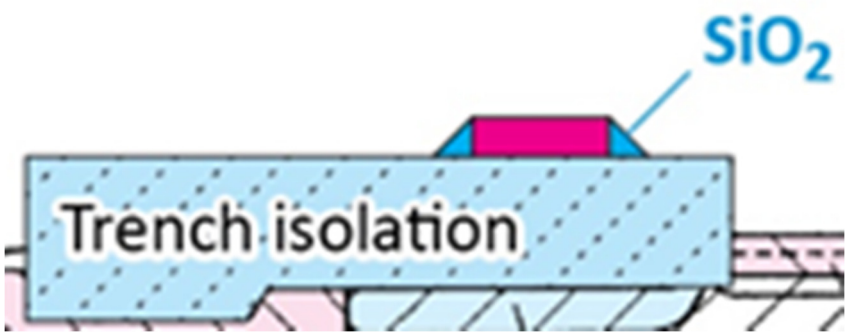
portion removed where the trench isolation will be inserted. As such, there would be no gate conductor electrode on top of the trench isolation.

427. The only reason such an electrode is present in *Lowrey* is that it was the result of laying down the gate stacks of the n and p-type transistors after forming the LOCOS isolation, but if these gate stacks are laid down as per *Noble*, i.e. before inserting the trench isolation, then there would not be a gate electrode on the trench isolation (STI).

428. Without a gate electrode on *Lowrey*'s trench isolation interconnection, when *Lowrey's* $SiO_2$ layers **62** and **71** (Fig. 7) are patterned into sidewall **81**, Petitioner has not shown that there would be sufficient height to the conductive wiring layer on the STI for an L-shape to form.[39] There is little opportunity for forming an L-shaped sidewall at the interconnect. Instead, what forms is likely not much more than a nub or blob having no distinguishable shape. It can be stated with certainty that the shape of the interconnection sidewall (i.e. second sidewall) will be different from the L-shape of the gate sidewall (i.e. first sidewall).

[39] The interconnect layer stack (element **140** in *Noble* and element **56** in *Ogawa*) is inherently thinner than the gate layer stack because the interconnect layer stack lacks the gate electrode layer.

429. An imaginary combination of *Lowrey* and the *Ogawa/Noble* devices would likely result in the interconnection shown below:



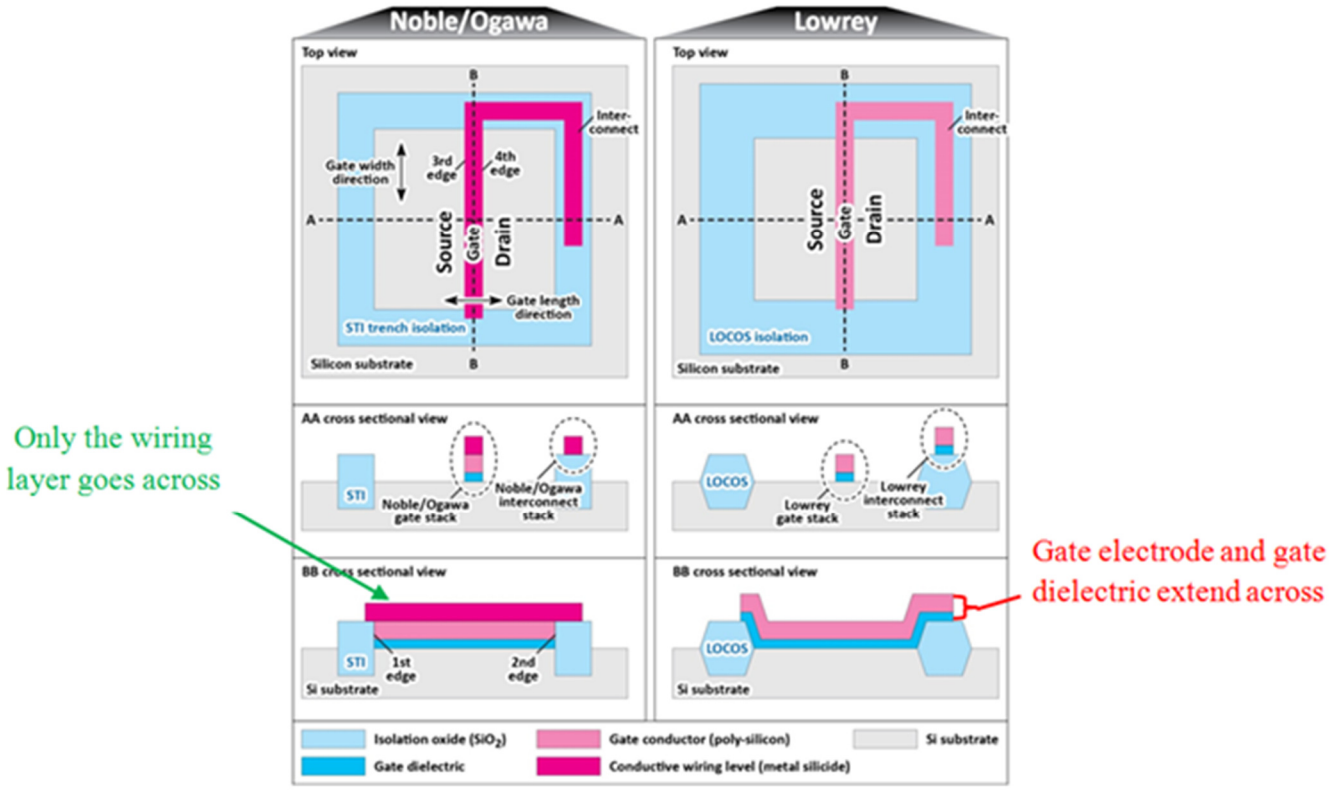

430. Given the reduced height of the interconnection it is highly unlikely that the same L-shaped sidewall would form and Petitioner has submitted no evidence to suggest what a combined device would look like, or whether L-shaped sidewalls would form on the interconnection.[40]

Conclusions Regarding Claim 1

431. *Lowrey* is not combinable with *Noble/Ogawa* because they lay down their isolation relative to the gate layer in opposite sequences which cannot be adapted to one another. If combined in some way, however, it has not been shown how the transplanted isolation trench with its accompanying surrounding gate electrode layer would impact the remaining *Lowrey* structure.

[40] Aside from the fact that *Lowrey* has no L-shaped sidewalls.

432. The depiction below shows the *Noble/Ogawa* structure on the left in contrast to the *Lowrey* structure on the right.




433. To the extent that Dr. Banerjee is suggesting that a POSITA would have combined certain portions of *Lowrey* with certain portions of *Noble/Ogawa* in a way he does not disclose to render the claims of the '174 patent obvious, he is using hindsight to pick and choose elements from each reference in order to obtain a device that has some of the elements of the claims of the '174 patent, rather than focusing on how a POSITA actually would have combined the references, if at all (and as stated above, they would not).

434. Even if pieced together as Petitioner may be proposing, then the final device would be lacking L-shaped sidewalls on both the gate electrode and interconnections since *Lowrey* does not teach final sidewalls, which resemble a capital "L," at either location.

435. Yet further, because of the limited height of the wiring layer on top of a modified hybrid device, there would be insufficient height to know whether L-shaped sidewalls would form on the interconnection.

436. Finally, Dr. Banerjee, although claiming that the combination of *Lowrey* with *Noble/Ogawa* would be possible and/or obvious, never shows how this combination would be done. His observations are entirely conclusory and lacking of any substance. Indeed, to the extent that he really believes that this could be done, he failed to provide a detailed explanation and a pictorial or narrative process sequence to illustrate his belief. Instead, Dr. Banerjee merely relies on a conclusory statement:

> Moreover, a person of ordinary skill in the art would have understood that replacing *Lee*'s LOCOS with *Ogawa's* trench isolation would have been entirely compatible and had no impact on the processes used for gate formation, source/drain formation, L-shaped sidewall formation, silicide formation, or any other aspect of the claims.

Exhibit 1024, ¶198.

437. The analyses provided herein establish that Dr. Banerjee's conclusory observations are baseless and wrong.

Dependent Claims

*Lowrey* In Combination With *Noble/Ogawa* Would Not Render Claims 4, 5, 8, And 16 Obvious

438. As explained above, *Lowrey* in combination with *Noble/Ogawa* would not render claim 1 obvious. For this reason alone, *Lowrey* in combination with *Noble/Ogawa* would not render claim 4 obvious, as well as claims 5, 8, and 16, which depend from claim 1.

*Lowrey* In Combination With *Noble/Ogawa* Would Not Render Claims 9 And 10 Obvious

439. To the extent that the Board relies on the prior art as teaching a level trench to be combined with *Lowrey*, claims 9 and 10 clearly distinguish in claiming a raised trench.

*Lowrey* In Combination With *Noble/Ogawa* Would Not Render Claims 11 And 12 Obvious

440. Petitioner points to *Lowrey* as teaching an interconnector formed of the same material as the gate electrode, but fails to take into account what the structure of the device would be if the trench isolations of *Noble* and *Ogawa* were substituted.

441. *Lowrey* in combination with *Noble/Ogawa* would not render claims 11 and 12 obvious because *Lowrey* in combination with *Noble/Ogawa* would not teach "the interconnection is composed of the same material as the gate electrode" or that "the gate electrode and the interconnection both have a polysilicon film".

442. *Lowrey* teaches that both the gate electrode **57** and interconnect **56** are made of doped polysilicon. Exhibit 1017, 8:42-44. However, as explained above, when forming the raised STI in *Noble/Ogawa*, *Noble/Ogawa* requires that the material for the gate electrode be deposited before the STI is formed, using the gate electrode as a rim (upper edge) to determine when to stop planarizing the wafer. Exhibit 1015, 5:55-57; Exhibit 1010, 6:16-22 and 7:31-49. Since the gate electrode is formed before the STI, the gate electrode cannot be formed on the STI. Instead, another deposition used to form conductive wiring **140** (*Noble*) **56** (*Ogawa*) on top of both the gate electrode and the STI is performed to form the interconnection. Exhibit 1010, 7:49-56); Exhibit 1015, 5:57-66. The wiring layer **140** is formed of a metal or a metal silicide or of heavily doped poly-silicon. Metals such as tungsten, molybdenum, titanium, or aluminum are suitable. Exhibit 1015, 5:61-65. The wiring layer **56** of *Ogawa* is molybdenum silicide. Exhibit 1010, 7:49-56. Thus, if a POSITA were to use the STI of *Noble* or *Ogawa* in the device of *Lowrey* (and they would not), the conductive wiring layers of *Noble* and

*Ogawa* would not "be composed of the same material" and not have "at least a polysilicon film".

443. Petitioner points to *Lowrey* as teaching this feature, but fails to address whether this feature would still be present if *Lowrey* is combined with *Noble* and *Ogawa*.

*Lowrey* In Combination With *Noble/Ogawa* Would Not Render Claim 14 Obvious

444. *Lowrey* in combination with *Noble/Ogawa* would not render claim 14 obvious because *Lowrey* in combination with *Noble/Ogawa* would not teach "the first and second L-shaped sidewalls are made of the same insulating film."

445. It would not teach second L-shaped sidewalls for the reasons stated above, namely that because the interconnect does not have a gate stack, there being only a conductive wiring level on top of the STI, Petitioner has not asserted that there is sufficient height to result in L-shaped sidewalls as a result of any subsequent patterning.

446. The sidewalls of *Noble/Ogawa* are not L-shaped but instead include a single structure shaped like a quarter circle (or ellipse) or a fan-shaped structure, and there is no component of the sidewalls that is L-shaped. That is to say, *Noble/Ogawa* does not disclose a sidewall that is substantially shaped like a capital letter "L" or its mirror image. The sidewalls of *Lowrey* also include a single structure shaped like a quarter circle (or quarter ellipse) or a fan-shaped structure,

and there is no component of the final sidewalls that is L-shaped. Although Figure 7 in *Lowrey* shows the sidewalls as having two layers **62** and **71**, once the layers are etched, layer **81** is a single layer sidewall, which is not L-shaped. Thus, there are no first or second L-shaped sidewalls in *Lowrey*, such that none of the references taken together teach this feature.

447. Given the relatively low height of the conductive wiring layer of *Noble* and *Ogawa* Petitioner has not shown that there would be L-shaped sidewalls on the interconnection.

Summary Of Argument

*Lowrey* and *Noble/Ogawa*

448. Petitioner has not met its burden of establishing invalidity by explaining how *Lowrey* and *Noble/Ogawa* would be combined to arrive at the claimed invention, as well as providing a definite resulting structure which meets the claim language.

449. *Lowrey* discloses a device which has LOCOS, and not trench isolation. Petitioner had the burden of establishing how, when in the fabrication process, and where, the trenches of *Noble/Ogawa* would be substituted for *Lowrey*'s LOCOS isolation. Petitioner has not done so.

450. Specifically, the fabrication process sequence of the LOCOS isolation of *Lowrey* is opposite to the fabrication processes of the trench isolation of

*Noble/Ogawa*. The isolation fabrication process will directly impact subsequent fabrication and ultimately the final device structure.

451. Petitioner points to "L-shaped sidewalls" in *Lowrey*, but did not meet its burden to establish that layers **62** and **71** (Fig. 7) continue to resemble an L-shaped sidewall in the final device.

452. Specifically, Petitioner has not met its burden to establish that when the two oxide layers are laid on top of each other they are sufficiently distinguishable such that there is a layer which substantially resembles a capital L or its mirror image.

453. Petitioner had the burden of establishing what the final structure of the interconnection (including "second" sidewalls) on top of the trench will be once it is substituted into *Lowrey* in order that this combined structure can be compared to the interconnection of claim 1. Petitioner has not done so.

454. Specifically, assuming that the Petitioner intends the substitution of the *Noble/Ogawa* trench isolations into the device of *Lowrey* in place of the LOCOS isolation, Petitioner has not explained whether the structure on top of the interconnection will contain a gate conductor (runner) and gate insulator.

455. Petitioner had the burden of establishing that in the final structure which Petitioner contemplates (but does not disclose) a POSITA would have found it obvious to provide second L-shaped sidewalls. They have not done so.

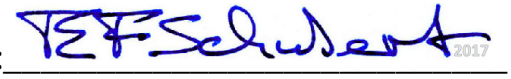
456. Specifically, if there is no gate conductor on top of the isolation trench which Petitioner has shown, Petitioner has not established whether and how second L-shaped sidewalls would be formed on the conductive wiring interconnection on top of the trench isolation. Absent the second L-shaped sidewalls of claim 1, as well as all the dependent claims, these claims are not invalid.

457. Petitioner has not shown the structure of the interconnection on top of the trench isolation which Petitioner would insert into *Lowrey*, and as such it is not possible to know whether the material of the interconnection on top of the trench isolation would be "composed of the same as the material" as the gate electrode (claim 11) or if both would contain "at least a polysilicon film" (claims 12). If it is not, Petitioner has not met its burden and claim 11 is not invalid.

458. Petitioner has not shown the structure of the interconnection on top of the trench isolation which Petitioner would insert into *Lowrey*, and as such it is not possible to know whether a second protection oxide film is formed between the interconnection and the second L-shaped sidewalls (claim 7) or whether those films would be L-shaped (claim 18). Petitioner has not shown the final device configuration, absent which each of these claims has not been shown to be invalid.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 24th day of March 2017, in Troy NY.

By: 

Dr. E. Fred Schubert

# APPENDIX A

**Curriculum Vitae**: **E. Fred Schubert**


***Contact information***

Department of Electrical, Computer, and Systems Engineering
Rensselaer Polytechnic Institute
110 Eighth Street, Troy, NY 12180
Telephone 518-276-8775 (office)
Email: EFSchubert@rpi.edu Homepage: http://www.rpi.edu/~schubert


| ***Year and place of birth*** | ***Home address*** | ***Marital status*** |
|---|---|---|
| 1956 | 17 Eaton Road, Troy NY 12180 | Married to |
| Stuttgart, Germany | Cell phone 518-253-3762 | Jutta M. Schubert |

***Education***

| | | | | |
|---|---|---|---|---|
| *University of Stuttgart* | Electrical Engineering | Vordiplom | (U. S. equivalent BSEE) | 1978 |
| *University of Stuttgart* | Electrical Engineering | Diplom Ingenieur (Honors) | (U. S. equivalent MSEE) | 1981 |
| *Oregon State University* | Electrical Engineering | Exchange Student | | 1977–1978 |
| *University of Stuttgart* | Electrical Engineering | Doktor Ingenieur (Honors) | (U. S. equivalent Ph. D.) | 1986 |

***Current appointment***

2002 – present: Distinguished Professor, Department of Electrical, Computer, and Systems Engineering; Rensselaer Polytechnic Institute, Troy NY

***Previous appointments***

2002 – 2015: Head and Founder of the Future Chips Constellation; Rensselaer Polytechnic Institute
2002 – 2015: Wellfleet Senior Constellation Professor, Future Chips (Chaired Professor); Rensselaer Polytechnic Institute
2002 – 2012: Professor Department of Physics, Applied Physics, and Astronomy; Rensselaer Polytechnic Institute
2008 – 2009: Director, Founding Director, and Principal Investigator, NSF Engineering Center for Smart Lighting, Rensselaer Polytechnic Institute
2002 – 2003: Adjunct Professor, Boston University
1995 – 2002: Professor, Boston University, Department of Electrical and Computer Engineering; Director of the Semiconductor Devices Research Laboratory; Affiliated Faculty of the Photonics Center.
1988 – 1995: Member of Technical Staff; Principal Investigator; and Member of Management at AT&T Bell Laboratories in Murray Hill, New Jersey
1985 – 1987: Post-Doctoral Member of Technical Staff at AT&T Bell Laboratories in Holmdel, New Jersey.
1981 – 1985: Scientific Member of Staff at the Max Planck Institute for Solid State Research in Stuttgart, Germany. Ph. D. Thesis title: "Modern Schottky gate field-effect transistors based on III–V semiconductors"

***Technical Achievements***

- First study of hot electron effects in selectively doped $Al_xGa_{1-x}As/GaAs$ heterostructures (1983)
- Demonstration and elimination of parallel conduction in $Al_xGa_{1-x}As/GaAs$ heterostructures (1984)
- First analysis of semiconductors doped with simultaneously shallow and deep donors (1984).
- Proposal and demonstration of the $\delta$-doped field-effect transistor. Short-channel effects in sub-micron field-effect transistors can be reduced to their theoretical minimum by using $\delta$-doped structures (1985)
- Development of the theory of alloy broadening in luminescence spectra of alloy semiconductors such as $Al_xGa_{1-x}As$. The current understanding of the low-temperature spectral linewidths of ternary and quaternary alloy semiconductors is based on this theoretical model. The publication analyzing the phenomenon of alloy broadening has been referenced far in excess of 100 times (1984)
- First demonstration of a light-emitting diode with a doping superlattice active region (1985)

- Application of δ-doping to selectively doped heterostructures; Demonstration of high-electron-mobility transistors with highest free electron concentrations; Analysis of structures by SEM, TEM, and SIMS (1986).
- Demonstration of delta-doped non-alloyed ohmic contacts with very low contact resistance and subsequent demonstration of self-aligned field-effect transistor with delta-doped non-alloyed ohmic contacts (1986)
- Demonstration of the spatial localization of dopants within 20 Å for a number of doping elements in delta-doped semiconductors including GaAs and Si for MESFET and MOSFET applications and the analysis of delta-doped structures by SIMS (secondary ion mass spectrometry) (with colleague Henry S. Luftman, 1983-1995)
- Significant improvement of the optical properties of doping superlattices by employment of delta doping. Improvement is demonstrated by the first observation of quantized interband transitions in the absorption (1988) and in the emission spectra (1989)
- First demonstration of tunable doping superlattice laser (1989)
- First quantitative analysis of the capacitance-voltage (CV) profiling technique in semiconductors with quantum-confined carriers. Demonstration that resolution of CV profiles in quantum-confined semiconductors is not limited to the Debye screening length (1990)
- Invention and demonstration a new concept by which heterojunction band discontinuities occurring between two different semiconductors are eliminated. The *elimination of heterojunction barriers* is based on parabolic compositional grading of doped heterojunctions. This concept is widely used in the fabrication of vertical cavity surface emitting lasers and other heterojunction devices (1991)
- Invention and first demonstration of resonant cavity light-emitting diode (RCLED) which uses photon quantization in microcavities to enhance the spontaneous emission properties (1992)
- Demonstration of giant enhancement of luminescence intensity in Er-doped $Si\text{-}SiO_2$ microcavities (1992)
- First demonstration of a resonant-cavity detector which is useful for wavelength-selective detection (1993)
- Demonstration of resonant-cavity light-emitting diode (RCLED) with very high brightness. The experimental brightness of the RCLED is five times higher than that of conventional LEDs. Based on calculations, the brightness of RCLEDs is expected to exceed that of conventional LEDs by more than a factor of ten (1994)
- Demonstration of delta doping in silicon for the fabrication of shallow junctions in scaled-down Si MOSFETs for integrated circuits (Si ICs) (with colleague Dr. H. J. Gossmann, 1990 – 1995)
- Invention of a new concept, *superlattice doping*, for enhanced p-type doping of GaN. All acceptors in GaN are deep, resulting in a low electrical acceptor activation of only 5 %. The new concept of superlattice doping is expected to increase the electrical activation of acceptors by more than a factor of ten (with post-doctoral associate Dr. W. Grieshaber, 1995)
- Investigation of yellow luminescence in GaN and the use of microcavity effects in Ag / GaN / sapphire structures to determine the refractive index of GaN (with post-doctoral associate Dr. W. Grieshaber, 1996)
- Demonstration of the first GaN / GaInN double heterostructure laser. The laser has cleaved facets and was optically pumped. Laser action was demonstrated by (*i*) a threshold in the light-versus-current characteristic, (*ii*) spectral narrowing below *k T* above threshold, (*iii*) a TE / TM polarization ratio greater than one hundred above threshold, and (*iv*) increased slope efficiency with increasing back-side facet reflectivity (with graduate student D. A. Stocker, 1997)
- Co-inventor of photonic-crystal light-emitting diode, PC-LED, jointly with group of Prof. John D. Joannopoulos at MIT (publication by Shanhui Fan *et al*. appeared in *Physical Review Letters* in 1997; US patent 5,955,749 was issued in 1999)
- First demonstration of crystallographic etching of GaN (with graduate student D. A. Stocker, 1998). The discovery, crystallographic etching, can be implemented by wet chemical etching, including photo-enhanced electrochemical (PEC) wet etching. The discovery is widely used in the LED industry to strongly enhance light extraction from LED chips and is found in LED light bulbs.
- Experimental demonstration of a ten-fold enhancement of p-type doping activation in $Al_xGa_{1-x}N$/GaN doped superlattices as compared to bulk GaN and $Al_xGa_{1-x}N$ (with graduate students D. A. Stocker and I. D. Goepfert, 1999)
- Invention and demonstration of the photon-recycling semiconductor light-emitting diode (PRS-LED) which emits *white* light and many other colors with very high luminous performance of > 300 lm/W (with graduate students X. Guo and J. W. Graff, 1999). Invention of the monolithically integrated GaInN/GaN PRS-LED (with graduate students X. Guo and J. W. Graff, 2000)

- Invention and demonstration of polarization-enhanced ohmic contacts in p-type and n-type GaN (with graduate students Y.-L. Li and J. W. Graff 2000)
- Invention and demonstration of AlGaInP light-emitting diode with omni-directional reflector (ODR) for high light extraction efficiency (with post-doctoral associate Th. Gessmann and graduate student J. W. Graff, 2001)
- Developed novel model for high diodes ideality factors ($n$ >> 2.0) in UV LEDs based on multiple rectifying elements (with graduate student J. M. Shah and Prof. Th. Gessmann, 2003)
- Developed theory for temperature coefficient of forward voltage in light-emitting diodes, particularly UV light-emitting diodes (with graduate student Yangang "Andrew" Xi, Dr. Jong Kyu Kim, and collaborators at Sandia National Laboratories, 2004, 2005)
- Invented highly efficient "remote phosphor configurations" in white light-emitting diodes (with Jong Kyu Kim, Hong Luo, and collaborators at SAIT-Samsung) (2004, 2005)
- Discovered whispering gallery modes in white LEDs with remote phosphors (with graduate student Hong Luo, Jong Kyu Kim, Yangang "Andrew" Xi, and collaborators at SAIT-Samsung, 2005)
- Developed new class of materials, low-refractive index materials, or low-$n$ materials, with an unprecedented low refractive index of $n < 1.10$; these materials are also suitable as low-$k$ materials for inter-metal-layer dielectrics in Si MOSFETs for integrated circuits (Si ICs) (with Dr. Jong Kyu Kim, "JQ" Xi, Professors Joel Plawsky, Bill Gill, 2005)
- Developed graded-index antireflection coatings that, unlike conventional anti-reflection coatings, have broadband omni-directional characteristics; the graded-index antireflection coatings use novel low-$n$ materials (with Jingqun "JQ" Xi, Jong Kyu Kim, 2007)
- Developed efficiency-droop reducing GaInN / GaInN and GaInN / AlGaInN LED active regions that were demonstrated to reduce the efficiency droop by as much as 40% (with Jong Kyu Kim, Martin F. Schubert, Di Zhu, Jiuru Xu, Mary Crawford, and Dan Koleske, 2009)
- Developed analytic model for efficiency droop based on drift-induced reduction of the carrier-injection efficiency (with Guan Bo Lin, Jaehee Cho, and others, 2012)

***Honors and awards***

- Google Scholar profile, including the Hirsch-index (h-index) can be found at < http://scholar.google.com > under profile "E. Fred Schubert"
- Elected to *Senior Member* of the *IEEE* "in recognition of professional standing" (1993)
- Recipient of the Literature Prize of the *Verein Deutscher Elektrotechniker* (*VDE*) for "Doping in III–V semiconductors" (Cambridge University Press, Cambridge, 1993). Citation: "The book concerns all aspects of doping in III–V semiconductors. Fundamental, practical, and technological issues of doping are addressed. The book covers the basic theory of shallow donors, shallow acceptors, deep levels, and their influence on the free carrier concentration. It also discusses doping during growth, epitaxy, diffusion, and ion implantation. In the field of semiconductor devices, the book emphasizes applications requiring highly controlled doping distributions. It is an excellent monograph equally suited for study, research, and industry" (1994)
- Elected as a member of the *Bohemian Physical Society* (Cornell University, Ithaca, New York). Citation: "For seminal contributions to the control of spontaneous emission by use of wavelength-size optical cavities, specifically the first demonstration in a glass host using rare earth implanted $Si/SiO_2$ resonant microcavities" (1994)
- Listed in "Who's Who In Science And Engineering" and "Who's Who in America" published by *Marquis Who's Who*, publishers of the original *Who's Who in America*. (*Marquis Who's Who*, New Providence, NJ) ISBN 0-8379-5755-9 (1996 – present)
- Elected to *Fellow of the SPIE* "For pioneering research in semiconductor doping and sustained contributions to the development of high-efficiency light-emitting diodes and lasers". According to the Society's bylaws, a Fellow "shall be distinguished through his achievements and shall have made outstanding contributions in the field of optics, or optoelectronics, or in a related scientific, technical, or engineering field" (1999)
- Recipient of the *Alexander von Humboldt Senior Research Award* of the Alexander von Humboldt Foundation, a Bonn-based non-profit organization promoting the exchange of scientific knowledge between German and highly qualified foreign scholars. According to the Alexander von Humboldt Foundation, academic qualification is the only selection criterion for the award. The award resulted in two extended visits with the Microoptics

Laboratory of Professor Jürgen Jahns at the University of Hagen, Germany (1999)

- Elected to *Fellow of the IEEE* "for contributions to semiconductor doping and resonant-cavity devices". According to the IEEE definition "the grade of Fellow is one of unusual professional distinction conferred by the Board of Directors only upon a person of extraordinary qualifications and experience" (1999)
- Listed in the "Dictionary of International Biography, 29th Edition" published by the *International Biography Center*, Cambridge, United Kingdom (2000)
- Recipient of the 2000 *Discover Magazine Award for Technological Innovation* presented by the *Christopher Columbus Foundation* in the category "Energy". The prize was awarded "for the invention and demonstration of the photon recycling semiconductor light-emitting diode", an all-semiconductor LED capable of emitting white light with very high efficiency, see < www.discover.com/awards > (2000)
- Recipient of the *RD100 Award* of the R&D Magazine that honors the "100 most technologically significant products of the year" (with Klaus Streubel of Osram-Sylvania Corp. and Rickard Marcks von Wurtemberg of Mitel Corp.). The prize was awarded for the "*Resonant-cavity light-emitting diode*" that uses enhanced spontaneous emission occurring in resonant cavities. The device is used in plastic optical fiber communication links, in telescopes for rifles, and many other applications (2000).
- Elected to *Fellow of the OSA* "for the invention and demonstration of the resonant-cavity LED and the photon-recycling semiconductor LED". OSA Fellows are elected by the OSA Board of Directors (2001)
- Recipient of the Boston University Provost Innovation Fund Award (Provost Dennis D. Berkey) valued at $ 25,000 for research and development of promising technologies (2001)
- Elected to *Fellow of the APS* "for pioneering contributions to the doping of semiconductors including delta doping, doping of compositionally graded structures resulting in the elimination of band discontinuities, and superlattice doping to enhance acceptor activation" (2001)
- Honored with RPI Medal as Senior Constellation Chair during Investiture Ceremony (2002)
- Received "2002 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (2002)
- Inducted as Wellfleet Senior Constellation Professor, Future Chips, Rensselaer Polytechnic Institute, November 21 (November 2003)
- Distinguished Lecturer of the IEEE Electron Devices Society (2003–2006)
- Elected member in Eta Kappa Nu (2004)
- "Best Oral Presentation Award" was won by Ph. D. student Hong Luo (who was the presenter), J. K. Kim, Y. A. Xi, J. M. Shah, Th. Gessmann and E. F. Schubert "Improvement of extraction efficiency of GaInN light-emitting diodes by employment diffuse omni-directional reflectors" *Connecticut Microelectronics & Optoelectronics Consortium (CMOC)*, 14th annual symposium, New Haven CT, March 17 (March 2005).
- "Best Student Poster Award" of the *International Semiconductor Device Research Symposium (ISDRS)* was won by Ph. D. student J.Q. Xi (who was the presenter), Jong Kyu Kim, Dexian Ye, Jasbir S. Juneja, T.-M. Lu, Shawn-Yu Lin, and E. Fred Schubert "Optical Thin Films with Very Low Refractive Index and Their Application in Photonic Devices", *International Semiconductor Device Research Symposium (ISDRS)*, Dec. 7 – 9, Bethesda, MD (December 2005)
- "MRS Silver Award" of the Materials Research Society was won by Ph. D. student Yangang Andrew Xi (who was the presenter), K. X. Chen, F. Mont, J. K. Kim, C. Wetzel, E. F. Schubert, W. Liu, X. Li, J. A. Smart "Extremely high quality AlN grown on (0001) sapphire by using metal-organic vapor-phase epitaxy" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (2006) Boston MA (December 2006)
- "25 Most Innovative Micro- and Nano-Products of 2007 Award" in July 2007 issue of *R&D Magazine* and *Micro/Nano Newsletter*. This recognition was given for the "Non-Reflective Coating" product that was published in *Nature Photonics* in 2007; full citation of publication: Xi, J.-Q., Martin F. Schubert, J. K. Kim, E. F. Schubert, Minfeng Chen, Shawn-Yu Lin, Wayne Liu, and Joe A. Smart "Optical thin-film materials with low refractive index for broadband elimination of Fresnel reflection" *Nature Photonics* **1**, 176, March 2007 (July 2007)
- "SCIENTIFIC AMERICAN 50 AWARD" of 2007, as published in the January 2008 issue of *Scientific American*. According to the *Scientific American Magazine*, this award "celebrates visionaries from the worlds of research, industry and politics whose recent accomplishments point toward a brighter technological future for everyone" (January 2008)

- "EDITORS' CHOICE" of *Science Magazine*, *Science*, Volume **319**, page 1163, February 29 (February 2008). This distinction was awarded for the publication: Jong Kyu Kim et al., "Light-extraction enhancement of GaInN light-emitting diodes by graded-refractive-index indium tin oxide anti-reflection contact" that appeared in *Advanced Materials* **20**, 801, 2008 (February / March 2008)
- Received "2008 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (2008)
- "Best Oral Presentation Award" won by David J. Poxson (who was the presenter), Frank W. Mont, Jong Kyu Kim, and E. Fred Schubert "Multilayer nano-structured anti-reflection coating with broad-band omni-directional characteristics" *Connecticut Microelectronics and Optoelectronics Conference* (*CMOC*), University of Connecticut, Storrs, Connecticut, April 9 (April 2008)
- "Best Oral Presentation Award" for presentation: David Meyaard, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Jong Kyu Kim, Daniel D. Koleske, and Mary H. Crawford "Temperature-dependent light-output characteristics of GaInN light-emitting diodes with different dislocation densities" *Connecticut Microelectronics and Optoelectronics Consortium* (CMOC) Symposium, New Haven CT, March 2 (March 2011)
- Identified as top 1% of patentees in the field of optoelectronics by study conducted by Professor Erica Fuchs of Carnegie Mellon University under a study supported by the US National Science Foundation (July 2011)
- Received "2012 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (November 2012)
- My "LinkedIn" profile was one of the top 10% most viewed "LinkedIn" profiles during 2012 (January 2013)
- My graduate student, Mr. Ming Ma, received the $ 30,000.00 Lemelson-Rensselaer Student Prize for the invention entitled "Graded-refractive-index (GRIN) structures for brighter and smarter light-emitting diodes"; The Prize is awarded annually by the Lemelson Foundation (March 2013)

***Service to the technical community***

- Current or former member of the *American Physical Society* (Member of the *Division of Materials Physics*, Member of the *Division of Condensed Matter Physics*), *Institute of Electrical and Electronics Engineers*, *Materials Research Society*, *Optical Society of America*, *Society for Optical Engineering* (*SPIE*), and the *Verein Deutscher Elektrotechniker*
- Co-author of hundreds of research articles, co-inventor of more than 30 United States patents, and numerous foreign patents (1981 – present)
- Gave many invited talks at scientific conferences organized by the *American Physical Society*, *Institute of Electrical and Electronic Engineers*, *Materials Research Society*, *SPIE* (*The International Society for Optical Engineering*), *Electrochemical Society*, *American Vacuum Society*, *Engineering Foundation*, and other professional societies (1985 – present).
- Co-editor (with A. M. Glass) of a Special Issue of the *Journal of Optical and Quantum Electronics* (Vol. **22**, 1990) on "Charge-transport assisted optical non-linearities in semiconductors" (1990)
- Symposium chair of the *American Vacuum Society Greater New York and New Jersey Chapter* on "Epitaxially grown semiconductors with atomic level control" (1991).
- Moderator of an Internet discussion on "Doping and Dopants in GaN" of the MRS Internet Journal (1995 – 1997)
- Member of review panels of the National Science Foundation (1995 – present)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1997)
- Technical work has been featured in popular journals, magazines and newspapers including the New Scientist, Discover Magazine, Wall Street Journal, Boston Globe, Focus, and on National Public Radio (1996 – present)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1998)
- Program Committee Member: IEEE IEDM, International Electron Devices Meeting (1999 and 2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (1999)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Berlin, Germany, March 5 – 10 (2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2000)

- Conference Chair and Co-Organizer of the TMS- and ONR-sponsored conference on "Doping, Dopants, and Low Field Carrier Dynamics in Wide Gap Semiconductors", Copper Mountain, Colorado, April 2 - 6 (2000)
- Chair, IEEE LEOS, Central New England Chapter. During my tenure as Chair, the Central New England Chapter won the IEEE LEOS Chapter award for the highest membership growth (1999 – 2000)
- Expert Witness involving semiconductor materials, devices, and packaging including elemental and compound semiconductors such as Si, SiGe, SiC, as well as III–V arsenides, phosphides and nitrides (1998 – present)
- Member of the Board of Governors, IEEE Laser and Electro-Optics Society (LEOS) (1999 – 2000)
- Member of the Optoelectronics Industry Development Association (OIDA) Roadmap Panel on Solid-State Lighting, Albuquerque NM Oct. 26 – 28 (2000)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2001)
- Panel Member of National Research Council meeting on "Solid State Lighting:" held at NAS and NAE, Washington DC, March 26 (2001)
- Program Committee Member of SPIE Photonics West conference on "Laser and LED Applications" chaired by Dr. Kurt Linden, San Jose CA Jan (2002)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose, CA (2002)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Cordoba, Spain, March 11–15 (2002)
- Program Committee Member for subcommittee on "Semiconductor lasers and LEDs" for OSA Conference on Lasers and Electro-Optics and Quantum Electronics and Laser Science Conference (CLEO / QELS) (2002 – 2003) Baltimore MD June 1–6 (2003)
- Reviewer for National Research Council of report entitled "Partnerships for Solid-State Lighting: Report of a Workshop" authored by the Board on Science, Technology, and Economic Policy. This report is forwarded to the US Congress for the initiation of a national Solid-State Lighting Initiative. (2002)
- Program Committee Member "Lester Eastman conference on high performance devices" University of Delaware, Newark, Delaware, August 6 – 8 (2002)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2003)
- OIDA Next Generation Lighting (NGL) Consortium. Member of "Light-Emitting Diode" Committee (2003)
- Program Committee Member, International Semiconductor Device Research Symposium (ISDRS) Washington DC, Dec. 8 – 12 (2003)
- Program Committee Member of "Display and Solid-State Lighting Devices" conference for OSA/IEEE Conference on Lasers and Electro-Optics (CLEO) (2003 – 2004)
- Elected Member of the IEEE Electron Device Society Administration Committee (IEEE AdCom) (2003 – 2008)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2004)
- Program Committee Member "Fourth International Conference on Solid State Lighting" August 2 – 6 Denver, CO (2004)
- Program Committee Member for the "Blue 2004: Advanced LEDs and Lasers Conference" Hsinchu, Taiwan, May 10 – 12 (2004)
- Conference Chair of SPIE Photonics West conference on "Light-emitting diodes: Research, Manufacturing, and Applications" San Jose CA (2005)
- Program Committee Member "International Semiconductor Device Research Symposium" December 7 – 9 Washington, DC (2005)
- Chair of "Display and Solid-State Lighting Devices" conference of OSA/IEEE Conference on Lasers and Electro-Optics (CLEO) (2005)
- Best Oral Presentation Award (Presenter: Hong Luo) at *Connecticut Microelectronics & Optoelectronics Consortium* (CMOC), 14th annual symposium, New Haven CT, March 17 (March 2005)
- Conference Chair of MRS Spring meeting "Symposium DD: Solid-State Lighting Materials and Devices" San Francisco, April 17 – 21 (April 2006)

- Member on the International Advisory Committee of *First International Conference on Display LEDs* (ICDL 2007), Seoul, Korea, January 31 to February 2 (2007)
- Member, Program Committee of *SPIE Photonics West* conference "Light-Emitting Diodes: Research, Manufacturing, and Applications XI" San Jose, CA, January 20 – 25 (2007)
- Program Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 20 – 25 (2007)
- Member, Executive Organizing Committee *SPIE Photonics West* conference "LASE 2007" San Jose, CA, January 20 – 25 (2007)
- Opto Track Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 21 – 24 (January 2008)
- Member, Program Committee, Light-emitting diodes: Research, Manufacturing, and Applications, SPIE Photonics West 2008, San Jose, California, January 19 – 24 (January 2008)
- Program Committee Member of the 7th International Symposium on Semiconductor Light Emitting Devices (ISSLED-2008) held in Phoenix, Arizona (USA), April 27 – May 2 (April 2008)
- Member, Program Committee, China SSL 2008, Shenzhen Convention & Exhibition Center, China, July 24 – 26 (July 2008)
- Member, Program Committee, International Workshop on Nitride Semiconductors, IWN 2008, Montreux, Switzerland, October 6 – 10 (October 2008)
- Opto Track Chair of *SPIE Photonics West* conference "Semiconductor Lasers and LEDs" San Jose, CA, January 25 – 29 (January 2009)
- Guest Editor of Special Issue on *Solid-State Lighting* published in the *IEEE Journal of Selected Topic in Quantum Electronics*, July / August edition (August 2009)
- Honorable Conference Chair, 6th China International Forum on Solid State Lighting (China SSL), Shenzhen Convention & Exhibition Center, China, October 14 – 16 (October 2009)
- Program Committee Member, International Conference on Nitride Semiconductors (ICNS), Jeju, South Korea, October 18 – 23 (October 2009)
- Program Committee Member, The Second International Conference on White LEDs and Solid State Lighting, Taipei, Taiwan, December 13 – 16 (December 2009)
- Editor, *Compound Semiconductors and Energy Applications and Environmental Sustainability*, Materials Research Society (MRS) Symposium Proceedings Volume 1167 (MRS, Warrendale PA, 2009)
- Conference Chair, OPTO, *SPIE Photonics West 2010*, San Francisco, California, January 23 – 27 (January 2010)
- Guest Editor of Special Issue on *Light-Emitting Diodes* published in the *IEEE Transactions on Electron Devices* (January 2010)
- Program Committee Member, *8th International Symposium on Semiconductor Light Emitting Devices* (ISSLED), Beijing, China, May 16 – 21 (May 2010)
- International Advisory Committee Member of the 16th *Microoptics Conference* (MOC'10) held in Hsinchu, Taiwan, sponsored and endorsed by OSA and IEEE/Photonics Society and organized by National Chiao Tung University, Oct. 31 to Nov. 3 (October 2010)
- Member of Academic Committee of *China Solid-State Lighting Conference* (CHINA SSL 2010) Shenzhen, China, October 14 – 16 (October 2010)
- Conference Co-Chair, OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Executive Organizing Committee OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XV *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2011 Conference on Lasers and Electro-Optics (CLEO), Baltimore, Maryland May 1 – 6 (May 2011)
- Member of the Academic Committee of the 8th China International Forum on Solid State Lighting (CHINA-SSL-2011) Guangzhou November 8 – 10 (November 2011)

- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XV *SPIE Photonics West 2012*, San Francisco, California, January 21 – 26 (January 2012)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2012 Conference on Lasers and Electro-Optics (CLEO), San Jose, California, May 6 – 11 (May 2012)
- Member of Academic Committee of the 9th China International Forum on Solid State Lighting (CHINA SSL 2012), Guangzhou, China, November 5 – 7, 2012 (November 2012)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XVI *SPIE Photonics West 2013*, San Francisco, California, 2 – 7 February 2013 (February 2013)
- Member of CLEO Subcommittee in the topic area: "Science & Innovation 15: LEDS, Photovoltaics and Energy-Efficient ("Green") Photonics" for the CLEO 2013 conference, April 28 – May 3, 2013 in Baltimore, Maryland (May 2013)
- Member, International Advisory Committee of the International Conference on Advanced Electromaterials (ICAE 2013) held on Jeju Island, Korea, from November 12 – 15, 2013 (November 2013)
- Program Committee Member, *Solid State and Organic Lighting* (*SOLED*), OSA Topical Meeting, 3 – 7 November 2013, Marriott Tucson Star Pass, Tucson, Arizona, USA (November 2013)
- Co-Chair, OPTIC International Conference, Chung Li, Taiwan, National Central University, December 5 – 7, 2013 (December 2013)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid State Lighting XVII" *SPIE Photonics West* 2013, San Francisco, California, 1 – 8 February (2014)
- Publication Committee Member, *5th International Conference on White LEDs and Solid State Lighting* (White LEDs), Jeju Island, Korea, May 25 – 28, 2014 (May 2014)
- Sub-Committee Chair of Track 6: Displays, Solid-State Lighting, Photovoltaics, and Energy-Efficient Photonics of *Asia Communications and Photonics Conference 2014* (ACP 2014). ACP is the largest and the most influential conference in Asia and Pacific Rim for communications and photonics technologies. ACP 2014, Shanghai International Convention Center, Shanghai, China, November 11 – 14 (2014)
- International Consultant of technical seminar of the 11th China International Forum on Solid State Lighting (SSL-China 2014) Guangzhou, China, November 6 – 8 (2014)
- Member of the International Advisory Committee of the 11th International Symposium on Semiconductor Light Emitting Devices (ISSLED 2017) held in Banff, Canada on October 8 – 13 (2017)

***Books***

- ***Doping in III-V semiconductors*** (author) Hardback and paperback, 628 pages (Cambridge University Press, Cambridge, UK, 1993). The following excerpt is from a book review by D. L. Miller, *University of Pennsylvania*, University Park PA, which appeared in *Physics Today*, Oct. 1994, p. 71: "[...] Fred Schubert has written a book that very nicely fills two roles: It serves as a reference volume for those of us who use III-V materials, and it provides enlightening explanations of interesting and important problems in semiconductor physics. [...] Schubert, who is employed by AT&T Bell Laboratories, brings his extensive research involvement with III-V materials physics straight to this book. His lucid explanations of some of the important physics of doped semiconductors is a major strength. For example, the chapter on deep centers provides the clearest treatment of the DX center I can remember reading, and it uses the large lattice distortion model and configurational coordinates introduced for the DX center to describe the EL2 deep level. This book can also serve as an excellent reference volume, because it briefly describes epitaxial growth techniques and the doping methods used with them, catalogs dopant-related phenomena, describes characterization techniques and provides 45 pages of citations to published articles and books. [...] I will use it to help my graduate students in the physics of semiconductors. [...] It will certainly be available on my bookshelf, in part to remind me what the Burstein-Moss shift is and in part for the literally hundreds of references that it provides on nearly every topic related to III-V semiconductor doping. Because of its clarity in treating some interesting phenomena of modern semiconductor physics, you too might want to get a copy of this book, even if you believe that Ga and As are just poor alternatives for doping silicon"

- ***Delta doping in semiconductors*** (editor) Hardback and paperback, 616 pages (Cambridge University Press, Cambridge, U. K., 1996)
- ***Light-emitting diodes*** (author) Hardback and paperback, 328 pages (Cambridge University Press, Cambridge, UK, 2003). The following excerpt is from a book review by David Bour, *Agilent Laboratories*, Palo Alto CA, which appeared in *Physics Today*, Nov. 2004, p. 66: "[...] In "*Light-emitting diodes*", E. Fred Schubert provides an excellent review of the physic and technology of semiconductor LEDs. […] Interesting anecdotes like [the first demonstration of electroluminescence], clearly written by someone with a broad perspective and expertise, appear throughout the book, making it enjoyable to read. […] Schubert provides an excellent description of the undesirable [non-radiative] recombination pathway. […] Schubert has made pioneering contributions to those devices, and this variety of LEDs may become more widely used in the future. […] Overall, "*Light-emitting diodes*" is an excellent examination of the physics and technology of semiconductor LEDs. The narration is simple and direct, and the book is well referenced for those seeking a deeper understanding of the topic. Written for the graduate level, the text will appeal to a broad audience; and for specialists who make semiconductor LEDs and laser diodes, it will serve as a useful connection to the scientific literature."
- ***Light-emitting diodes, second edition*** (author) Hardback, 422 pages (Cambridge University Press, Cambridge, UK, 2006)

***Courses and laboratories developed at Boston University***

- Developed first laboratory for "Physics of semiconductor devices" (SC-471) Fall (1998)
- Developed course "Quantum mechanics applied to semiconductor devices" (SC-574) Fall (1999)
- Developed course "Semiconductor light emitters" (SC-760) Fall (2000)
- Developed distance-learning course and NTU course on "Light-emitting diodes – Device physics and applications" Fall (2000)

***Courses taught at Boston University***

- Undergraduate Course "Physics of semiconductor devices" (SC-471)
- Graduate course "Fiber optic communication systems" (SC-563)
- Graduate course "Quantum mechanics applied to semiconductor devices" (SC-574)
- Graduate course "Introduction to solid state physics of devices" (SC-577)
- Graduate course "Quantum electronics" (SC-700)
- Graduate course "Integrated optoelectronics" (SC-770)
- Graduate course "Compound semiconductor devices" (SC-771)
- Graduate course "Light-emitting diodes" (SC-760)
- Graduate course "Research seminar" (SC-860, SC-892)
- Other courses "Research", "Guided Study", "Master Thesis", and "Dissertation" (SC-900)

***Courses taught at Rensselaer Polytechnic Institute***

- Graduate Course "Semiconductor devices and models II" (ECSE-6290)
- Undergraduate course "Microelectronics technology" (ECSE-2210)
- Undergraduate course "Fields and Waves 1" (ECSE-2100)
- Graduate course "Quantum mechanics applied to semiconductor devices" (ECSE-6968)
- Graduate course "Physical foundations of solid-state devices" (SC-6960)
- Graduate course "Light-emitting diodes and solid-state lighting" (SC-6961)
- Other courses "Research", "Guided Study", "Master Thesis", and "Dissertation"

***Teaching evaluations and students' comments***

(**1997**) Students have made the following comments: Clear … organized … excellent explanations … I've never had a professor like him – I wish all are like him … very clear and concise presentation … strong response to students questions and concerns … Professor provided excellent notes … laid out lectures in a clear and precise manner which worked out wonderfully … well organized and confident … responsive to students' concerns … excellent for students going into semiconductor industry … excellent hand-outs and course materials … well prepared … clear

lectures … I was strongly encouraged … materials is very interesting … hand-outs were excellent … material is very important … presentation of materials was very clear … hand-outs were excellent support to the class … efforts made by Prof. Schubert in keeping everyone at the same pace was remarkable …

(**1998**) Professor was always well prepared … excellent content … very relevant for the field of solid state devices … excellent preparation for the class … handouts were very good … very well organized teacher … excellent knowledge of material … provided complete background of all material … easy to talk to … excellent overall teaching skills … really enjoyed coming to class … his choice of topics and homework helped me a lot … enthusiastic in teaching and helpful during the office hours … one of the best professors I have had at BU … course gave a very good overview of the different solid state physics principles … course was very well organized … relevant examples and homework were given … good explanations were given … presented clearly … presentation was clear … communicated effectively … very knowledgeable … good demonstrations in class … gives clear descriptions … asks questions of class … grades homework fairly … good at answering questions … no weak points … excellent instructor and scientist … inspiring professor … thorough … instructor is very precise and well prepared … his knowledge of the material is exact … very responsive to feedback … encourages student questions, class participation and discussion … instructor cared about whether students understood material … instructor used applications immediately after showing theory … handouts were excellent … guest lecture and lab tour excellent idea … excellent class notes … presented topics neatly … well prepared … review of ongoing research topics was great … Professor Schubert is undoubtedly an expert in his area …

(**1999**) He enjoyed teaching the material and was very clear … presentation of the material in class was excellent … he helped me to understand a lot about semiconductors … Prof. Schubert always tried to make sure that we would all have a clear understanding of the material … manuscripts were very helpful … encouraged lots of class participation and was always readily available for help … presentation was excellent … instructor was always willing to help me … very helpful … clearly, Prof. Schubert is more than just extremely knowledgeable about this material … very thorough and exact communication of points … excellent course packet written by instructor … he was very well prepared for class … He is extremely fair and encourages participation … he is also very accessible … excellent instructor … very approachable and easy to ask questions of … handouts were very effective and helpful … Prof. Schubert is very prepared and concepts are well explained … [materials] will be very useful for my future … very open to questions …

(**2000**) He did a lot of experiments which really helped … material is very interesting and cutting edge … clear presentations … good in-class demonstrations … very clear lectures … the material really does challenge you … takes the time to answer your questions … very interesting material … relevant to today's world of communication … field trip was fun … in-class demonstrations really added to class … good understanding of course material … excellent details, willing to help, good explanations … in-depth details on quantum mechanics … instructor was extremely accessible to students … he encouraged participation in class … he gave intuitive arguments and explained concepts in a very physical way … I very much enjoyed Professor Schubert and would like to take more classes with him … material was very beautiful … I very much enjoyed the papers that were discussed … everything is well organized … hand-out material is very complete and clear … lectures are clear … professor prepared an excellent manuscript … explained things very clearly … he has strong enthusiasm to solve students' questions … it's a very important course … Professor follows the course notes exactly, so one can concentrate on material without having to focus on details … clearly presented material … course is great preparation for future courses in solid state … I greatly admire Professor Schubert …

(**2001**) He has thorough understanding of subject … I like the fact that he shows us examples in class demonstrations … manuscript was good … instructor provides good notes … materials are presented clearly … in this course you learn a lot … very illustrative and in depth … very interesting course … Professor presented material well … Professor seemed to have strong grasp on what he was teaching … the basics were presented correctly … smooth transition into more complex materials … presented basics well … Professor's strong points are knowledge, organization and class materials … clear conception … very important and useful class … Professor knew what was going on … manuscript and his notes were very helpful … responded to suggestions … notes were comprehensive … just fine … manuscript was good … knows the material very well … notes handed out are good … expert knowledge of material … developed lectures logically and straightforward … lecture notes were prepared for us - very nice touch … Professor has deep knowledge of the materials … Professor is always prepared for lectures … he emphasizes principles and the concepts … good preparation … good stuff and clear presentation … good research and industry experience … excellent handout notes and materials … excellent teaching skills …

inspires the interest of students … great knowledge of material … well organized course notes … Professor Schubert gave very clear instructions … listening to his presentation is a true enjoyment of an excellent art of lecture style … manuscript has quality of excellent book … manuscript was excellent reference source book … instructor was very clear and well organized and encouraged participation … text [written by Schubert] was extremely good … expert knowledge of materials … class demonstrations were very beneficial … can clearly relate complex ideas – very good … has a high amount of patience … excellent understanding of material … very enthusiastic in teaching … always available for discussion … very knowledgeable … I don't see any weak points … he explains the theory very clearly …

(**2002**) Always prepared … presented difficult material in a manner that was easy to understand … presented everything neatly … very helpful and organized … presents subject in an very easy and friendly format … very well qualified … great experience … very detailed notes … well organized … very useful … very good diagrams and explanations … he knows the material extremely well … notes given to us are extremely helpful … professor was very knowledgeable … was able to answer any of our questions … very informative course … very knowledgeable and a great teacher … instructor is enthusiastic to teach students … instructor can explain theory very clearly …

(**2003**) Great overall knowledge … good organization skills … demonstrations were very interesting and useful … effective instructor … handouts were extremely useful and organized … good course for completely understanding many points of fiber optics …

(**2004**) SPIE short course: … encouraged questions and handled them well … excellent short course … I really appreciated and enjoyed this course … good course – covered very broad matter … the instructor was very knowledgeable on the topic … excellent! … RPI Semiconductor devices and models II (ECSE 6290): Overall excellence of teacher: 4.8 (average 4.2). Overall excellence of course: 4.6 (average 3.9). Comments: … course was very well prepared … [course] was very organized … this is an excellent course … I learned a lot from this course … course was very good … thanks Prof. Schubert for a wonderful course … it's been a great course … thank you … RPI Microelectronics Technology (ECSE 2210): Overall excellence of teacher: 4.7 (average 4.2). Overall excellence of course: 4.3 (average 3.9). Comments: … understandable presentation … great job [of] Prof. Schubert … very nicely done class … very helpful throughout the entire course … provided timely explanations to complicated material … very informative … course was fun and interesting … very interesting lecturer … very down to earth and easy to ask for help … [instructor] did a good job in presenting [material] … good course … fun course … excellent instructor … he is a great guy and very knowledgeable (RateMyProfessor.com) … I would definitely take a class from him again (RateMyProfessor.com) **Book review** by Neal Oldham (San Jose, CA, USA) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (May 17, 2002): [This is the] best book I've encountered in the semiconductor field. This is, no question, the best book that I've encountered in the entire field of semiconductor physics. It is expertly organized and indexed, easy to follow, complete in its treatment of electrical and materials-science aspects of III-V semiconductor production and measurement, well-written ... worth every penny if you even have the most remote interest in the subject. **Book review** by Debdeep Jena (Santa Barbara, CA, United States) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (July 6, 2001): Very useful text for semiconductor crystal growers. Doping is a big, big issue in semiconductors; this text does appreciable justice in its treatment of the issue. In addition, Schubert treats heterostructure physics appreciably well (in fact better than many textbooks on semiconductor physics!). Perusal of this book has proved very rewarding for me, and I expect it will do the same wonder for you too.

(**2005**) SPIE Photonics West short course: … very good instructor! … very knowledgeable … clear on complex subjects … good job fielding questions … (numerical score 4.3 out of 5.0). Educational materials on the web: … I have greatly enjoyed your LED slide show. CLEO short course: … very good and well organized course! ECSE 6968: … class presentations were very helpful in learning … very useful in learning the details of fundamental concepts … course is very good … course is excellent for engineers … your […] treatment brought about a much better understanding … examples were great and helpful … [discussion of] history and photons […] helped increase interest … after your course now, I can actually approach a quantum mechanics text book without fear … overall, I just wanted to say – thank you … excellent course … instructor made it interesting and taught very effectively … manuscript provided was also very well written … class was excellently structured … will benefit my studies in the future … especially liked the term paper requirement … Prof. Schubert is an excellent instructor, who is well prepared (improved student attitude: 4.6 out of 5.0; overall excellence of teacher: 4.8 out of 5.0; overall excellence of course: 4.8 out of 5.0). SPIE Photonics North short course: … very good and clear in presentation … (numerical

score 4.4 out of 5.0). ECSE 6960 mid-course and final feedback: … Professor has provided all course materials … really appreciate it … well presented … technical support was great … my learning experience has been good … responses to my homework questions have been very timely … I have enjoyed the course and found it interesting and useful … homework assignments has been extremely beneficial … set of notes is very comprehensive … good class structure … (improved student attitude: 4.4 out of 5.0; overall excellence of teacher: 5.0 out of 5.0; overall excellence of course: 4.6 out of 5.0). Comment on web educational materials: … notes look very thorough and clear …

(**2006**) SPIE Photonics West short course: … excellent, knowledgeable … excellent presentation … (numerical score 3.91 out of 5.0). ECSE 6961 (Light-emitting diodes and solid-state lighting) mid-course and final feedback: … excellent: informative, comprehensive and interesting … the best part of this course, in terms of my learning experience, has been the course materials … just an outstanding class … so much is newly discovered and so much is current on-going research and commercially relevant … Dr. Schubert is obviously a leading researcher and did a great job of conveying his experience and understanding to the class … a highly technical topic that still makes a good general conversational topic … I liked the course material … I liked the fact that Prof. Schubert lectured directly from the textbook … I liked the structure of the course … I learned a lot about lasers and LEDs and other optical devices … it is a basic and fundamental class … instructor gives ideas, concepts, and samples very clearly … very good course … students interested in LEDs and solid-state lighting are strongly recommended to take it … liked the overall coverage … teaching pace was good … he covered a lot of material that is important for the subject, but it was clearly always related to the topic … the manuscript that he let us use was excellent in my opinion … the most important thing I liked about the course was the course material and the structure of the course … right amount of homework and the two exams and the term paper presentation … it was great to learn this course from someone who is a world leader in this field … well-organized material … liked the course format … organization was good … allowed me to know exactly what we were covering so I could look through the material prior to the lecture … course content was good, starting with LED basics and covering materials through modern technologies, and then a look at solid-state lighting and sort of an intro to communication devices … good fundamentals in LEDs … GREAT Professor … awesome course … informative course … ability to view course online was helpful … very fruitful course … covering a lot of materials … very good and very important for graduate students to take this one … for people in industry it's also useful … for the instructor, this course is thought through very clearly … the text book is also very good … great course … excellent instructor … cute instructor … course is very good … I benefited a lot from it … (numerical scores: excellence of teacher 4.7 out of 5.0; excellence of course 4.4 out of 5.0; overall average of ratings 4.6 out of 5.0). ECSE 2210 (Microelectronics Technology) … excellent teaching method … I like that the Professor asks random questions at the end of class – it helped me understand the subject better … I thought Prof. Schubert was fabulous … his organization of the class encouraged learning … I highly recommend this class to everyone … a devoted and involved teacher … displayed more enthusiasm in teaching than other Professors I had … he also seemed to have a philosophy about teaching that was beyond helping students get good grades … he emphasized real-world applications of material and had general advice about working in the real world after leaving academia … helpful … though he was harder in grading and exams, Prof. Schubert challenged us more and made the course more interesting … the many class activities provide lots of practice of materials just learned … provided good back-up information … made sure students understood concepts …thank you for asking students questions during class to reinforce concepts … thank you for allowing open book exams … (numerical scores: excellence of teacher 4.4 out of 5.0; excellence of course 4.3 out of 5.0; overall average of ratings 4.4 out of 5.0)

(**2007**) Book review by Steven J. Wojtczuk (Lexington, MA, USA) on "Light-Emitting Diodes" (E. F. Schubert, Cambridge University Press, Cambridge UK, 2003) on amazon.com (March 14, 2006): … Schubert (RPI) has written an excellent book on LEDs that manages to explain and derive simple quantitative models for many phenomena of current interest … many monographs are a compendium of results in the field with hundreds of references … in contrast, Schubert, while giving copious references, is the sole author, leading to a coherent presentation well suited to learning … there are plentiful and good figures and drawings, as well as many exercises and solutions integrated into the text … SPIE photonics West Short Course: … excellent talk … ECSE 2210 (Microelectronics Technology) … thank you … great course … excellent instructor … interesting course … appreciated that you did not lecture completely from the slides and that you probed the class to ensure that we were understanding the key points … course is fine … good professor … Professor Schubert is one of the best lecturers I had … the pace at which he moves the topic, the way he explains things, and the manner in which he asks students questions all came

together to help me learn much more form his lectures than I could on my own … instructors are absolutely very intelligent … Professor Schubert was a good professor … I actually learned things when Professor Schubert taught … ECSE 6968 (Physical Foundations of Solid-State Devices) … the instructor explained every concept in a very simple and effective manner … I really enjoyed taking this course … (numerical scores: excellence of teacher 4.5 out of 5.0; excellence of course 4.5 out of 5.0; overall average of ratings 4.5 out of 5.0)

(**2008**) SPIE Photonics West short course feedback: … very good … clear … very nice … answered questions readily … (numerical score 4.25 out of 5.0) … ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback: … It was great for me to have the opportunities to take two consecutive classes, *Physical Foundation* and *LEDs*, from you … both these classes have taught me a lot … they were very well organized … thank you for all the help … I have really enjoyed your classes … relevant material … very good professor … (numerical scores: excellence of teacher 4.3 out of 5.0; excellence of course 4.3 out of 5.0; overall average of ratings 4.3 out of 5.0) … Internet educational materials feedback: … I recently came across your course notes while trying to get a basic understanding about semiconductors and I wanted to thank you. Your notes for course "ECSE-2210 Microelectronics Technology" are the most useful and informative thing I have found on semiconductors on the Internet. I'm a chemist by trade and this is a great introduction for me … 2007 Chautauqua Short Course and High School Teacher Summer Course, held at RPI June 26 and July 12, 2007 (numerical average of scores: 9 out of 10) … ECSE 6968 (Physical Foundations of Solid-State Devices) feedback: … Prof. Schubert is one of the best professors I've ever had … his ability to explain difficult and complex materials in a clear and concise manner is unmatched … the presentations, although time consuming, I felt were a great idea … thanks for your efforts professor! … I have really enjoyed taking this course … By email: … thank you professor … it has been a pleasure taking this course with you … (numerical scores: excellence of teacher 4.4 out of 5.0; excellence of course 4.4 out of 5.0)

(**2009**) SPIE Photonics West short course feedback: … one of the best short courses I have taken … it was very nice to hear about the history of LEDs … very interesting but also very theoretical … (numerical score 4.10 out of 5.0). ECSE 2210 (Microelectronics Technology) … great course … instructors were excellent … encourages students to stay up to date with the subject matter … thanks for this well-organized class … [the instructor] tries to get students come out with the best grade possible … this was a good class … ECSE 6968 (Physical Foundations of Solid-State Devices) feedback: … it is really an excellent course … clear hand script … great professor! … (numerical scores: excellence of teacher 4.6 out of 5.0; excellence of course 4.7 out of 5.0)

(**2010**) SPIE Photonics West short course feedback: … good to get the latest data and charts … very good … very broad course and well organized … it was great … (numerical score 4.04 out of 5.0) … ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback: … a good course … this was a wonderful course … it has given me a lot of understanding … the course has inspired me to take up LED research … useful … straight forward … very good advisor … good course … (numerical scores: excellence of teacher 4.3 out of 5.0; excellence of course 4.2 out of 5.0) … ECSE 6220 (Physical Foundations of Solid-State Devices) feedback: … overall excellent course … Professor Schubert is a good teacher … he can explain every discipline very clearly and relate them to practical applications … I like his teaching style very much … overall, it was a nice course … material explained in a clear organized manner … (numerical scores: excellence of teacher 4.7 out of 5.0; excellence of course 4.3 out of 5.0)

(**2011**) SPIE Photonics West short course feedback: "… very nice overview … instructor was excellent! … very good instructor … I would recommend lengthening to 6 hours … excellent presentation, materials and text … thanks … very clear and easy to follow … to be recommended … excellent presentation … good compromise for a person with a busy schedule …" (numerical score 4.45 out of 5.0); … ECSE 2210 (Microelectronics Technology) "… this was a great course … I enjoyed Professor Schubert's views … I was successful … this course was taught very well … this subject I now find quite interesting and am no longer intimidated by it … I liked the material of this course … thank you …" (numerical scores: excellence of teacher 3.3 out of 5.0; excellence of course 3.2 out of 5.0); Feedback on book *Light-Emitting Diodes*: I am a graduate student from National Chiao Tung University, Taiwan … your wonderful book *Light-Emitting Diodes*, both first- and second- edition, gave me a lot of information and help … I would like to ask when can the third of the masterpiece be published? I wish I can get it as soon as possible and study more about the lighting devices; Feedback on Internet pages: I found your website and information […] quite enlightening and provides a great start … I simply wish to quickly express my thanks and gratitude. Feedback on book *Physical Foundations of Solid-State Devices*: Dear Prof. Schubert, I have read your book Physical Foundations of Solid-State Devices and I must say it is amazing the explanations are really good and I am most thankful that you have decided to put the book online thank you. Itamar Jade Balla, The Israel Institute Of

Technology. Feedback on book *Light-Emitting Diodes* by Trung Nguyen (San Jose, California): It is a good book about Light Emitting Diodes (LEDs). It provides very good info and it is a good reference for engineers who work in LED field; … ECSE 6220 (Physical Foundations of Solid-State Devices) feedback: "… amazing course … great instructor … very good course … the text and lectures were very useful and informative … I definitely learned a lot from taking this course … I liked the course materials! …" (numerical scores: excellence of teacher 4.6 out of 5.0; excellence of course 4.5 out of 5.0)

(**2012**) Feedback on Internet-based materials: "I'm Cheng Liu [Wuhan National Laboratory for Optoelectronics, China], currently a graduate student major in Physical Electronics … I deeply admire your profound knowledge on this field and your unselfish sharing of it …" ; … SPIE Photonics West short course feedback: … Dr. Schubert was very clear and very patient with people who had questions … the materials were comprehensive … ; Feedback on Internet-based materials: "… supremely-rich course contents posted on your website. Thank you very much for showing such awesome materials for the world to see …" (Prof. Natee Tangtrakarn, Thailand) … ECSE 6962 (Light-Emitting Diodes and Solid-State Lighting) feedback: "… very interesting course … Professor Schubert did a great job explaining the material … his textbook is very clear and understandable … nice course … I learned a lot of new things by taking it …" (numerical scores: excellence of teacher 4.7 out of 5.0; excellence of course 4.7 out of 5.0)

(**2013**) ***SPIE Photonics West short course*** feedback (SC-052, Light-Emitting Diodes): "… Great instructor with admirable combination of knowledge in academic and commercial knowledge … I appreciated the depth of his knowledge and experience … length of the course was good … Overall this was an excellent course … Thank you … course is very easy and I understand easily … Excellent course! … Instructor was fantastic -- clear, explicit, took questions as we went and answered well … One of the best SPIE courses I've taken (and I've taken lots)! … Great course -- thanks! … I was happy that the slides were updated with 2012 data". ***RPI course numerical scores (ECSE-6962, Light-Emitting Diodes and Solid-State Lighting)***: The instructor's presentation is clear and understandable: 4.67 out of 5.0; The instructor is aware of students' understanding or difficulties: 4.5 out of 5.0; The pace of the class is appropriate: 4.33 out of 5.0; The instructor adequately covers ways of applying discussed theories or methods to actual, real-world engineering systems: 4.50 out of 5.0; Verbatim comments: "… The course is pretty good … needs no improvement … I can appreciate the more wide-angle approach from the course … These areas are very important and previously I had no knowledge of them … It was a pleasure attending your class …" ***RPI course numerical scores (ECSE-6968, Physical Foundations of Solid-State Devices)***: Excellence of course: 4.83 out of 5.0; Excellence of instructor: 4.83 out of 5.0; Verbatim comments: "It has been an awesome experience of learning for me in this course ... Thanks you for everything ... Thank you for the great semester ... Have a good break ... Thank you for the great semester ... Have a good break ... Professor, thank you for an engaging and interesting class this semester ... I enjoyed the subject of my paper and learned quite a bit particularly about GaN, which I had not had a chance to really do any research into before ... Very good and interactive class ... I liked the style of the class ... I thought the topics covered were very interesting ... I think I got much more out of the class this way than if we would have followed the manuscript chapter by chapter."

**(2014)** ***SPIE Photonics West short course*** verbatim feedback (SC-052, Light-Emitting Diodes): "Very knowledgeable instructor ... course was packed with information ... handouts are excellent ... Excellent presentation and contents ... the color rendering section which was interesting and fun ..." Numerical score: 4.36 out of 5.0; ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments: "Instructor is clearly very knowledgeable about the topics ... Very clear and comprehensive ... This is the best class ever ... I'm quite enjoying this course ... I don't really have any recommendations on things to change ... The homeworks and lectures being sent out at the beginning was very helpful ... Both the TA and the professor were able to explain things very well ... I think he is a good lecturer ... I think the homeworks each were very very good at teaching me the material and the exam was fairly graded and easy to understand ... I like the professor definitely and I would have him again ... A good class ... I enjoyed Prof. Schubert's style of teaching ... I would still recommend Prof. Schubert as a professor ... Microelectronics is a good class ... Prof. Schubert keeps it interesting though ... he's a great professor ... The two TAs are also great ..." Numerical score of students' evaluation of instructor: 4.25 out of 5.0 (RPI interpolated median). ***RPI Course ECSE-6220 Physical Foundations of Solid-State Devices***; Verbatim comments: "The book and lectures seem to be entirely in sync with one another ... it really enforces the material covered in the book ... the material is covered thoroughly and improves students' understanding of quantum physics ... The class was interesting with excellent learning materials ... I loved how the course was so well organized ... The lectures were very well put together ..." Numerical score of students' evaluation of instructor:

4.75 out of 5.0 (average).

(**2015**) SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes, Verbatim comments: "I was very satisfied with this short course" Numerical score of students' evaluation: 4.53 out of 5.0; ***RPI Course ECSE-6960 Light-Emitting Diodes***; Verbatim comments: "the class has been excellent! ... I've learned a good amount about LEDs ... Also I'd like to thank you for a great semester and say that you've peaked my interest in the LED field! ... I would like to add that the course was an excellent experience for me and that I really enjoyed learning about LED technology! ... Thank you very much for teaching such a wonderful class ... It was a great learning course" Numerical score of students' evaluation of instructor: 4.60 out of 5.0 (average), 5.0 out of 5.0 (median), and 4.88 out of 5.0 (RPI interpolated median). ***RPI Course ECSE-2100 Fields and Waves 1***; Verbatim comments: "This class is going perfectly and I love the way its run ... The material is great and understandable ... the pace is perfect ... I like the pacing of the course and the fact that we spend time really developing an understanding of the theory and concepts that we will be using ... I like the Professor ... The lectures are great ... I really enjoy this professor and he is very understanding of the students' levels of learning and focused on that ... Professor Schubert is clear and easy to understand ... Overall a very good professor ... very knowledgeable and helpful ... I thought the professor was very knowledgeable and was an excellent instructor ..." Numerical score of students' evaluation of instructor: 4.08 out of 5.0 (average), 4.0 out of 5.0 (median), and 4.17 out of 5.0 (RPI interpolated median).

(**2016**) ***SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes***, Verbatim comments: "This has been my favorite course (over 3 years) ... Well-structured presentation, and well given ... I was surprised by how much I didn't know. I learned a lot ... Explained difficult concepts in a clear and simple manner ... Able to go "off script" to clarify during questions." Numerical score of students' evaluation: 4.56 out of 5.0; ***RPI Course ECSE-2100 Fields and Waves 1***; Verbatim comments: "This is cool material ... This class was one of the most well put together I have ever taken in terms of lecture pace, lecture clarity, TA support, and quality of teaching and communication ... The lectures never felt too long or too short, the pace was good, I never felt lost or without an option to turn for help ... The homework was neither too long nor too short, and was well balanced with conceptual and quantitative questions ... Prof. Schubert's lecture style was very clear, concise, and to the point, with many useful examples in real life scenarios which made the material more interesting ... Very well done ... Great class ... I liked that the pace of the class ... it helps with understanding the material a lot ... The labs [...] were fun and very educational ... Overall I learned a lot of this course ... The speed of the class is perfect ... I really got a chance to learn ... This professor is very good ... Also, [in] the lab section I was able to really break down what I leaned in class ... Schubert has the neatest handwriting of any professor I've ever had in my 3 years here ... His diagrams are extremely neat and he is easy to understand verbally too ... Lot of conceptual knowledge covered ... Overall [...] it was an enjoyable class ..." Numerical score of students' evaluation of instructor: 4.28 out of 5.0 (average), 5.0 out of 5.0 (median), and 4.60 out of 5.0 (RPI interpolated median). ***RPI Course ECSE-2210 Microelectronics Technology***; Verbatim comments: "So far, this has been one of my favorite courses at RPI … I'm a huge fan of Prof. Schubert's ability to clearly describe concepts both conceptually and mathematically … Class activities […] were really helpful! … Otherwise the class is great! … Prof Schubert knows his stuff … Best professor I have had … This course was well taught … Professor Schubert's explanations were very clear and understandable … he took time to address student questions with in-depth answers … I feel as though I gained a lot from this course, especially with regards to explanations of why certain things in ECSE-2050 (Intro to Electronics) occur the way they do like where the diode Kn property comes from and how material properties of electronic components give rise to the very real circuit characteristics we see in ECSE-2050 labs … In this sense, Microelectronics Tech is a very good companion class to Intro to Electronics, and I highly recommend future students take them at the same time … this was a quite good class … Best MET instructor … I was so actively engaged during the lectures that it was kind of scary ... The lecture notes and lectures were mostly great … The material covered in it was succinct and interesting, yet still covered the knowledge needed to tackle engineering problems in semiconductors." Numerical score of students' evaluation of instructor: 4.17 out of 5.0 (average), 5.0 out of 5.0 (median), and 4.64 out of 5.0 (RPI interpolated median).

(**2017**) ***RPI Course ECSE-2100 Fields and Waves 1***; Verbatim comments: "I thoroughly enjoy this class … " ***SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes***, Verbatim comments: "…"

***Post-doctoral fellows and visiting personnel for which I served as Major Research Advisor***

| | | |
|---|---|---|
| Dr. Li-Wei Tu | Post-Doctoral Fellow | 1988–1990 |
| Dr. Neil Hunt | Post-Doctoral Fellow | 1991–1993 |

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|---|---|---|
| Dr. Matthias Passlack | Post-Doctoral Fellow | 1993–1995 |
| Dr. Wolf Grieshaber | Post-Doctoral Fellow | 1995–1997 |
| Dr. Thomas Gessmann | Post-Doctoral Fellow | 2000–2002 |
| Dr. Jong Kyu Kim | Post-Doctoral Fellow | 2003–2005 |
| Dr. Min Ho Kim, SEMCo | Visiting Engineer | 2007–2008 |
| Prof. Ji-Myon Lee, Sunchon University | Visiting Professor | 2007–2008 |
| Dr. Jaehee Cho | Post-Doctoral Fellow | 2008–2009 |
| Dr. Yongjo Park, Samsung LED | Visiting Vice President | 2010–2012 |
| Dr. Yangang Andrew Xi | Visiting Scientist | 2013–2014 |
| Dr. Guan-Bo Lin | Post-Doctoral Fellow | 2014–2015 |

***Graduate students for which I served as Major Research Advisor***

| | | |
|---|---|---|
| Dr. Dean A. Stocker | Ph.D. Dissertation | Ph. D. completed in 1999 |
| Xiaoyun (Jane) Guo | Master Thesis | M.S.E.E. completed in 1999 |
| John W. Graff | Master Thesis | M.S.E.E. completed in 1999 |
| Dr. Ian D. Goepfert | Ph.D. Dissertation | Ph. D. completed in 2000 |
| Yun-Li Li | Master Thesis | M.S.E.E. completed in 2000 |
| Dr. Xiaoyun (Jane) Guo | Ph.D. Dissertation | Ph. D. completed in 2001 |
| Dr. John W. Graff | Ph.D. Dissertation | Ph. D. completed in 2002 |
| Dr. Erik L. Waldron | Ph.D. Dissertation | Ph. D. completed in 2002 |
| Jay M. Shah | Master Thesis | M.S.E.E. completed in 2002 |
| Dr. Yun-Li Li | Ph.D. Dissertation | Ph. D. completed in 2003 |
| Jingqun ("JQ") Xi | Master Thesis | M.S. completed in 2003 |
| Yangang Andrew Xi | Master Thesis | M.S. completed in 2003 |
| Ronald Jackson | Master Thesis | M.S. completed in 2004 |
| Sameer Chhajed | Master Thesis | M.S. completed in 2004 |
| Hong Luo | Master Thesis | M.S. completed in 2005 |
| Xiaolu Li | Master Thesis | M.S. completed in 2005 |
| Kaixuan Chen | Master Thesis | M.S. completed in 2005 |
| Dr. Jay M. Shah | Ph.D. Dissertation | Ph. D. completed in 2006 |
| Frank Mont | Master Thesis | M.S.E.E. completed in 2006 |
| Dr. Hong Luo | Ph.D. Dissertation | Ph. D. completed in 2006 |
| Dr. Jingqun ("JQ") Xi | Ph.D. Dissertation | Ph. D. completed in 2006 |
| Dr. Yangang Andrew Xi | Ph.D. Dissertation | Ph. D. completed in 2006 |
| Won Seok Lee | Master Thesis | M.S. completed in 2007 |
| Qi Dai | Master Thesis | M.S. completed in 2007 |
| Di Zhu | Master Thesis | M.S. completed in 2007 |
| Jiuru Xu | Master Thesis | M.S. completed in 2007 |
| Ahmed Noemaun | Master Thesis | M.S. completed in 2007 |
| Roya Mirhosseini | Master Thesis | M.S. completed in 2008 |
| David Poxson | Master Thesis | M.S. completed in 2008 |
| Qifeng Shan | Master Thesis | M.S. completed in 2009 |
| Ming Ma | Master Thesis | M.S. completed in 2010 |
| Xing Yan | Master Thesis | M.S. completed in 2010 |
| Dr. Roya Mirhosseini | Ph.D. Dissertation | Ph. D. completed in 2010 |
| Dr. Sameer Chhajed | Ph.D. Dissertation | Ph. D. completed in 2010 |
| Dr. Jiuru Xu | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Frank Mont | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Wonseok Lee | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Di Zhu | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Qi Dai | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Ahmed Noemaun | Ph.D. Dissertation | Ph. D. completed in 2011 |

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|---|---|---|
| Dr. David Poxson | Ph.D. Dissertation | Ph. D. completed in 2011 |
| Dr. Qifeng Shan | Ph.D. Dissertation | Ph. D. completed in 2012 |
| Dr. Ann Mao | Ph.D. Dissertation | Ph. D. completed in 2013 |
| Dr. Xing Yan | Ph.D. Dissertation | Ph. D. completed in 2013 |
| Dr. Ming Ma | Ph.D. Dissertation | Ph. D. completed in 2013 |
| Dr. David Meyaard | Ph.D. Dissertation | Ph. D. completed in 2013 |
| Dr. Guan-Bo Lin | Ph.D. Dissertation | Ph. D. completed in 2013 |

**1982**

1. H. Künzel, H. Jung, E. F. Schubert, and K. Ploog "Influence of growth conditions and of alloy composition on electrical and optical properties of MBE AlGaAs" *Journal Physique Colloque C5*, **C5/175**, 42 (1982)

**1984**

2. E. F. Schubert, K. Ploog, H. Dämbkes, and K. Heime "Selectively doped n-AlGaAs/ GaAs heterostructures with high-mobility two-dimensional electron gas for field-effect transistors. Part I: Effect of parallel conductance" *Applied Physics* **A33**, 63 (1984)
3. E. F. Schubert, K. Ploog, H Dämbkes., and K. Heime "Selectively doped n-AlGaAs/ GaAs heterostructures with high-mobility two-dimensional electron gas for field-effect transistors. Part II: Hot electron effects" *Applied Physics* **A33**, 183 (1984)
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6. E. F. Schubert and K. Ploog "Shallow and deep donors in direct-gap n-AlGaAs:Si grown by molecular-beam epitaxy" *Physical Review* **B30**, 7021 (1984)

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7. E. F. Schubert, J. Knecht, and K. Ploog "Transient and persistent photoconductivity in n-AlGaAs and selectively doped n-AlGaAs/GaAs heterostructures" *Journal of Physics C: Solid State Physics* **18**, L215 (1985)
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10. E. F. Schubert, A. Fischer, and K. Ploog "Electron-impurity tunneling in selectively doped n-type AlGaAs/GaAs heterostructures" *Physical Review* **B31**, 7937 (1985)
11. E. F. Schubert, Y. Horikoshi, and K. Ploog "Radiative electron-hole recombination in a new sawtooth semiconductor superlattice grown by molecular-beam epitaxy" *Physical Review* **B32**, 1085 (1985)
12. E. F. Schubert and K. Ploog "The delta-doped field-effect transistor" *Japanese Journal Applied Physics Letters* **24**, L608 (1985)
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14. E. F. Schubert and K. Ploog "Electron subband structure in selectively doped n-AlGaAs/ GaAs heterostructures" *IEEE Transactions on Electron Devices*, **ED-32**, 1868 (1985)
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16. E. F. Schubert, A. Fischer, and K. Ploog "The delta-doped field-effect transistor" *IEEE Transactions on Electron Devices,* **ED-33**, 625 (1986)
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**1989**

51. E. F. Schubert, J. E. Cunningham, T. H. Chiu, J. B. Stark, B. Tell, and C. W. Tu "Spatial localization and diffusion of Si in delta-doped GaAs and AlGaAs and its application to electron-mobility optimization in selectively doped heterostructures" *GaAs and Related Compounds* Ed. J. S. Harris. (1989)
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20. N. E. J. Hunt, E. F. Schubert, and G. J. Zydzik “Photodetector with a resonant cavity” US Patent No. 5,315,128; issued May 24 (1994)
21. A. M. Glass, N. E. J. Hunt, J. M. Poate, E. F. Schubert, and G. J. Zydzik “Absorption resonant rare-earth-doped microcavities” US Patent No. 5,363,398; issued Nov. 8 (1994)
22. N. E. J. Hunt, M. Passlack, E. F. Schubert, and G. J. Zydzik “Electron beam deposition of gallium oxide thin films using a single high purity crystal source” US Patent No. 5,451,548; issued Sep. 19 (1995)
23. N. K. Dutta , R. J. Fischer , N. E. J. Hunt , M. Passlack , E. F. Schubert , and G. J. Zydzik “Gallium oxide coatings for optoelectronic devices using electron beam evaporation of a high purity single crystal $Gd_3Ga_5O_{12}$ source” US Patent No. 5,550,089; issued Aug. 27 (1996)
24. U. K. Chakrabarti, J. de Jong, E. F. Schubert, J. Wynn, and G. J. Zydzik “Mechanical fixture and procedure for in-vacuum coating of semiconductor laser facets” US Patent No. 5,719,077; issued Feb. 17 (1998)
25. E. F. Schubert “Enhanced p-type doping of wide-gap semiconductors” US Patent No. 5,932,899; issued Aug. 3 (1999)

26. J. D. Joannopoulos, S. Fan, P. R. Villeneuve, and E. F. Schubert "Light emitting device utilizing a periodic dielectric structure" US Patent No. 5,955,749; issued Sep. 21 (1999)
27. E. F. Schubert and D. A. Stocker "Crystallographic wet chemical etching on GaN" US Patent No. 6,294,475; issued Sep. 25 (2001)
28. E. F. Schubert "Light-emitting diode with omni-directional reflector" US Patent No. 6,784,462; issued August 31 (2004)
29. Jaehee Cho, Hong Luo, Jong Kyu Kim, Yong Jo Park, Cheolsoo Sone, and E. Fred Schubert "Light emitting device having protection element and method of manufacturing the light emitting device" US Patent No. 7,411,221 B2; issued August 12 (2008)
30. Jaehee Cho, Frank Wilhelm Mont, Cheolsoo Sone, Jong-kyu Kim, June-o Song, E. Fred Schubert "Optical thin film, semiconductor light emitting device having the same and methods of fabricating the same" US Patent No. 7,483,212; issued January 27 (2009)
31. Jaehee Cho, Martin F. Schubert, E. Fred Schubert, Jong Kyu Kim, Cheolsoo Sone "Light emitting diodes and display apparatuses using the same" US Patent No. 7,560,746; filed February 28 (2007); issued July 14 (2009)
32. Martin F. Schubert, Sameer Chhajed, Jong Kyu Kim, E. Fred Schubert, and Jaehee Cho "Reflector shapes for light-emitting diode-polarized light sources" US Patent No. 7,765,495; filed June 24 (2008); issued August 3 (2010)
33. Jaehee Cho, Jong-Kyu Kim, Cheolsoo Sone, and E. Fred Schubert "LED device having diffuse reflective surface" US Patent No. 7,816,855; filed December 28 (2005); issued October 19 (2010)
34. Jaehee Cho, E. Fred Schubert, and Xing Yan "Liquid crystal display with refractive index matched electrodes" US Patent No. 8,164,727; filed April 28, 2010; issued April 24 (2012)
35. Mary H. Crawford, Daniel Koleske, Jaehee Cho, Di Zhu, Troy, Ahmed Noemaun, Martin F. Schubert, and E. Fred Schubert "High efficiency III-Nitride light-emitting diodes" US Patent No. 8,451,877; filed March 17, 2011; issued May 28 (2013)
36. Min-ho Kim, Martin F. Schubert, Jong Kyu Kim, E. Fred Schubert, Yongjo Park, Cheolsoo Sone, and Sukho Yoon "Nitride semiconductor light-emitting device" US Patent No. 8,502,266 filed September 8 (2010); issued August 6 (2013)

**Patent Licensing**

Patents invented or co-invented by E. Fred Schubert have been licensed to several companies.

**1990**

1. (**Invited talk**) E. F. Schubert "Delta-doping of III–V compound semiconductors" *36th Annual Symposium of the American Vacuum Society* Boston, MD, October 23 – 27 (1989)
2. (**Invited colloquium**) E. F. Schubert "Delta-doping III–V compound semiconductors: Fundamentals and device applications" *Harry Diamond Laboratories* Baltimore, MD, January (1990)
3. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Si MBE at room temperature: Solution to the Si doping problem" *6th International Conference on MBE* San Diego, CA, August 27 – 31 (1990)
4. (**Invited talk**) E. F. Schubert, R. F. Kopf, and J. M. Kuo "Delta-doping III–V semiconductors" *4th International Conference on Shallow Impurities in Semiconductors* London, England, July 31 – August 2 (1990)
5. E. F. Schubert, R. F. Kopf, and J. M. Kuo "Mechanisms for impurity redistribution in delta-doped III–V semiconductors grown by MBE" *International Conference on MBE* San Diego, CA, August 27 – 31 (1990)
6. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Si MBE at room temperature: Solution to the Si doping problem" *International Conference on Electronic Materials* Newark, NJ, Sept. 17 – 19 (1990)
7. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Si MBE at room temperature: Solution to the Si doping problem" *37th Annual Symposium of the American Vacuum Society* Toronto, Canada, October 8 – 12 (1990)
8. M. Hong, E. F. Schubert, L.-W. Tu, R. F. Kopf, J. P. Mannaerts, and G. J. Zydzik "Low threshold vertical cavity surface emitting lasers with metallic Ag mirrors and high quantum efficiencies" *6th International Conference on MBE* Univ. of CA, San Diego, CA, August 27 – 31 (1990)
9. E. F. Schubert, R. F. Kopf, G. H. Gilmer, H. S. Luftman, and J. M. Kuo "Repulsive coulcomb interaction in delta-doped GaAs grown by molecular beam epitaxy" *International Conference on Electronic Materials* Newark, NJ, Sept. 17 – 19 (1990)
10. (**Invited colloquium**) E. F. Schubert "Delta-doping of semiconductors" *Philips Research Labs* Redhill, England, July 30 (1990)
11. (**Invited colloquium**) E. F. Schubert "Vertical cavity semiconductor lasers" *AEG Research Labs* Ulm, Germany, August 6 (1990)
12. (**Invited colloquium**) E. F. Schubert "Delta-doping of semiconductors" *University of Texas* Austin TX, August 24 (1990)
13. H.-J. Gossmann, E. F. Schubert, D. J. Eaglesham, and M. Cerullo "Si molecular beam epitaxy at room temperature: Solution to the doping problem" *Topical Conference on Si Based Heterostructures* Toronto, Canada, October 8 – 10 (1990)
14. E. F. Schubert, H. S. Luftman, R. F. Kopf, R. L. Headrick, and J. M. Kuo "Secondary mass spectrometry on delta-doped GaAs grown by molecular beam epitaxy" *37th Annual Symposium of the American Vacuum Society* Toronto, Canada, October 8 – 12 (1990)

**1991**

1. (**Invited talk**) E. F. Schubert "Limitations of doping distributions in III–V semiconductors" *Second International Meeting on Advanced Processing and Characterization Technologies (APCT'91)* Clearwater Beach FL, May 8 – 10 (1991)
2. (**Invited talk**) E. F. Schubert "Smart doping of III–V semiconductor heterostructure devices" *180th Meeting of the Electrochemical Society, State-of-the-Art Program on Compound Semiconductors* Phoenix AZ, October 13 – 18 (1991)
3. E. F. Schubert, G. H. Gilmer, R. F. Kopf, and H. S. Luftman "Extremely highly doped semiconductors: What limits the doping concentration?" *March Meeting of the American Physical Society* Cincinnati, Ohio, March 18 – 22 (1991)
4. H.-J. Gossmann, D. J. Eaglesham, E. F. Schubert, and M. Cerullo "Low temperature growth and doping of silicon" *March Meeting of the American Physical Society* Cincinnati, Ohio, March 18 – 22 (1991)
5. L.-W. Tu, Y. H. Wang, H. M. O'Bryan, B. E. Weir, G. J. Zydzik, E. F. Schubert, and A. Y. Cho "Quantum well lasers with vertical-injection and side-injection schemes" *March Meeting of the American Physical Society* Cincinnati, Ohio, March 18 – 22 (1991)

6. L.-W. Tu, E. F. Schubert, H. M. O'Bryan, Y. H. Wang, B. E. Weir, G. J. Zydzik, and A. Y. Cho "Vertical-injection top-emitting quantum well lasers using transparent conductive metal-oxide contacts" *Conference on Lasers and Electrooptics (CLEO'91)* Baltimore MD, May 12 – 17 (1991)
7. R. F. Kopf, E. F. Schubert, T. D. Harris, and R. S. Becker "Photoluminescence of GaAs quantum wells grown by molecular beam epitaxy with growth interruptions", *Symposium on Properties and Growth of Semiconductors with Atomic Level Control* Murray Hill, NJ, March 6 (1991)
8. H.-J. Gossmann, E. F. Schubert, G. H. Gilmer, D. Monroe, D. E. Eaglesham, H. S. Luftman, F. Schrey, and M. Cerullo "Growth of silicon by molecular beam epitaxy at ultra-low temperatures: exploring the limits of doping in silicon" *Symposium on Properties and Growth of Semiconductors with Atomic Level Control* Murray Hill NJ, March 6 (1991)
9. H. S. Luftman, E. F. Schubert, and R. F. Kopf "Optimized depth resolution for delta-doped samples with secondary ion mass spectrometry" *Symposium on Properties and Growth of Semiconductors with Atomic Level Control* Murray Hill, NJ, March 6 (1991)

**1992**

1. (**Invited talk**) E. F. Schubert "Delta-doping of III–V semiconductors" *March Meeting of the American Physical Society* Indianapolis, Indiana, March 16 – 21 (1992)
2. (**Invited talk**) E. F. Schubert, T. D. Harris, R. S. Becker, G. H. Gilmer, and R. F. Kopf "GaAs/AlGaAs interface configurations probed by photoluminescence and scanning tunneling microscopy" *Materials Research Society Fall Meeting* Boston, MA, Nov 30 – December 4 (1992)
3. A. M. Vredenberg, E. F. Schubert, P. C. Becker, L. C. Feldman, N. E. J. Hunt, D. C. Jacobson, J. M. Poate, Y. H. Wong, and G. J. Zydzik "Spontaneous emission from Er implanted in a resonant Si/$SiO_2$ optical cavity" *8th Int. Conference on Ion Beam Modification on Materials (IBMM)* Heidelberg, Germany, Sept. 7 – 11 (1992)
4. A. M. Vredenberg, D. C. Jacobson, J. M. Poate, P. C. Becker, L. C. Feldman, R. C. Kistler, and E. F. Schubert "High energy Er implantation doping of optical devices" *IX International Conference on Ion Implantation Technology* University of Florida, Gainesville, FL Sept. 21 – 24 (1992)
5. R. F. Kopf, E. F. Schubert, T. D. Harris, and R. S. Becker "Modification of GaAs/AlGaAs growth-interrupted interfaces through changes in ambient conditions during growth" *North American Conf. on Molecular Beam Epitaxy* Ottawa, Canada, October 12 – 14 (1992)
6. A. M. Vredenberg, E. F. Schubert, N. E. J. Hunt, D. C. Jacobson, J. M. Poate, and G. J. Zydzik "Control of spontaneous emission from MeV-implanted Er in a resonant Si/$SiO_2$ optical cavity" *Materials Research Society Fall Meeting, Symposium A* Boston, MA, November 30 – December 4 (1992)
7. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Alcatel/SEL Research Laboratories* Stuttgart, August 31 (1992)
8. E. F. Schubert and R. F. Kopf "Selective n- and p-type C-doping in $Ga_{0.47}In_{0.53}As$ ordered superlattices" *International Conference on Molecular Beam Epitaxy* Schwäbisch Gmünd, Germany, August 24 – 28 (1992)
9. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Max-Planck-Institut für Festkörperforschung* Stuttgart, Sept. 1 (1992)
10. N. E. J. Hunt, E. F. Schubert, R. A. Logan, and G. J. Zydzik "Extremely narrow spectral widths from resonant cavity light-emitting diodes (RCLEDs) suitable for wavelength-division multiplexing at 1.3 μm and 1.5 μm" *1992 International Electron Devices Meeting (IEDM)* San Francisco, CA, December 13 – 16 (1992)

**1993**

1. A. M. Vredenberg, N. E. J. Hunt, E. F. Schubert, D. C. Jacobson, J. M. Poate, and G. J. Zydzik "Controlled atomic-like spontaneous emission from implanted erbium in a $Si/SiO_2$ microcavity" *Quantum Optoelectronics Topical Meeting* Palm Springs, CA, March 17 – 19 (1993)
2. N. E. J. Hunt, E. F. Schubert, D. L. Sivco, A. Y. Cho, R. F. Kopf, and G. J. Zydzik "Narrow spectral emission and high output efficiencies from resonant cavity light-emitting diodes at 0.94 μm wavelength" *Conference of Lasers and Electro-Optics (CLEO '93)* Baltimore, MD, May 2 – 7 (1993)
3. (**Invited talk**) N. E. J. Hunt, E. F. Schubert, D. L. Sivco, A. Y. Cho, R. F. Kopf, and G. J. Zydzik "High-intensity resonant-cavity light-emitting diodes" *March Meeting of the American Physical Society* Seattle WA, March 22 – 26 (1993)

4. H. Yao, E. F. Schubert, and R. F. Kopf "Optical characterizations of delta-doped GaAs" *March Meeting of the American Physical Society* Seattle WA, March 22 – 26 (1993)
5. R. S. Becker, E. F. Schubert, and R. Kopf "Surface/interface morphology of As-capped III–V heterostructure materials" *March Meeting of the American Physical Society* Seattle WA, March 22 – 26 (1993)
6. (**Invited colloquium**) E. F. Schubert and N. E. J. Hunt "Resonant-cavity light-emitting diodes" *Seminar Series on Quantum Devices* Northwestern University, Evanston IL, March 26 (1993)
7. (**Invited talk**) E. F. Schubert and N. E. J. Hunt "Resonant cavity devices" *Brazilian School on Semiconductor Physics* Sao Carlos, Brazil, July 11 – 16 (1993)
8. (**Invited talk**) N. E. J. Hunt, E. F. Schubert, D. L. Sivco, A. Y. Cho, R. F. Kopf, R. A. Logan, and G. J. Zydzik "High efficiency, narrow spectrum resonant cavity light emitting diodes" *A NATO Advanced Study Institute on Confined Electrons and Photons: New Physics and Applications* Erice, Italy, July 13 – 26 (1993)
9. (**Invited talk**) N. E. J. Hunt, A. M. Vredenberg, E. F. Schubert, P. C. Becker, D. C. Jacobson, J. M. Poate, and G. J. Zydzik "Spontaneous emission control of $Er^{3+}$ in $Si/SiO_2$ microcavities" *A NATO Advanced Study Institute on Confined Electrons and Photons: New Physics and Applications* Erice, Italy, July 13 – 26 (1993)
10. (**Invited colloquium**) E. F. Schubert "Integration of information and communication – A technology vision of AT&T" *Hessische Zentrale für Datenverarbeitung (HZD) and Landesautomationsausschuß Hessen (LAA)* Wiesbaden, Germany, November 5 (1993)
11. W. Tsang, E. F. Schubert, and J. E. Cunningham "Doping in semiconductor layered structures and their applications" *1993 Fall Meeting of the Materials Research Society* Boston, MA November 29 – December 3 (1993)

**1994**

1. N. E. J. Hunt, E. F. Schubert, R. J. Malik and G. J. Zydzik "Resonant cavity light-emitting diodes for optical interconnections" *1994 March Meeting of the American Physical Society* Pittsburgh PA, March 21 – 25 (1994)
2. M. Passlack, N. E. J. Hunt, E. F. Schubert and G. J. Zydzik "High quality dielectric $Ga_2O_3$ films for electronic and optoelectronic applications" *1994 March Meeting of the American Physical Society* Pittsburgh, PA, March 21 – 25 (1994)
3. H. Yao, E. F. Schubert, R. F. Kopf and Y. C. Chang "Optical studies of doped GaAs/AlGaAs quantum wells and delta-doped GaAs – a 2D electron system" *1994 March Meeting of the American Physical Society* Pittsburgh PA, March 21 – 25 (1994)
4. (**Invited talk**) E. F. Schubert "Doping in III–V semiconductors" *Spring Meeting of the Materials Research Society* San Francisco, CA, April 4 – 8 (1994)
5. M. Passlack, E. F. Schubert, M. Hong, G. J. Zydzik, W. S. Hobson, J. P. Mannaerts and N. E. J. Hunt "$Ga_2O_3$ films for electronic and optoelectronic applications" *21st International Symposium on Compound Semiconductors* San Diego CA, Sept. 18 – 22 (1994)
6. (**Invited talk**) E. F. Schubert "Resonant cavity light-emitting diodes" *21st International Symposium on Compound Semiconductors* San Diego CA, Sept. 18 – 22 (1994)
7. (**Invited colloquium**) E. F. Schubert "Optoelectronic Devices with Optical Cavities" *Walter Schottky Institute* Garching, Munich, Germany, October 19 (1994)
8. (**Invited talk**) E. F. Schubert "Resonant cavity light-emitting diodes" *International Symposium on guided-Wave Optoelectronics: Device Characterization, Analysis and Design* Polytechnic University, Brooklyn NY, October 26 – 28 (1994)

**1995**

1. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Yale University* New Haven CT, January 20 (1995)
2. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Stanford University*, Edward L. Ginzton Laboratory, Stanford CA, February 6 (1995)
3. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Hewlett-Packard Research Laboratories* Palo Alto CA, February 7 (1995)
4. (**Invited talk**) E. F. Schubert "Resonant cavity devices" *International Symposium on Opto-electronic, Microphotonic, and Laser Technologies* San Jose CA, February 4 – 10 (1995)
5. (**Invited colloquium**) E. F. Schubert "Resonant cavity devices" *Colorado State University* Fort Collins CO, February 10 (1995)

6. Y. C. Chang, H. Yao, E. F. Schubert, and R. F. Kopf "Raman studies of heavily doped $GaAs/Al_xGa_{1-x}As$ multiple quantum wells" *1995 March Meeting of the American Phys. Soc.* San Jose CA, March 20 – 24 (1995)
7. M. Passlack, M. Hong, E. F. Schubert, J. Kwo, J. P. Mannaerts, and G. J. Zydzik "In-situ fabricated $Ga_2O_3$–GaAs structures with low interface recombination velocity" *1995 March Meeting of the American Physical Society* San Jose CA, March 20 – 24 (1995)
8. (**Invited colloquium**) E. F. Schubert "Semiconductor LEDs and lasers" *University of Nebraska* Lincoln NE, April 6 (1995)
9. (**Invited colloquium**) E. F. Schubert "Die Zukunft der Computertechnik und Kommunikationstechnik" *Informationsveranstaltung der AT&T Global Information Solutions und der BB-Data*, Kiel, Germany, June 22 (1995)
10. (**Invited colloquium**) E. F. Schubert "Directions in semiconductor laser and LED research" *Lasertron*, Burlington MA, October 5 (1995)
11. E. F. Schubert "Future Research Directions in the Semiconductor Devices Research Laboratory" Graduate Seminar of the Electrical and Computer Engineering Department, Boston University, Boston MA, November (1995)

**1996**

1. Y. C. Chang, H. Yao, M. Mohiuddin, E. F. Schubert, and L. Pfeiffer "Raman spectra of delta-doped GaAs and heavily doped $GaAs/Al_xGa_{1-x}As$ multiple quantum wells" *1996 March Meeting of the American Physical Society* Saint Louis MO, March 18 – 22 (1996)
2. (**Invited colloquium**) Schubert E. F. "Resonant Cavity Devices" EECS/RLE Seminar Series on "Optics and Quantum Electronics" Massachusetts Institute of Technology, Cambridge MA, March 6 (1996)
3. (**Invited colloquium**) Schubert E. F. "Improvement of Light Emitting Diopdes with Resonant Cavities" Rome Laboratories, Hanscom Air Force Base, Lexington MA, May 23 (1996)
4. (**Invited colloquium**) Schubert E. F. "Improvement of Light Emitting Diodes with Resonant Cavities" *Quantum Energy*, Cambridge MA, June, 6 (1996)
5. Grieshaber W., Schubert E. F., Goepfert I. D., Karlicek R. F. Jr., Schurman M. J., and Tran C. "Nature of ultraviolet and yellow luminescence in GaN" *Fall Meeting of the Materials Research Society*, Boston MA, November (1996)
6. W. Grieshaber, E. F. Schubert, R. F. Karlicek Jr., M. J. Schurman, and C. Tran "Yellow luminescence under spontaneous and stimulated emission conditions in GaN homostructures and heterostructures" *LEOS 1996 Annual Meeting*, Boston MA, October (1996)
7. (**Invited colloquium**) E. F. Schubert "Novel designs for high-efficiency optoelectronic semiconductor devices" Colloquium of the Boston Section of IEEE/LEOS, Lexington MA, December 19 (1996)

**1997**

1. Grieshaber W., Schubert E. F., Karlicek Jr. R. F., Schurman M. J., and Tran C. "Relevance of the GaN yellow luminescence for light-emitting diodes" *SPIE Photonics West Conf. on* Light-emitting diodes: Research and Manufacturing*, San Jose* CA February 10 – 14 (1997)
2. (**Invited colloquium**) Schubert E. F. "Optical Properties of GaN" Emcore Corp., Somerset NJ, March 11 (1997)
3. Tu L.-W., Schubert E. F., Hong M., and Zydzik G. J. "In-situ cleaving and coating of semiconductor laser facets" *March Meeting of the American Physical Society*, Kansas City MO, March 17 – 21 (1997)
4. (**Invited colloquium**) Schubert E. F. "Optical Properties of GaN" *Spire Corporation*, Bedford MA, April 8, (1997)
5. (**Invited colloquium**) Schubert E. F. "Microoptoelectromechanical research at Boston University" *Physical Sciences Inc*., Andover MA, June. 13 (1997)
6. (**Invited colloquium**) Schubert E. F. "Optical Properties of GaN" *Cree Research Corp*., Durham NC, June 16 (1997)
7. (**Invited colloquium**) Schubert E. F. "GaN and MEMS research at Boston University" *US Army Research Office*, Research Triangle Park NC, June 17 (1997)
8. (**Invited colloquium**) Schubert E. F. "Demonstration of optically pumped GaInN/GaN double heterostructure lasers" *Dept. of Electrical Engineering*, University of Connecticut, Storrs CT, November 14 (1997)
9. (**Invited colloquium**) Schubert E. F. "Demonstration of optically pumped GaInN/GaN double heterostructure lasers" *Dept. of Electrical Engineering*, *University of Connecticut*, Storrs CT, November 14 (1997)

10. Stocker D., Schubert E. F., Grieshaber W., Redwing J. M., Boutros K. S., Flynn J. S., and Vaudo R. P., "Fabrication and optical pumping of laser cavities made by cleaving and wet chemical etching" *Mater. Res. Soc*. *Symp*., Boston MA, December 1 – 5 (1997)
11. Goepfert I. D. Schubert E. F. and Redwing J. M. "Luminescence properties of Si-doped GaN and evidence of compensating defects as the origin of the yellow luminescence" *Materials Research Society Symp*osium, Boston MA, December 1 – 5 (1997)

**1998**

1. Schubert E. F., Grieshaber W., Boutros K. S., and Redwing J. M. "Yellow luminescence in MOCVD-grown n-type GaN" *SPIE Photonics West*, San Jose CA, January 28 – 29 (1998)
2. Stocker D. A., Schubert E. F., Boutros K. S., Flynn J. S., Vaudo R. P., Phanse V. M., and Redwing J. M. "Optically pumped InGaN/GaN double heterostructure lasers with cleaved facets" *SPIE Photonics West*, San Jose CA, January 28 – 29 (1998)
3. Schubert E. F. "Demonstration of the first GaInN/GaN double heterostructure laser" *Graduate Student Seminar*, *Dept. of Elec. and Comp. Eng*., Boston Univ., Boston MA, April 18, (1998)
4. Stocker D. A., Schubert E. F., Boutros K. S. and Redwing J. M. "Fabrication of smooth GaN-based laser facets" *Fifth Wide Bandgap Nitride Semiconductor Workshop*, St. Louis MO, August 5 – 7 (1998)
5. Toussaint K., Goepfert I. D., and Schubert E. F. "Differential Hall-effect measurement technique on lightly doped p-type GaN" *Fifth Wide Bandgap Nitride Semiconductor Workshop*, St. Louis MO, August 5 – 7, (1998)

**1999**

1. (**Invited talk**) Boutros K., Smith G. M., Vaudo R. P., Redwing J. M., and Schubert E. F., "InGaN/GaN LED development on GaN-on-sapphire substrates" *SPIE Photonics West*, San Jose CA, January 26 – 28 (1999)
2. (**Invited colloquium**) Schubert E. F. "Demonstration optically pumped GaInN/GaN lasers with smooth facets" *Hewlett Packard Optoelectronics Division*, San Jose CA, January 25 (1999)
3. (**Invited colloquium**) Schubert E. F. "Demonstration optically pumped GaInN/GaN lasers with smooth facets" *Xerox Palo Alto Research Center*, Palo Alto, CA, January 29 (1999)
4. (**Invited colloquium**) Schubert E. F. "P-type doping in GaN and demonstration optically pumped GaInN/GaN lasers with smooth facets" *Army Research Laboratory*, Adelphi MD, February 24 (1999)
5. (**Invited colloquium**) Schubert E. F. "P-type doping in GaN and" *University of Maryland*, College Park MD, February 24 (1999)
6. (The following paper won the Best Student Presentation Award) Stocker D. A., Schubert E. F. and Redwing J. M. "Optically pumped InGaN/GaN lasers with photo-electrochemically and crystallographically wet-etched facets" *Connecticut Symposium on Microelectronics and Optoelectronics* held at Yale University, New Haven CT, March 16 (1999)
7. Goepfert I. D. and Schubert E. F. "Superlattice doping p-type GaN to efficiently activate the deep acceptor magnesium" *Connecticut Symposium on Microelectronics and Optoelectronics* held at Yale University, New Haven CT, March 16 (1999)
8. Schubert E. F. "GaN-based white-light-emitting diodes with high luminous performance" *Optical Physics Seminar Series*, Boston University, Boston MA, October 7 (1999)
9. Schubert E. F. "GaN-based white-light-emitting diodes with high luminous performance", *Optics and Quantum Electronics Seminar Series*, Massachusetts Institute of Technology (MIT), Cambridge MA, November 10 (1999)
10. Guo X. Y., Graff J., and Schubert E. F. "Photon-recycling semiconductor white light emitting diodes" *International Electron Devices Meeting* (IEDM), Washington DC, December 7 (1999)
11. Goepfert I. D., Schubert E. F., Osinski A. and Norris P. E. "Superlattice doping p-type GaN to efficiently activate the deep acceptor magnesium" *Fall meeting of the Materials Research Society (MRS)* Boston MA, November 29 (1999)

**2000**

1. Guo X. Y., Graff J., and Schubert E. F. "Photon-recycling semiconductor white light emitting diodes" *SPIE Photonics West*, San Jose CA, January 25 – 27 (2000)
2. Schubert E. F. "Light-emitting diodes: Device physics and applications" Short course given at the *SPIE Photonics West*, San Jose CA, January 25 – 27 (2000)

3. Waldron E. L., Graff J. W., Schubert E. F., Osinsky A., Schaff W. J., and Eastman L. F. "P-doped AlGaN / GaN superlattices: Physical properties and device applications" *6th Annual Wide Bandgap III-Nitride Workshop*, Richmond VA, March 12 – 15 (2000)
4. Osinsky A., Chernyak L., Zhou L., Adesida I., Graff J. W., and Schubert E. F. "Characterization of Diodes Based on AlGaN/GaN Heterostructures and Superlattices for Bipolar Transistor Applications" *6th Annual Wide Bandgap III-Nitride Workshop*, Richmond VA, March 12 – 15 (2000)
5. Waldron E. L., Schubert E. F., Graff J. W., and Schaff W. J. "Polarization effects in AlGaN/GaN superlattices" *Connecticut Microelectronics and Optoelectronics Symposium*, Hartford CT, March 14 (2000)
6. (**Invited talk**) Schubert E. F., Waldron E. L., Graff J. W., Osinsky A., Schaff W. J., and Eastman L. F. "Current results and future potential of doped AlGaN/GaN superlattices", *ONR / TMS Workshop on Doping and Dopants in GaN*, Copper Mountain CO, April 2 – 6 (2000)
7. Osinsky A., Chernyak L., Fuflyigin V., Graff J. W., and Schubert E. F. "P-type superlattice doping: Material characteristics pertaining to bipolar devices" *ONR / TMS Workshop on Doping and Dopants in GaN*, Copper Mountain CO April 2 – 6 (2000)
8. Schubert E. F. "Light-emitting diodes: Device physics and applications" Short course given at the *University of Hagen*, Germany, July 19 (2000)
9. (**Invited colloquium**) Schubert E. F. "Photon-recycling semiconductor light-emitting diodes" the *University of Hagen*, Germany, July 11 (2000)
10. Graff J. W., Schubert E. F., and Osinsky A "Reduction of base access resistance in npn AlGaN/GaN heterobipolar transistors with p-type AlGaN / GaN superlattice base layers" Cornell Workshop on High-Speed Semiconductor Devices, Ithaca NY, August 6 – 9 (2000)
11. (**Invited talk**) Schubert E. F. Interview on National Public Radio (NPR) in "Here and Now" with Robin Young on the "Photon-recycling semiconductor light-emitting diode". Interviewed on August 22 (2000). Interview transmitted on NPR on August 29 (2000)
12. (**Invited talk**) Schubert E. F., Graff J. W., Li Y.-L., Waldron E. L. and Osinsky A. "Polarization effects, acceptor activation, and ohmic contacts in p-type GaN and AlGaN / GaN superlattices" ONR Workshop on Polarization Effects in III–Nitrides, Kalispell MO, August 27 – 31 (2000)
13. Schubert E. F. "Light-emitting diodes: Device physics and applications" Short course given at the *OSA Annual Meeting*, Providence RI, October 22 (2000)
14. (**Invited colloquium**) Schubert E. F. "Novel concepts for high-efficiency white-light LEDs" Sandia National Laboratories, Albuquerque NM, October 24 (2000)
15. (**Invited talk**) Schubert E. F. "Novel concepts for high-efficiency white-light LEDs" OIDA Workshop and Roadmap Panel on "LED and VCSEL Solid State Lighting" Albuquerque NM, October 25 – 26 (2000)
16. Schubert E. F. "Light-emitting diodes: Device physics and applications" Short course given at the *Photonics East Meeting*, Boston MA, November 8 (2000)
17. Schubert E. F. "Light-emitting diodes: Device physics and applications" Short course given at the *IEEE LEOS Central New England Chapter*, Boston MA, November 18 (2000)
18. (**Invited colloquium**) Schubert E. F. "GaN materials for high-efficiency light emitters" National Central University, Chung-Li, Taiwan, R.O.C., December 4 (2000)
19. (**Invited colloquium**) Schubert E. F. "Novel concepts for high-efficiency white-light LEDs" National Chiao Tung University, Hsin Chu, Taiwan, R.O.C., December 5 (2000)
20. (**Invited colloquium**) Schubert E. F. "Novel concepts for high-efficiency white-light LEDs" National Taiwan University, Taipei, Taiwan R.O.C., December 6 (2000)
21. (**Invited colloquium**) Schubert E. F. "Light emitting diodes" National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., December 8 (2000)
22. (**Invited colloquium**) Schubert E. F. "Novel concepts for high-efficiency white-light LEDs" National Cheng Kung University, Tainan, Taiwan, R.O.C., December 11 (2000)
23. (**Television Interview**) Schubert E. F. "Light emitting diodes for illumination applications" interview broadcast on the 11 PM News of WB56 Boston Television Station. Also shown on many other stations December 15 (2000)
24. Waldron E. L., Schubert E. F., Graff J. W., Osinsky A., Murphy M. J., and Schaff W. F. "Polarization effects in $Al_xGa_{1-x}N$ / GaN superlattices" *Fall Meeting of the Materials Research Society (MRS)*, Boston MA, November 27 – December 1 (2000)

**2001**

1. Guo X. and Schubert E. F. "Current crowding in GaInN / GaN LEDs grown on insulation substrates" *SPIE Photonics West*, San Jose CA, January 24 – 25 (2001)
2. (**Invited colloquium**) Schubert E. F. "GaN materials for high-efficiency light emitters" University of Central Florida, Orlando, Florida, February 22 (2001)
3. (**Invited colloquium**) Schubert E. F. "GaN materials and device issues for high-efficiency light emitting diodes" National Research Council, Ottawa, Canada, March 5 (2001)
4. Li Y.-L., Schubert E. F., Graff J. W., Guo X. Y., and Waldron E. "Low-resistance ohmic contacts to p-type GaN" Connecticut Microelectronics and Optoelectronics Symposium, Storrs CT, April 3 (2001)
5. Guo X. and Schubert E. F. "Current crowding and efficiency improvement in GaInN / GaN LEDs" Connecticut Microelectronics and Optoelectronics Symposium, Storrs CT, April 3 (2001)
6. (**Invited colloquium**) Schubert E. F. "GaN materials and device issues for high-efficiency light emitting diodes" Yale University, New Haven, CT, May 2 (2001)
7. Waldron E. L., Graff J. W., and Schubert E. F. "Improved mobilities and resistivities in modulation doped p-type AlGaN/GaN superlattices" Fourth International Conference on Nitride Semiconductors, Denver CO, July 16 – 20 (2001)
8. Li Y.-L., Graff J. W., Waldron E. L., Guo X., Shah J., and Schubert E. F. "Novel polarization enhanced ohmic contacts to GaN" Fourth International Conference on Nitride Semiconductors, Denver CO, July 16 – 20 (2001)
9. Schubert E. F. "Low-resistance ohmic contacts to p-type GaN using thin InGaN cap layers" ONR workshop on "Sub-surface and near-surface effects in GaN and GaN substrate materials" Kodiak, Alaska, August 6 – 10 (2000)
10. (**Invited talk**) Schubert E. F. "Future light emitting diodes" Symposium on "Future Chips" held at Rensselaer Polytechnic Institute, Troy NY, November 2 (2001)
11. (**Invited talk**) Schubert E. F. "White LEDs based on semiconductors" *Fall meeting of the Materials Research Society (MRS)* Boston MA, November 26 – 30 (2001)
12. Gessmann T., Li Y.-L., Graff J. W., and Schubert E. F. "Low-resistance ohmic contacts to p-type GaN by using InGaN cap layers" *Fall meeting of the Materials Research Society (MRS)* Boston MA, November 26 – 30 (2001)
13. (The following paper won a Best Student Presentation Silver Award) Waldron E. L., Graff J. W., and Schubert E. F. "Improved mobilities in modulation doped p-type AlGaN / GaN superlattices" *Fall meeting of the Materials Research Society (MRS)* Boston MA, November 26 – 30 (2001)

**2002**

1. Gessmann Th., Li Y.-L., Waldron E. L., Graff J. W., and Schubert E. F. "Novel type of ohmic contacts to p-type GaN utilizing polarization fields in thin InGaN capping layers" *Connecticut Symposium on Microelectronics and Optoelectronics*, New Haven, CT, March 13 (Mar 2002)
2. Schubert E. F., Graff J. W., Waldron E. L., Li Y.-L., Gessmann Th., and Sheu J. K. "Recent progresses on superlattice doping of ternary III-nitrides" *Seventh Wide Bandgap III-Nitride Workshop*, Richmond, VA, March 10 – 14 (Mar 2002)
3. Schubert E. F. "The bright future of light-emitting diodes" Brown Bag Lunch Seminar Series at Boston University, Boston, MA, May 22 (May 2002)
4. (**Invited short course**) Schubert E. F. "Light-emitting diodes" *SPIE Photonics Boston*, Boston MA, July 29 – August 2 (Aug 2002)
5. Gessmann Th., Graff J. W., Li Y.-L., Waldron E. L., and Schubert E. F. "Novel ohmic contact technology in III-nitrides using polarization effects in cap layers" *Lester Eastman conference on high-speed devices*, University of Delaware, Newark, DE, August 6 – 8 (Aug 2002)
6. (**Invited talk**) Schubert E. F. "White LEDs based on semiconductors" *Department of Physics, Applied Physics, and Astronomy*, Rensselaer Polytechnic Institute, Troy NY, October 9 (Oct 2002)
7. (**Invited talk**) Schubert E. F. "White LEDs based on an all-semiconductor approach" *Intertech conference entitled Light-emitting diodes 2002*, San Diego CA, October 21 – 23 (Oct 2002)
8. (Short-course) Schubert E. F. "Fundamentals of white LEDs" *Intertech conference entitled Light-emitting diodes 2002*, San Diego CA, October 21 – 23 (Oct 2002)

**2003**

1. (Short course) Schubert E. F. "Light-emitting diodes" *SPIE Photonics West*, San Jose CA, January 27 (January 2003)
2. Gessmann Th., Li Y.-L., Schubert E. F., Graff J. W., and Sheu J. K. "GaInN light-emitting diodes with omni-directional reflectors" *SPIE Photonics West*: Integrated Optoelectronic Devices, San Jose CA, January 25 – 31 (January 2003)
3. Gessmann Th., Schubert E. F., Graff J. W., and Streubel K. "AlGaInP light-emitting diodes with omni-directionally reflecting submount" *SPIE Photonics West*: Integrated Optoelectronic Devices, San Jose CA, January 25 – 31 (January 2003)
4. Schubert E. F. "Ultraviolet-spectrum light-emitting diodes with omni-directional reflectors for high extraction efficiency" *DARPA SUVOS Program Review*, Dana Point CA, February 4 – 6 (February 2003)
5. Li Y.-L., Gessmann Th., Shah J. M., and Schubert E. F. "GaInN-based light-emitting diodes with two active regions for white light emission" *Fifth International Conference on Nitride Semiconductor Research*, Nara, Japan, May 25 – 30 (May 2003)
6. (Short course) Schubert E. F. "Light-emitting diodes" *Conference on Lasers and Electrooptics* (CLEO), Baltimore MD, June 2 – 6 (June 2003)
7. Schubert E. F., Gessmann Th., Graff J. W., Li Y.-L., Sheu J. K., and Streubel K. "Light-emitting diodes with omni-directional reflectors" *Conference on Lasers and Electrooptics* (CLEO), Baltimore MD, June 2 – 6 (June 2003)
8. (Short course) Schubert E. F. "Nanostructures in Optoelectronics" NSF Chautauqua Short Course at RPI, Troy NY, June 23 (June 2003)
9. Schubert E. F. "Research in the Future Chips Constellation on GaN materials and devices" *IBM-RPI Broadband Center Meeting*, Yorktown Heights NY, July 8 (July 2003)
10. Li Y.-L., Shah J. M., Gessmann Th., and Schubert E. F. "Performance characteristics of white light sources consisting of multiple light-emitting diodes" *SPIE Annual Meeting*, San Diego CA, August 4 – 8 (August 2003)
11. Shah J. M., Li Y.-L., Gessmann Th., and Schubert E. F. "Experimental analysis and theoretical model for anomalously high ideality factors in AlGaN/GaN p-n junction diodes " *8th Wide Band Gap III-V Nitride Workshop*, Richmond VA, Sept. 29 – October 1 (October 2003)
12. (**Invited Colloquium**) Schubert E. F. "Semiconductor light emitting diodes for illumination and information technology applications" University at Albany SUNY, School of Nano-sciences, Albany NY, October 16 (October 2003)
13. (**Invited Colloquium**) Schubert E. F. "Semiconductor light emitting diodes for illumination and information technology applications" University at Buffalo SUNY, Department of Electrical Engineering, Buffalo NY October 22 (October 2003)
14. Schubert E. F. "Light-emitting diodes and color perception" undergraduate lecture series entitled *A Passion for Physics*, Rensselaer Polytechnic Institute November 6 (November 2003)
15. Schubert E. F. "Perpendicular transport in AlGaN superlattices and UV-LED diode ideality factors" *DARPA SUVOS Program Review*, Austin TX, November 18 – 20 (November 2003)
16. Shah J. M., Li Y.-L., Gessmann Th., and Schubert E. F. "Experimental analysis and a new theoretical model for anomalously high ideality factors ($n >> 2.0$) in GaN-based p-n junction diodes" *2003 MRS Fall Meeting*, Boston MA, December 1 – 5, (December 2003)
17. Kim J. K., Gessmann Th., Li Y.-L., and Schubert E. F. "GaInN Light-emitting diodes with omni-directional reflectors using rare-earth metal oxides", *2003 MRS Fall Meeting*, Boston MA, December 1 – 5 (December 2003)
18. Li Y.-L., Shah J. M., Gessmann Th., Schubert E. F., and Sheu J. K. "Carrier dynamics of monolithic InGaN/GaN light-emitting pn-junction structures with two active regions" *2003 MRS Fall Meeting*, Boston MA, December 1 – 5 (December 2003)
19. Shah J. M., Li Y.-L., Gessmann Th., and Schubert E. F. "Experimental analysis and a new model for the high ideality factors in GaN-based diodes" *2003 International Semiconductor Device Research Symposium (ISDRS)*, Washington D.C., December 10 – 12 (December 2003)

**2004**

1. Gessmann T., Luo H., Xi J.-Q., Streubel K. P., and Schubert E. F. "Light-emitting diodes with integrated

omnidirectionally reflective contacts" *Photonics West*, San Jose, CA, January 27 – 28 (2004)

2. Shah J., Li Y., Gessmann T., and Schubert E. F. "Experimental analysis and new theoretical model for anomalously high ideality factors ($n$ >> 2) in GaN-based p-n junction diodes" *SPIE Photonics West – Light Emitting Diodes: Research, Manufacturing, and Applications*, San Jose CA, January 27 – 28 (2004)
3. (Short course) Schubert E. F. "Light-emitting diodes" *SPIE Photonics West*, San Jose CA, January 29 (January 2004)
4. (**Invited**) Schubert E. F. "Semiconductor light emitting diodes for illumination and information technology applications" *Samsung Research Center (SAIT)*, Seoul, Korea, March 15 (March 2004)
5. (**Invited**) Schubert E. F. "Smart lighting" *International Symposium on the Physics of Semiconductors and Applications (ISPSA)*, Gyeongju, Korea, March 16 (March 2004)
6. (**Invited**) Schubert E. F. "Semiconductor light emitting diodes for illumination and information technology applications" *Pohang University for Science and Technology (POSTECH)*, Pohang, Korea, March 17 (March 2004)
7. Kim J. K., Waldron E. L., Lee Y.-L., Gessmann T., Jang H. W., Lee J.-L., and Schubert E. F. "P-type conductivity in bulk $Al_xGa_{1-x}N$ and $Al_xGa_{1-x}N/Al_yGa_{1-y}N$ superlattices with average Al mole fraction $\geq$ 20% for LED confinement layers" *The 5th International Symposium on Blue Laser and Light Emitting Diodes* (ISBLLED-2004) p. 275, Gyeongju, Korea, March 15 – 19 (2004)
8. Kim J. K., Gessmann T., Luo H., and Schubert E. F. "GaInN light emitting diodes with omni-directional reflectors" *Connecticut Microelectronics and Optoelectronics Symposium*, Univ. of Connecticut, Storrs CT, April 7 (2004)
9. Li Y.-L., J. Shah M., Jackson R., Xi Y., Chhajed S., Kim J. K., Gessmann Th., and Schubert E. F. "Illumination sources based on multiple light-emitting diodes" *Conference on Lasers and Electro-Optics (CLEO)*, San Francisco CA, May 16 – 20 (2004)
10. (Short course) Schubert E. F. "Light Emitting Diodes and Solid-State Lighting" *Conference on Lasers and Electrooptics (CLEO)*, San Francisco CA, May 16 – 20 (2004)
11. (Short course) Schubert E. F. "Nanostructures in Optoelectronics" NSF Chautauqua Short Course at RPI, Troy NY, June 28 – 29 (2004)
12. Schubert E. F. "Smart Lighting" *University of Rochester*, Rochester NY, July 12 (2004)
13. Furis M., Cartwright A. N., Waldron E. L., and Schubert E. F. "Spectral and temporal resolution of recombination dynamics from multiple states in modulation-doped AlGaN/GaN multiple quantum well heterostructures" *International Workshop on Nitride Semiconductors (IWNS)*, Pittsburgh PA, July 19 – 23 (2004)
14. Kim J. K., Gessmann T., Luo H., and Schubert E. F. "GaInN light-emitting diodes with omni-directional reflectors" *2004 IEEE Lester Eastman Conference on High Performance Devices*, Rensselaer Polytechnic Institute, USA, August 4 – 6 (2004)
15. Xi Y. and Schubert E. F. "Junction-temperature measurements in GaN UV light-emitting diodes using the diode forward voltage" *IEEE Lester Eastman Conference on High Performance Devices*, Troy NY, August 4 – 6 (2004)
16. Xi J.-Q., Ojha M., Cho W., Gessmann T., Schubert E. F., Plawsky J. L., and Gill W. N. "Omni-directional reflector using a low-refractive-index material" *IEEE Lester Eastman Conference on High-Performance Devices*, Rensselaer Polytechnic Institute, Troy NY August 4 – 6 (2004)
17. Luo H., Gessmann Th., and Schubert E. F. "Ray tracing simulation of extraction efficiency of truncated-inverted pyramid AlGaInP light emitting diodes with omni-directional reflector" *IEEE Lester Eastman Conference on High-Performance Devices*, Rensselaer Polytechnic Institute, Troy NY August 4 – 6 (2004)
18. Chhajed S., Xi Y., Li Y.-L., Gessmann T., and Schubert E. F. "Influence of junction temperature on luminous efficacy and color rendering properties of a trichromatic LED-based white light source" *IEEE Lester Eastman Conference on High Performance Devices*, Troy NY, August 4 – 6 (2004)
19. (Short course) Schubert E. F. "Light Emitting Diodes and Solid-State Lighting" *SPIE Photonics North*, Ottawa, Canada, September 27 – 29 (2004)
20. (**Invited**) Schubert E. F. "Novel Concepts for the Advancement of Solid-State Light Emitters" Seminar at Department of Physics, Applied Physics, and Astronomy, RPI, October 4 (2004)
21. (**Invited**) Schubert E. F., Kim J. K., Gessmann T., Chhajed S., Li Y.-L., Luo H., Mont F. W., Shah C., Shah J., Xi J.Q., Xi Y., Lin S. Wetzel C. Plawsky J., Gill W., and Siegel R. "Research in the Future Chips Constellation" *General Electric Corporation*, Schenectady NY, October 26 (2004)

22. (**Invited**) Schubert E. F. "Light-emitting diodes and solid-state lighting" featured as module in the web-based IEEE Xplore-Enabled Learning Library (IEEE XELL). The module was delivered to IEEE in October (2004)
23. (**Invited**) Schubert E. F. "Efficiency limitations of solid-state sources used in general illumination applications" *28th Annual EDS/CAS Activities in Western New York Conference*, Rochester, NY, November 3 (2004)
24. (**Invited**) Schubert E. F. "Nano-Materials in Optoelectronics" Nanotechnology – Innovation, Opportunity, and Commercialization RPI, Troy NY, Nov 15 – 16 (2004)
25. (**Invited**) Schubert E. F. "Efficiency limitations in inorganic solid-state sources for lighting applications" *Annual Meeting of the American Vacuum Society*, Anaheim CA, November 15 – 19 (2004)
26. (**Invited**) Schubert E. F. "Novel omnidirectional reflectors with unprecedented performance characteristics" *2004 OIDA Annual Forum*, Washington, D.C. November 18 – 19 (2004)
27. Xi Y., Xi J.-Q., Gessmann Th., Shah J. M. , Kim J. K., Schubert E. F., Fischer A. J., Crawford M. H., Bogart K. H. A., and Allerman A. A. "Junction temperature measurements in deep-UV light-emitting diodes" *MRS Fall meeting*, Boston MA, November 29 – December 3 (2004)
28. Kim J. K., Luo H., Xi Y., Shah J. M., Gessmann Th., and Schubert E. F. "Enhancement of light extraction efficiency of GaInN LEDs by omni-directional diffuse reflectors" *MRS Fall Meeting*, Boston MA, November 29 – December 3 (2004)
29. Xia Y., Williams E., Park Y., Yilmaz I., Shah J., Schubert E. F., and Wetzel C. "Discrete steps in the capacitance-voltage characteristics of GaInN/GaN light emitting diode structures" *MRS Fall Meeting*, Boston MA, November 29 – December 3 (2004)
30. (**Invited**) Schubert E. F. "High-reflectivity omni-directional reflectors for light-emitting diodes" *International Electron Devices and Materials Symposium* (IEDMS), National Chiao Tung Univ., Hsin Chu, Taiwan, December 20 – 23 (2004)

**2005**

1. Yangang Xi, Sameer Chhajed, J.-Q. Xi, Thomas Gessmann, Jay M. Shah, Jong Kyu Kim and E. F. Schubert "Junction and carrier temperature measurements in light-emitting diodes using three different methods" *SPIE Photonic West*, San Jose CA, January 22 – 27 (Jan 2005)
2. J.-Q. Xi, M. Ojha, W. Chow, C. Wetzel, Th. Gessmann, E. F. Schubert, J. L. Plawsky, and W. N. Gill "Omni-directional reflector using a low-refractive-index material" *SPIE Photonics West – Light-Emitting Diodes: Research, Manufacturing, and Applications*, San Jose CA, January 22 – 27 (Jan 2005)
3. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonics West – Light-Emitting Diodes: Research, Manufacturing, and Applications*, San Jose CA, January 22 – 27 (Jan 2005)
4. (**Invited keynote address**) E. F. Schubert, Jong Kyu Kim, Hong Luo, Yangang Xi, Jay M. Shah, and Thomas Gessmann "Enhancement of light extraction in GaInN light-emitting diodes by diffuse omni-directional reflectors" *Second Asia-Pacific Workshop on Widegap Semiconductors* (APWS-2005) Hsinchu, Lakeshore Hotel, Hsinchu, Taiwan, March 7 – 9 (March 2005)
5. (**Invited colloquium**) E. F. Schubert "Innovations in Light-Emitting Diodes" University of Florida, Department of Electrical and Computer Engineering, Gainesville FL, March 15 (March 2005)
6. (**Best Oral Presentation Award.** Speaker Hong Luo) Hong Luo, Jong Kyu Kim, Yangang Xi, Jay M. Shah, Thomas Gessmann and E. Fred Schubert "Improvement of extraction efficiency of GaInN light-emitting diodes by employment diffuse omni-directional reflectors" *Connecticut Microelectronics & Optoelectronics Consortium* (CMOC), 14th annual symposium, New Haven CT, March 17 (March 2005)
7. Yangang Xi, J.-Q. Xi, Thomas Gessmann, Jay M Shah., Jong Kyu Kim, E. F. Schubert, A. J. Fischer, M. H. Crawford, K. H. A. Bogart and A. A. Allerman "Junction temperature and thermal resistance measurement in deep-UV light-emitting diodes" *Connecticut Microelectronics & Optoelectronics Consortium*, 14th annual symposium, New Haven CT, March 17 (March 2005)
8. J.-Q. Xi, M. Ojha, W. Cho, Th. Gessmann, E. F. Schubert, J. L. Plawsky, and W. N. Gill "Omni-directional reflector using a low refractive index material" *Connecticut Microelectronics & Optoelectronics Consortium*, 14th annual symposium, New Haven CT, March 17 (March 2005)
9. J.-Q. Xi, M. Ojha, W. Chow, C. Wetzel, T. Gessmann, E. F. Schubert, J. L. Plawsky, and W. N. Gill "Omni-Directional Reflector Using a Low Refractive Index Material" *Conference on Lasers and Electrooptics* (CLEO), Baltimore MD, May 22 – 27 (May 2005)
10. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" *Conference on Lasers and*

*Electrooptics* (CLEO), Baltimore MD, May 22 – 27 (May 2005)

11. (**Invited**) E. F. Schubert "Solid-state light sources getting smart" Radio interview with BBC Worldwide Service, May 26 (May 2005)
12. (**Invited**) E. F. Schubert "Solid-state light sources getting smart" Radio interview with German SWR Service, May 26 (May 2005)
13. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" *Chautauqua Short Course* at RPI, Troy NY, June 13 (June 2005)
14. (**Invited**) E. F. Schubert and Jong Kyu Kim "Solid-state light sources getting smart" Television interview with Jim Kambrich, Albany NBC Affiliate, Channel 13, June 15 (June 2005)
15. (**Invited**) E. F. Schubert and Jong Kyu Kim "Innovations in light-emitting devices" Samsung Advanced Institute of Technology, Suwan City, Korea, June 27 (June 2005)
16. (**Invited**) E. F. Schubert "Short course on light-emitting diodes" Samsung Mechatronics Corporation, Suwan City, Korea, June 28 (June 2005)
17. (**Invited**) E. F. Schubert and Jong Kyu Kim "Innovations in light-emitting devices" Seoul National University, Seoul Korea, June 29 (June 2005)
18. E. F. Schubert "AlGaN UV light-emitting diodes grown by MOVPE" Crystal IS Corporation, Green Island NY, July 22 (July 2005)
19. Jong Kyu Kim, J.-Q. Xi, Hong Luo, and E. Fred Schubert "Enhancement of light extraction in GaN ultraviolet light-emitting diodes by omni-directional reflectors with nanoporous low-index layer" *SPIE Annual Meeting, Illumination Engineering, Fifth International Conference on Solid State Lighting*, San Diego, CA, August 1 – 4, (August 2005)
20. (**Invited**) E. F. Schubert "Innovations in light-emitting devices" University of Delaware, Department of Electrical and Computer Engineering, September 7 (September 2005)
21. Thomas Gessmann, Yangang Xi, Hong Luo, Jong Kyu Kim, J.-Q. Xi, Kaixuan Chen, Jay M. Shah and E. Fred Schubert "Polarization-enhanced ohmic contacts to GaInN-based blue light-emitting diodes" *AVS 52nd International Symposium & Exhibition*, October 30 – November 4, Boston MA (October 2005)
22. Hong Luo, Jong Kyu Kim, Yangang Xi, E. Fred Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Trapped whispering-gallery optical modes in white light-emitting diodes lamps with remote phosphor" *AVS 52nd International Symposium & Exhibition*, October 30 – November 4, Boston MA (October 2005)
23. Yangang Xi, Xiaolu Li, Jong Kyu Kim, Frank W. Mont, Thomas Gessmann, Hong Luo, Alyssa Pasquale, and E. Fred Schubert "Quantitative assessment of diffusivity and specularity of textured surfaces for light extraction in light-emitting diodes", *AVS 52nd International Symposium & Exhibition*, October 30 – November 1, Boston MA (October 2005)
24. Hong Luo, Jong Kyu Kim, Yangang Xi, E. F. Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Analysis of high-power packages for white-light-emitting diode lamps with remote phosphor" *MRS Fall Meeting*, November 28 – December 2, Boston MA (November 2005)
25. Jong Kyu Kim, J.-Q. Xi, Hong Luo, Jay M. Shah, Thomas Gessmann, Jaehee Cho, Cheolsoo Sone, Yongjo Park, and E. Fred Schubert "Enhancement of light extraction in GaInN light-emitting diodes by omni-directional reflectors with ITO nanorod low-index layer" *2005 Materials Research Society (MRS) Fall Meeting* November 28 – December 2, Boston MA (November 2005)
26. Jay M. Shah, Jong Kyu Kim, Hong Luo, Yangang Xi, Thomas Gessmann, and E. Fred Schubert "Reduction of base access resistance in AlGaN/GaN heterojunction bipolar transistors using GaInN base cap layer and selective epitaxial growth" *2005 Materials Research Society (MRS) Fall Meeting* November 28 – December 2, Boston MA (November 2005)
27. J.-Q. Xi, Jong Kyu Kim, Dexian Ye, Jasbir S. Juneja, T.-M. Lu, Shawn-Yu Lin and E. F. Schubert "Optical thin films with very low refractive index and their application in photonics" *2005 Materials Research Society (MRS) Fall Meeting* November 28 – December 2, Boston MA (November 2005)
28. Hong Luo, Jong Kyu Kim, Yangang Xi, Jaehee Cho, Cheolsoo Sone, Yongjo Park, and E. Fred Schubert, "High power packages for phosphor-based white-light-emitting diode lamps" *International Semiconductor Device Research Symposium (ISDRS)*, December 7 – 9, Bethesda MD (December 2005)
29. (**Best Poster Award**) J.-Q. Xi, Jong Kyu Kim, Dexian Ye, Jasbir S. Juneja, T.-M. Lu, Shawn-Yu Lin, and E. Fred Schubert "Optical Thin Films with Very Low Refractive Index and Their Application in Photonic Devices", *International Semiconductor Device Research Symposium (ISDRS)*, December 7 – 9, Bethesda, MD (December

2005)

30. (**Key Note Address**) E. F. Schubert and Jong Kyu Kim "Innovations in Light-Emitting Devices" Thirteenth International Workshop on The Physics of Semiconductor Devices, New Delhi, India, December 13 – 17 (December 2005)

**2006**

1. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" Centro de Investigacion Y De Estudios Avanzados del I.P.N. (Center for Research and Advanced Studies) Mexico City, Mexico, January 12 – 13 (January 2006)
2. (**Invited colloquium, IEEE Distinguished Lecture Program**) E. F. Schubert and Jong Kyu Kim "Innovations in light-emitting diodes" Centro de Investigacion Y De Estudios Avanzados del I.P.N. (Center for Research and Advanced Studies) Mexico City, Mexico, January 12 – 13 (January 2006)
3. (**Invited colloquium**) E. F. Schubert and Jong Kyu Kim "Innovations in light-emitting diodes" Optical Science Center, University of Arizona, Tucson, January 19 (January 2006)
4. (**Invited colloquium**) E. F. Schubert "Innovations in light-emitting diodes" Nanotechnology Seminar, Wayne State University, Detroit MI, February 7 (February 2006)
5. (**Invited colloquium**) E. F. Schubert "Material challenges for solid-state lighting" Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy NY, February 23 (February 2006)
6. (**Invited**) E. F. Schubert "Material challenges for solid-state lighting" March Meeting of the American Physical Society (APS), Baltimore MD, March 13 (March 2006)
7. (**Invited press conference presentation**) E. F. Schubert "Material challenges for solid-state lighting" March Meeting of the American Physical Society (APS), Baltimore MD, March 13 (March 2006)
8. (**Invited colloquium**) E. F. Schubert "Innovations in light-emitting diodes for solid-state lighting applications" New Jersey Institute of Technology together with the IEEE NJ Section Electron Devices, Circuits and Systems; New Jersey Institute of Technology (NJIT), Newark NJ, March 22 (March 2006)
9. (**Invited plenary short course**) E. F. Schubert "Light-emitting diodes for solid-state lighting" *Spring Meeting of Materials Research Society*, MRS, San Francisco CA, April 17 – 21 (April 2006)
10. Y. A. Xi, Th. Gessmann, K. X. Chen, X. Li, J. K. Kim, E. F. Schubert, W. Liu, J. A. Smart, and L. J. Schowalter "AlGaN UV LEDs emitting at 340 nm grown on AlN bulk substrates" *Spring Meeting of Materials Research Society*, MRS, San Francisco CA, April 17 – 21 (April 2006)
11. (**Invited colloquium**) E. F. Schubert "Innovations in light-emitting diodes for solid-state and smart lighting applications" *The Ohio State University, IEEE Distinguished Lecture Series*, Columbus OH, April 27 (April 2006)
12. (**Plenary presentation**) E. F. Schubert "Solid-state lighting – Opportunities for fundamental innovation" U.S. Department of Energy (DOE*), Solid State Lighting Workshop*, Bethesda MD, May 21 – 24 (May 2006)
13. (**Invited tutorial**) E. F. Schubert "Solid-state lighting – Opportunities for fundamental innovation" *Conference on Lasers and Electrooptics (CLEO)*, Long Beach CA, May 22 – 26 (May 2006)
14. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" *Conference on Lasers and Electrooptics (CLEO)*, Long Beach CA, May 22 – 26 (May 2006)
15. Jong Kyu Kim, J.-Q. Xi, Hong Luo, E. Fred Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Enhancement of light-extraction in GaN light-emitting diodes by conductive omni-directional reflectors" *Conference on Lasers and Electrooptics (CLEO)*, Long Beach CA, May 22 – 26 (May 2006)
16. (**Invited short course**) E. F. Schubert "Solid-state lighting" Summer Short Course under "*2006 Summer @ Rensselaer*" program organized by the *RPI Outreach Programs Office*, Troy NY, June 7 – 8 (June 2006)
17. (**Invited short course**) E. F. Schubert "Light-emitting diodes and solid-state lighting" Short Course under "*Chautauqua Program of the National Science Foundation and the RPI Center for Directed Assembly of Nanostructures*" Troy NY, June 12 (June 2006)
18. Y. A. Xi, Th. Gessmann, K. X. Chen, X. Li, J. K. Kim, E. F. Schubert, W. Liu, J. A. Smart, L. J. Schowalter "AlGaN UV light-emitting diodes emitting at 340 nm grown on AlN bulk substrates" *IEEE Lester Eastman Conference on High Performance Devices*, Ithaca NY, August 2 – 4 (August 2006)
19. K. X. Chen, Y. A. Xi, F. Mont, J. K. Kim, E. F. Schubert, C. Wetzel, W. Liu, X. Li, J. A. Smart, and L. J. Schowalter "Very high quality AlN grown on (0001) sapphire by using metal-organic vapor-phase epitaxy" *IEEE Lester Eastman Conference on High Performance Devices*, Ithaca NY, August 2 – 4 (August 2006)
20. Hong Luo, Jong Kyu Kim, E. Fred Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Highly efficient

package configurations for white-light-emitting diode lamps" *IEEE Lester Eastman Conference on High Performance Devices*, Ithaca NY, August 2 – 4 (August 2006)

21. (**Plenary presentation**) E. Fred Schubert and Jong Kyu Kim "Solid-state lighting – Opportunities for fundamental innovation" *International Symposium on Compound Semiconductors* (ISCS), Vancouver, Canada, August 14 – 17 (August 2006)
22. (**Plenary presentation**) E. Fred Schubert and Jong Kyu Kim "Solid-state lighting – Opportunities for fundamental innovation" *Asia-Pacific Optical Communications Conference* (APOC), Gwangju, Korea, September 3 – 7 (September 2006)
23. (**Invited**) E. F. Schubert and Jong Kyu Kim "Smart lighting" Seminar at *Samsung Advanced Institute of Technology* (SAIT), Suwon, Korea, September 18 (September 2006)
24. (**Plenary presentation**) E. Fred Schubert and Jong Kyu Kim "Solid-state lighting – Opportunities for fundamental innovation" *13th International Workshop on Inorganic and Organic Electroluminescence* and *2006 International Conference on the Science and Technology of Emissive Displays and Lighting* (EL2006), Jeju Island, Korea, September 18 – 22 (September 2006)
25. Jong Kyu Kim, J.-Q. Xi, Hong Luo, E. F. Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Improvements in light-extraction efficiency of light-emitting diodes with omnidirectional reflectors" *13th International Workshop on Inorganic and Organic Electroluminescence* and *2006 International Conference on the Science and Technology of Emissive Displays and Lighting* (EL2006), Jeju Island, Korea, September 18 – 22 (September 2006)
26. Y. Li, W. Zhao, Y. Xia, M. Zhu, J. Senawiratne, T. Detchprohm, E. F. Schubert, and C. Wetzel "Temperature dependence of the quantum efficiency in green light-emitting diode dies" *International Workshop on Nitride Semiconductors* (IWN 2006) Kyoto, Japan, October 22 – 27 (October 2006)
27. (**Invited colloquium**) E. F. Schubert "Solid-State Lighting – Opportunities for Fundamental Innovation" *OSA Colloquium Rochester*, University of Rochester, Institute of Optics, October 24 (October 2006)
28. (**Invited colloquium**) E. F. Schubert, S. Y. Lin, and C. Wetzel "Solid-state lighting research at RPI" *Sandia National Laboratories*, Albuquerque NM, November 3, (November 2006)
29. (**Invited short course**) E. F. Schubert "Light-emitting diodes and LED-based Imaging Systems" *Thirteenths Color Imaging Conference*, Scottsdale AZ, November 7 – 11 (November 2006)
30. J. Das, J. K. Kim, Y. A. Xi, E. F. Schubert, and P. M. Mensz "Recombination dynamics at dislocations in GaInN-based light-emitting diodes" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
31. Y. A. Xi, K. X. Chen, F. Mont, J. K. Kim, C. Wetzel, E. F. Schubert, W. Liu, X. Li, J. A. Smart "Extremely high quality AlN grown on (0001) sapphire by using metal-organic vapor-phase epitaxy" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
32. Y. A. Xi, K. X. Chen, F. Mont, J. K. Kim, E. F. Schubert, W. Liu, J. A. Smart, X. Li, L. J. Schowalter "AlGaN UV light-emitting diodes (< 345 nm) grown on AlN bulk substrates" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
33. Roya Mirhosseini, Jong Kyu Kim, Hong Luo, J. Cho, C. Sone, Y. Park, and E. F. Schubert "Omni-directional reflectors for GaInN vertical-structure light-emitting diodes" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
34. Frank Mont, Hong Luo, Jong Kyu Kim, E. F. Schubert, and R. W. Siegel "Enhancement of light-extraction efficiency in light-emitting diodes by optimized scattering properties of nanoparticle-loaded encapsulants" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
35. J.-Q. Xi, Jong Kyu Kim, and E. F. Schubert "Low-refractive-index materials: A new class of material for optoelectronic and photonic applications" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
36. J.-Q. Xi, Hong Luo, Jong Kyu Kim, and E. F. Schubert "High light-extraction efficiency in GaInN light-emitting diode with pyramid reflector" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)
37. Kaixuan Chen, Yangang A. Xi, Frank Mont, Jong Kyu Kim, E. F. Schubert, Xiaolu Li, Wayne Liu, Joseph A. Smart "Effect of Si modulation doping in multiple quantum well active region on characteristics of AlGaN ultraviolet light-emitting diodes" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 –December 1 (December 2006)

38. Hong Luo, Jong Kyu Kim, E. Fred Schubert, Jaehee Cho, Cheolsoo Sone, and Yongjo Park "Whispering-gallery modes in GaN-based white-light-emitting diode lamps with remote phosphor" *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (December 2006)

**2007**

1. Frank W. Mont, Jong Kyu Kim, Martin F. Schubert, Hong Luo, E. Fred Schubert, and Richard W. Siegel "High refractive index nanoparticle-loaded encapsulants for light-emitting diodes" *SPIE Photonic West*, San Jose CA, January 22 – 26 (January 2007)
2. J.-Q. Xi, Hong Luo, Jong Kyu Kim, and E. F. Schubert "High light-extraction efficiency in GaInN light-emitting diode with pyramid reflector" *SPIE Photonic West*, San Jose CA, January 22 – 26 (January 2007)
3. Frank W. Mont, Jong Kyu Kim, Martin F. Schubert, Hong Luo, E. Fred Schubert, and Richard W. Siegel "High refractive index nanoparticle-loaded encapsulants for light-emitting diodes" *Connecticut Microelectronics & Optoelectronics Consortium*, 16th annual symposium, New Haven CT, March 21 (March 2007)
4. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Jose CA, January 22 – 26 (January 2007)
5. (**Invited colloquium**) E. Fred Schubert "Solid-state lighting – Opportunities for fundamental innovation" Department of Physics Colloquium, Queen's University, Kingston, Ontario, Canada, March 28 (March 2007)
6. Arthur J. Fischer, Frank Mont, Jong Kyu Kim, E. Fred Schubert, Daniel Koleske, and Mary Crawford "Enhanced light extraction from InGaN quantum wells using refractive-index-matched $TiO_2$" *Conference on Lasers and Electro-optics* (CLEO), Baltimore MD, May 6 – 11 (May 2007)
7. Jong Kyu Kim, Martin F. Schubert, J. Q. Xi, Frank W. Mont, and E. Fred Schubert "Enhancement of light extraction in GaInN light-emitting diodes with graded-index indium tin oxide layer" *Conference on Lasers and Electro-optics* (CLEO), Baltimore MD, May 6 – 11 (May 2007)
8. (**Invited colloquium**) E. Fred Schubert "Solid-state lighting – Opportunities for fundamental innovation" General Electric (GE) Global Research Laboratories with live simulcast to GE Research Laboratories in Munich, Germany and Bangalore, India; Niskayuna NY, May 25 (May 2007)
9. E. Fred Schubert "Nanotechnology – Opportunities for Innovations in Solid-State Lighting" *National Institute for Nano-Engineering (NINE) Workshop*, Sandia National Laboratories, Albuquerque NM, June 11 – 13 (June 2007)
10. E. Fred Schubert "Solid-state lighting – Opportunities for fundamental innovation" *RPI NSEC Center Seminar for Graduate Students*, RPI, Troy NY, June 26 (June 2007)
11. E. Fred Schubert "Solid-state lighting – Opportunities for fundamental innovation" *RPI NSEC Nanoscale Science and Engineering: A Short Course for High School Teachers*, RPI, Troy NY, July 12 (July 2007)
12. (**Invited keynote address**) E. Fred Schubert and Jong Kyu Kim "Light-Emitting Diodes – Looking back 100 years and looking forward to the next 10 years" 2007 China International Solid State Lighting Forum and Exhibition (CHINA SSL 2007), Shanghai, China, August 22 – 24 (August 2007)
13. Y. A. Xi, K. X. Chen, F. W. Mont, J. K. Kim, W. Lee, and E. F. Schubert "Kinetic study of Al-mole fraction in $Al_xGa_{1-x}N$ grown on c-plane sapphire and AlN bulk substrates by metal-organic vapor-phase epitaxy" *7th International Conference on Nitrides Semiconductors* (*ICNS-7*) Las Vegas, NV, September 16 – 21 (September 2007)
14. M. H. Crawford, D. D. Koleske, N. A. Missert, S. R. Lee, M. A. Banas, D. M. Follstaedt, K. H. A. Bogart, G. Thaler, and K. C. Cross, Y. Xia, C. Wetzel, and E. F. Schubert "Mechanisms for enhanced quantum efficiency of InGaN quantum wells grown on InGaN underlayers" *7th International Conference on Nitrides Semiconductors* (*ICNS-7*) Las Vegas, NV, September 16 – 21 (September 2007)
15. Min-Ho Kim, Martin F. Schubert, Qi Dai, Jong Kyu Kim, Joachim Piprek, Yongjo Park, and E. Fred Schubert "Cause and solution of efficiency droop in GaN-based light-emitting diodes" *7th International Conference on Nitrides Semiconductors* (*ICNS-7*) Las Vegas, NV, September 16 – 21 (September 2007)
16. K. X. Chen, W. Lee, Q. Dai, F. W. Mont, J. K. Kim, E. F. Schubert, W. Liu, S. Wu, and J. A. Smart "Effect of ammonia and silane flow rate on the structural, electrical and optical properties of n-type AlGaN for UV emitter applications" *7th International Conference on Nitrides Semiconductors* (*ICNS-7*) Las Vegas, NV, September 16 – 21 (September 2007)
17. Jong Kyu Kim, Sameer Chhajed, Martin F. Schubert, Jaehee Cho, Cheolsoo Sone, and E. Fred Schubert "Enhancement in light-extraction of GaInN light-emitting diodes by using indium-tin-oxide graded-refractive-

index antireflection contacts" *7th International Conference on Nitrides Semiconductors* (*ICNS-7*) Las Vegas, NV, September 16 – 21 (September 2007)

18. (**Invited keynote address**) E. Fred Schubert and Jong Kyu Kim "Low-refractive-index materials: A new class of optical thin-film materials for solid-state lighting" *7th International Conference on the Numerical Simulation of Optoelectronic Devices* (NUSOD 2007), Newark DE, September 24 – 27 (September 2007)
19. Min-Ho Kim, Martin F. Schubert, Qi Dai, Jong Kyu Kim, Joachim Piprek, Yongjo Park, and E. Fred Schubert "Cause and solution of efficiency droop in GaN-based light-emitting diodes" *31st Annual EDS/CAS Activities in Western New York Conference, Electron Devices Society – Western New York*, Rochester NY, November 7 (November 2007)
20. K. X. Chen, Q. Dai, W. Lee, Jong Kyu Kim, E. Fred Schubert, W. Liu, S. Wu, X. Li, and J. A. Smart "Parasitic sub-band-gap emission originating from compensating native defects in Si doped AlGaN" *31st Annual EDS/CAS Activities in Western New York Conference, Electron Devices Society – Western New York*, Rochester NY, November 7 (November 2007)
21. (**Invited keynote address**) E. Fred Schubert and Jong Kyu Kim "Light-emitting diodes – Looking back 100 years and looking forward to the next 10 years" *S&T/SID's 15th Color Imaging Conference (CIC)*, Albuquerque NM, November 5 – 9 (November 2007)
22. Min-Ho Kim, Martin F. Schubert, Jong Kyu Kim, and E. Fred Schubert, Hee Seok Park, Yong Jo Park, and Joachim Piprek "Investigation on origin of efficiency droops in InGaN-based high-power blue light emitting diodes" *Materials Research Society (MRS) Fall Meeting*, Boston, MA, November 26 – 30 (November 2007)
23. Wonseok Lee, Kaixuan Chen, Qi Dai, Min-Ho Kim, Jong Kyu Kim, and E. Fred Schubert, W. Liu, S. Wu, X. Li, and J. A. Smart "Effect of structural properties of AlN templates on the optical and electrical properties of n-type AlGaN" *Materials Research Society (MRS) Fall Meeting*, Boston, MA, November 26 – 30 (November 2007)
24. Martin. F. Schubert, Sameer Chhajed, Jong Kyu Kim, E. Fred Schubert, and Jaehee Cho "Polarization anisotropy in the light emission of blue GaInN/GaN light-emitting diodes grown on (0001) oriented sapphire substrates" *Materials Research Society (MRS) Fall Meeting*, Boston, MA, November 26 – 30 (November 2007)
25. Frank Wilhelm Mont, David J. Poxson, Jong Kyu Kim, E. Fred Schubert, Arthur J. Fischer and Mary H. Crawford "Enhancement of light extraction efficiency in GaInN blue light-emitting diodes by graded-refractive-index antireflection coating of co-sputtered titanium dioxide and silicon dioxide" *Materials Research Society (MRS) Fall Meeting*, Boston, MA, November 26 – 30 (November 2007)

**2008**

1. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Innovation in optical materials for the advancement of solid-state lighting technologies" *Workshop on Nano Optoelectronics*, Korea Institute of Science and Technology (KAIST), Daedeok Science Town, Daejeon, South Korea, January 6 – 8 (January 2008)
2. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Progress on light-emitting diode research" Samsung Electro-Mechanics Company, Suwon-City, South Korea, January 9 (January 2008)
3. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Jose CA, January 21 – 24 (January 2008)
4. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Low-refractive index materials – A new class of materials for photonic applications" *SPIE Photonic West*, San Jose CA, January 21 – 24 (January 2008)
5. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Innovation in optical materials for the advancement of solid-state lighting technologies" *Colloquium*, Rochester Institute of Technology, Rochester, New York, March 13 (March 2008)
6. Q. Dai, M. F. Schubert, M. H. Kim, J. K. Kim, E. F. Schubert, D. D. Koleske, M. H. Crawford, S. R. Lee, A. J. Fischer, G. Thaler, and M. A. Banas "Effect of dislocation density on internal quantum efficiency in GaInN/GaN multiple quantum wells" *Connecticut Microelectronics and Optoelectronics Conference* (*CMOC*), University of Connecticut, Storrs, Connecticut April 9 (April 2008)
7. (**Best Oral Presentation Award**) David J. Poxson, Frank W. Mont, Jong Kyu Kim, and E. Fred Schubert "Multilayer nano-structured anti-reflection coating with broad-band omni-directional characteristics" *Connecticut Microelectronics and Optoelectronics Conference* (*CMOC*), University of Connecticut, Storrs, Connecticut April 9 (April 2008)
8. Frank W. Mont, David J. Poxson, Martin F. Schubert, Ahmed Noemaun, Jong Kyu Kim, E. Fred Schubert, Arthur J. Fischer and Mary H. Crawford "Micro-patterned graded-refractive-index coatings of co-sputtered TiO2 and

SiO2 for enhanced light-extraction from GaInN light-emitting diodes" *International Symposium on Semiconductor Light Emitting Devices*, *ISSLED*, Phoenix, Arizona, April 27 – May 2 (April 2008)

9. M. F. Schubert, S. Chhajed, J. K. Kim, E. F. Schubert, M. H. Kim, D. D. Koleske, M. H. Crawford, S. R. Lee, A. J. Fischer, G. Thaler, M. A. Banas, and J. Piprek "Efficiency droop in GaInN/GaN LEDs: the effect of dislocation density, physical origin, and possible solution" *International Symposium on Semiconductor Light Emitting Devices*, *ISSLED*, Phoenix, Arizona, April 27 – May 2 (April 2008)
10. J. R. Grandusky, J. A. Smart, M. C. Mendrick, L. J. Schowalter, K. X. Chen, and E. F. Schubert, "Pseudomorphic growth of thick n-$Al_xGa_{1-x}N$ layers on low defect density bulk AlN substrates for UV LED applications", *International Symposium on Semiconductor Light Emitting Devices*, Phoenix, AZ, April 27 – May 2 (April 2008)
11. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Innovation in optical materials for the advancement of solid-state lighting technologies" *Colloquium*, State University of New York Stony Brook, Stony Brook, New York, May 6 (May 2008)
12. (**Invited**) Jong Kyu Kim, Min-Ho Kim, Martin F. Schubert, Qi Dai, Sagong Tan, Sukho Yoon, Cheolsoo Sone, Yongjo Park, Joachim Piprek, and E. Fred Schubert "The origin of efficiency droop in GaN-based light-emitting diodes and its solution" *Conference on Lasers and Electro-Optics*, *CLEO*, San Jose, California May 4 – 9 (May 2008)
13. K. X. Chen, Q. Dai, W. Lee, J. K. Kim and E. F. Schubert, W. Liu, S. Wu, X. Li, and J. A. Smart "Parasitic sub-band-gap emission originating from compensating native defects in Si- doped AlGaN" *2008 Electronic Materials Conference*, *EMC*, Santa Barbara, California, June 25 – 27 (June 2008)
14. J. R. Grandusky, J. A. Smart, M. C. Mendrick, L. J. Schowalter, K. X. Chen, and E. F. Schubert "Pseudomorphic growth of thick n-type $Al_xGa_{1-x}N$ layers on low defect density bulk AlN substrates for UV LED applications" *2nd International Symposium on Growth of III-Nitrides*, Laforet Shuzenji, Izu, Japan, July 6 – 9 (July 2008)
15. Frank W. Mont, Arthur J. Fischer, Mary H. Crawford, David J. Poxson, Sameer Chhajed, Ahmed Noemaun, Jong Kyu Kim and E. Fred Schubert "Enhanced light extraction from GaInN light-emitting diodes using micro-patterned graded-refractive-index coatings" *Sandia NINE Community Week Conference*, Sandia National Laboratories, Albuquerque NM, July 31, 2008
16. Roya Mirhosseini, Jong Kyu Kim, C. Sone, Y. Park, and E. F. Schubert "Light-extraction efficiency enhancement in vertically structured GaInN-based light-emitting diode on bulk GaN substrate" *2008 Lester Eastman Biennial Conference on High-Performance Devices*, University of Delaware, Newark, Delaware, August 5 – 7 (August 2008)
17. Jiuru Xu, Martin F. Schubert, Jong Kyu Kim, and E. Fred Schubert, "The effect of hole-injection efficiency on efficiency droop of GaN-based light emitters investigated by light-emitting triodes" *2008 Lester Eastman Biennial Conference on High-Performance Devices*, University of Delaware, Newark, Delaware, August 5 – 7 (August 2008)
18. Ahmed Noemaun Frank W. Mont, David J. Poxson, Di Zhu, Jong Kyu Kim, and E. Fred Schubert "Design of graded refractive index micro-patterns to enhance light-extraction efficiency in GaInN blue light-emitting diodes" *2008 Lester Eastman Biennial Conference on High-Performance Devices*, University of Delaware, Newark, Delaware, August 5 – 7 (August 2008)
19. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Relevance of light-emitting diodes and photonics for energy" *US-Korea Conference on Science, Technology, and Entrepreneurship*, UKC 2008, San Diego, California, August 14 – 17 (August 2008)
20. M. F. Schubert, S. Chhajed, Jong Kyu Kim, J. Cho, and E. F. Schubert "Polarized c-plane GaInN/GaN light-emitting diodes" *International Workshop on Nitride Semiconductors*, IWN 2008, Montreux, Switzerland, October 6 – 10 (October 2008)
21. Jong Kyu Kim, M. H. Kim, M. F. Schubert, Q. Dai, J. Piprek, S.-M. Lee, S. Yoon, C. Sone, Y. Park, D. D. Koleske, M. H. Crawford, S. R. Lee, E. Fred Schubert "Efficiency droop in GaN-based light-emitting diodes" *International Workshop on Nitride Semiconductors*, IWN 2008, Montreux, Switzerland, October 6 – 10 (October 2008)
22. David J. Poxson, F. W. Mont, M. F. Schubert, J. K. Kim, E. F. Schubert "Quantification of porosity and deposition rate of nano-porous films grown by oblique angle deposition" *55th International Symposium of the American Vacuum Society*, Boston, Massachusetts, October 19 – 24 (October 2008)
23. (**Invited short course**) E. Fred Schubert "Light emitting diodes and solid-state lighting" *OSA Frontiers in Optics 2008*, University of Rochester, Rochester, New York, October 24 – 26 (October 2008)

24. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Energy implications of solid-state lighting technology" *OSA Frontiers in Optics 2008*, University of Rochester, Rochester, New York, October 24 – 26 (October 2008)
25. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Smart Lighting" *BASF Corporation*, Ossining, New York, December 1 (December 2008)
26. (**Invited**) Jong Kyu Kim and E. Fred Schubert "Low-refractive index materials" *BASF Corporation*, Ossining, New York, December 1 (December 2008)
27. (**Invited**) E. Fred Schubert "Smart Lighting" *ERC 2008 Annual Meeting*, Bethesda Maryland, December 3 – 5 (December 2008)
28. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Light-Emitting Diodes – Looking back 100 years and looking forward to the next 10 years" *Interlight Show*, Moscow, Russia, December 8 – 12 (December 2008)
29. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Light-Emitting Diodes – Looking back 100 years and looking forward to the next 10 years" *Moscow University*, Moscow, Russia, December 11 (December 2008)

**2009**

1. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Jose CA, January 26 – 30 (January 2009)
2. (**Invited**) E. Fred Schubert, Jong Kyu Kim, Min Ho Kim, Martin F. Schubert "Polarization-matching in GaInN light-emitting diodes: a new concept for reducing efficiency droop and enhancing performance" *SPIE Photonic West*, San Jose CA, January 26 – 30 (January 2009)
3. (**Invited**) Min-Ho Kim, Wonseok Lee, Zhu Di, Martin F. Schubert, Jong Kyu Kim, E. Fred Schubert, Cheolsoo Sone, Yongjo Park, and Joachim Piprek "Origin of Efficiency Droop in GaInN/GaN MQW LEDs and its Possible Solution" *SPIE Photonic West*, San Jose CA, January 26 – 30 (January 2009)
4. Jiuru Xu, Martin F. Schubert, Ahmed N. Noemaun, Di Zhu, Jong Kyu Kim, E. Fred Schubert, Min Ho Kim, Sukho Yoon, Hun-Jae Chung, Cheolsoo Sone, and Yongjo Park "Reduction of Efficiency Droop, Forward Voltage, Electroluminescence Peak Shift and Ideality Factor in Polarization-matched GaInN/GaInN Multi-quantum-well Light-emitting Diodes" *MRS Spring Meeting*, San Francisco, California, April 13 – 17 (April 2009)
5. (**Invited**) M. F. Schubert, J. Xu, Q. Dai, F. Mont, M. H. Kim, J. K. Kim, E. F. Schubert, H. Chung, S. Yoon, C. Sone and Y. Park "Study of Efficiency Droop in GaInN/GaN and Polarization-matched GaInN/AlGaInN and GaInN/GaInN Light-emitting Diodes" *215th Electrochemical Society Meeting*, San Francisco CA, May 24 – 29 (2009)
6. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Low-refractive index materials – A new class of optical thin-film materials for photonics applications" *Workshop on Metamaterials*, University of North Carolina, Charlotte, North Carolina, May 27 – 29 (May 2009)
7. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Low-refractive index materials – A new class of optical thin-film materials for photonics applications" *Conference on Lasers and Electro-optics* (CLEO / IQEC) Baltimore, Maryland, May 31 – June 5 (June 2009)
8. Q. Dai, M. F. Schubert, M. H. Kim, J. K. Kim, E. F. Schubert, D. D. Koleske, M. H. Crawford, S. R. Lee, A. J. Fischer, G. Thaler, and M. A. Banas "Internal quantum efficiency and non-radiative recombination coefficient of GaInN/GaN multiple quantum wells with different dislocation densities" *Conference on Lasers and Electro-optics* (CLEO / IQEC) Baltimore, Maryland, May 31 – June 5 (June 2009)
9. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Energy implications of solid-state lighting technology" OSA 2009 Topical Meeting, Optics and Photonics for Advanced Energy Technology, Massachusetts Institute of Technology (MIT), Cambridge MA, June 24 and 25 (June 2009)
10. Wonseok Lee, Min-Ho Kim, Di Zhu, Ahmed N. Noemaun, E. Fred Schubert, and Jong Kyu Kim "Growth and characteristics of GaInN/GaInN light-emitting diodes: 2009 *Electronic Materials Conference* (EMC) University Park, Pennsylvania, June 24 – 26 (June 2009)
11. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Energy implications of solid-state lighting technology" Colloquium at the University of Hagen, Hagen, Germany, July 14 (July 2009)
12. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Energy implications of solid-state lighting technology" Colloquium at Everlight Europe, Karlsruhe, Germany, July 15 (July 2009)
13. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Energy implications of solid-state lighting technology" Osram Opto Semiconductors, Regensburg, Germany, July 17 (July 2009)

14. (**Invited**) Jong Kyu Kim and E. Fred Schubert "Energy implications of solid-state lighting technology" *US-Korea Conference on Science, Technology and Entrepreneurship*, Raleigh, North Carolina, July 16 – 19 (July 2009)
15. Roya Mirhosseini, Martin F. Schubert, Sameer Chhajed, Jaehee Cho, Jong. K. Kim, and E. Fred Schubert "Enhancements in color rendering and luminous efficacy of phosphor-converted white light-emitting diodes with dual-blue emitting active regions" *SPIE Annual Meeting, Ninth International Conference on Solid-State Lighting*, San Diego, California, August 2 – 6 (August 2009)
16. Martin F. Schubert, Jong Kyu Kim and E. Fred Schubert "Novel low-refractive-index materials and their applications" *SPIE Annual Meeting, Ninth International Conference on Solid-State Lighting*, San Diego, CA, August 2 – 6 (August 2009)
17. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Light-emitting diode designs for high power applications – overcoming high-power loss mechanisms" *International Conference on Nitride Semiconductors* (*ICNS*) Jeju, South Korea, October 18 – 23 (October 2009)
18. Jong Kyu Kim, F. W. Mont, A. Noemaun, D. Meyaard, and E. Fred Schubert "Enhanced light extraction and controllability of far-field emission pattern of GaInN light-emitting diodes by graded-refractive-index micro-pillars" *International Conference on Nitride Semiconductors* (*ICNS*) Jeju, South Korea, October 18 – 23 (October 2009)
19. (**Invited**) E. Fred Schubert "Light-emitting diode designs for high power applications – overcoming high-power loss mechanisms" Samsung LED Company, Suwon, South Korea October 21 (October 2009)
20. (**Invited**) E. Fred Schubert and Jong Kyu Kim "Challenges and opportunities in solid-state lighting" *Materials Research Society Fall Symposium* (MRS), Boston, Massachusetts, November 30 – December 4 (December 2009)
21. Di Zhu, Jiuru Xu, Ahmed N. Noemaun, Jong-Kyu Kim, E. Fred Schubert, Mary H. Crawford, and Daniel D. Koleske "The origin of the high diode-ideality factors in GaInN/GaN multiple quantum well light-emitting diodes" *Materials Research Society Fall Symposium* (MRS), Boston, Massachusetts, November 30 – December 4 (December 2009)
22. Ahmed N. Noemaun, Frank Mont, David J. Poxson, Jong-Kyu Kim, E. Fred Schubert "Graded-refractive-index micro-patterns on GaInN light-emitting diodes for enhanced light extraction and control over the far field emission pattern" *Materials Research Society Fall Symposium* (MRS), Boston, Massachusetts, November 30 – December 4 (December 2009)
23. David Meyaard, Jaehee Cho, Martin F. Schubert, Sameer Chhajed, Jong Kyu Kim, and E. Fred Schubert "Nitride based light emitting diodes embedded with a wire-grid polarizer" *Materials Research Society Fall Symposium* (MRS), Boston, Massachusetts, November 30 – December 4 (December 2009)
24. (**Keynote address**) E. Fred Schubert and Jong Kyu Kim "Material and Device Innovations in Light-Emitting Diodes for High Efficiency at High Currents" *International Conference on White LEDs and Solid State Lighting*, Taipei, Taiwan, December 13 – 16 (December 2009)

**2010**

1. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Francisco CA, January 24 – 28 (January 2010)
2. (**Invited**) E. Fred Schubert "Promises and challenges in solid-state lighting" *March Meeting of the American Physical Society*, Portland, Oregon, March 15 – 19 (March 2010)
3. (**Keynote presentation**) E. Fred Schubert "Tailored refractive index structures for photonic devices" *Workshop on Black Materials organized by the Defense Advanced Research Projects Agency (DARPA)*, Arlington, Virginia, March 31 – April 1 (March 2010)
4. (**Invited**) E. Fred Schubert "Promises and challenges in solid-state lighting" *Connecticut Symposium on Microelectronics and Optoelectronics* (*CMOC*), Storrs, Connecticut, April 7 (April 2010)
5. (**Invited**) E. Fred Schubert and Martin F. Schubert "Efficiency droop in GaInN solid-state-lighting devices" *Conference on Lasers and Electro-optics* (*CLEO*), San Jose, California, May 16 – 21 (May 2010)
6. (**Invited**) E. Fred Schubert "Promises and challenges in solid-state lighting" *AVS-MI Spring Symposium*, University of Michigan, Ann Arbor, Michigan, May 26 (May 2010)
7. Qi Dai, Qifeng Shan, Jing Wang, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Mary H. Crawford, and Daniel D. Koleske "Carrier-loss mechanisms behind efficiency droop in GaInN/GaN light-emitting diodes" *IEEE Lester*

*Eastman Conference on High Performance Devices*, Rensselaer Polytechnic Institute, Troy NY, August 3 – 5 (August, 2010)

8. An Mao, Qi Dai, Jaehee Cho, and E. Fred Schubert "Characteristics of dot-shaped green emission in GaInN blue light-emitting diode" *IEEE Lester Eastman Conference on High Performance Devices*, Rensselaer Polytechnic Institute, Troy NY, August 3 – 5 (August, 2010)
9. Jiuru Xu, Martin. F. Schubert, Ahmed. N. Noemaun, Jaehee Cho, E. Fred Schubert, Min-Ho Kim, and Yongjo Park "Reducing efficiency droop in GaInN based light-emitting diodes by matching material polarization" *IEEE Lester Eastman Conference on High Performance Devices*, Rensselaer Polytechnic Institute, Troy NY, August 3 – 5 (August, 2010)
10. Xing Yan, Frank W. Mont, David J. Poxson, Martin F. Schubert, Jaehee Cho, and E. Fred Schubert "Anti-reflection coating made of indium-tin-oxide (ITO) electrode for liquid crystal display panel" *IEEE Lester Eastman Conference on High Performance Devices*, Rensselaer Polytechnic Institute, Troy NY, August 3 – 5 (August, 2010)
11. Di Zhu, Ahmed N. Noemaun, Martin F. Schubert Jaehee Cho, E Fred Schubert, Mary H. Crawford, Daniel D. Koleske "Enhanced electron capture and symmetrized carrier distribution in GaInN LEDs having tailored barrier doping" *International Workshop on Nitride Semiconductors* (IWN2010) Tampa, Florida, September 19 – 24 (September 2010)
12. Jaehee Cho, Di Zhu, An Mao, Jong Kyu Kim, Joong Kon Son, Yongjo Park, and E. Fred Schubert "Characteristics of reverse current in GaInN light-emitting diodes" *International Workshop on Nitride Semiconductors* (IWN2010) Tampa, Florida, September 19 – 24 (September 2010)

**2011**

1. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Francisco CA, January 22 – 27 (January 2011)
2. (**Invited**) E. Fred Schubert and Jaehee Cho "The efficiency droop in GaInN light-emitting diodes" *SPIE Photonic West*, San Francisco CA, January 22 – 27 (January 2011)
3. Ashok K. Sood, Roger E. Welser, Adam W. Sood, E. James Egerton and Yash R. Puri, David Poxson, Jaehee Cho, E. Fred Schubert, Dennis L. Polla, Nibir K. Dhar, and Martin B. Soprano "Nanosdtructure-based antireflection coatings for EO/IR sensor applications" *SPIE Photonic West*, San Francisco CA, January 22 – 27 (January 2011)
4. Qi Dai, Qifeng Shan, Jing Wang, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Mary H. Crawford, Daniel D. Koleske, Min-Ho Kim, and Yongjo Park "Carrier recombination mechanisms and efficiency droop in GaInN/GaN light-emitting diodes" *SPIE Photonic West*, San Francisco CA, January 22 – 27 (January 2011)
5. (**Best Oral Paper Award**) David Meyaard, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Jong Kyu Kim, Daniel D. Koleske, and Mary H. Crawford "Temperature-dependent light-output characteristics of GaInN light-emitting diodes with different dislocation densities" *Connecticut Microelectronics and Optoelectronics Consortium* (CMOC) Symposium, New Haven CT, March 2 (March 2011)
6. (**Invited**) E. Fred Schubert and Jaehee Cho "Promises and challenges in light-emitting diodes for lighting applications" 2011 IEEE Workshop on Microelectronics and Electron Devices, WMED-2011, Boise State University, April 22, (2011)
7. Qi Dai, Qifeng Shan, Jaehee Cho, E. Fred Schubert, Mary H. Crawford, Daniel D. Koleske, Min-Ho Kim, and Yongjo Park "On the symmetry of efficiency-versus-carrier-concentration curves in GaInN/GaN light-emitting diodes and relation to droop-causing mechanisms" Conference on Lasers and Electro Optics, CLEO, Baltimore, Maryland, May 1 – 6 (2011)
8. (**Invited**) E. Fred Schubert and Jaehee Cho "Tunable-refractive-index materials – A new class of optical thin-film materials" Workshop on Meta-materials and Plasmonics: Novel Materials, Designs, and Applications, University of Buffalo, Buffalo NY, May 16 and 17 (2011)
9. Qi Dai, Qifeng Shan, Jaehee Cho, E. Fred Schubert, Mary H. Crawford, and Daniel D. Koleske "On the symmetry of efficiency-versus-carrier-concentration curves in GaInN/GaN light-emitting diodes and relation to droop-causing mechanisms" Energy Frontiers Research Center (EFRC) Meeting, US Department of Energy, Washington DC May 25 – 27 (2011)
10. (**Invited**) Jong Kyu Kim, Jaehee Cho, and E. Fred Schubert "Promises and challenges in light-emitting diodes for lighting applications" 15th International Symposium on the Physics of Semiconductors and Applications (ISPSA-XV), Jeju, Korea, July 5 – 8 (2011)

11. Jaehee Cho, An Mao, Qifeng Shan, Jong Kyu Kim, Joong Kon Son, and E. Fred Schubert "Leakage current analysis in GaInN blue light-emitting diodes" *International Conference on Nitride Semiconductors* ICNS, Glasgow, UK, July 10 – 15 (2011)
12. Ahmed N. Noemaun, Frank W. Mont, Gi Bum Kim, Cheolsoo Sone, Jaehee Cho, and E. Fred Schubert "Study of patterned graded-refractive-index layers to enhance light-extraction efficiency and control of far-field emission pattern of GaInN LEDs" *International Conference on Nitride Semiconductors* ICNS, Glasgow, UK, July 10 – 15 (2011)
13. E. Fred Schubert, Jaehee Cho, Mary Crawford, and Dan Koleske "Efficiency droop in GaInN LEDs" Sandia National Laboratories, Albuquerque NM, July 27 (2011)
14. David J. Poxson, Richard Siegel and E. Fred Schubert "Tailored refractive index nanoporous thin films on flexible substrates" *Rensselaer Nanotechnology Center Symposium*, Troy NY (Oct 2011)
15. Sameer Chhajed, Jong Kyu Kim, Wonseok Lee, Jaehee Cho, E. Fred Schubert "Light-Extraction Enhancement in GaInN LEDs by Self-Organized Nanoscale Patterning of p-Type GaN using Oblique-Angle Deposition" International Conference on Applied Electromaterials, ICAE 2011, Jeju, Korea, November 7 – 10 (2011)
16. (**Invited Plenary Presentation**) Jaehee Cho, E. Fred Schubert "Promises and challenges in light-emitting diodes for lighting applications" International Conference on Applied Electromaterials, ICAE 2011, Jeju, Korea, November 7 – 10 (Nov 2011)
17. David J. Poxson, Xing Yan, Frank W. Mont, Jaehee Cho, E. Fred Schubert "Broadband Omnidirectional Antireflection Coatings: Enhanced Solar Cell Device Performance" Center for Future Energy Systems Symposia, RPI Troy NY (Nov 2011)
18. (**Invited Plenary Presentation**) E. Fred Schubert "Promises and challenges in light-emitting diodes for lighting applications" State and Organic Lighting (SOLED) Meeting of the OSA, Austin Texas, November 2 – 3 (Nov 2011)
19. Qifeng Shan, David S. Meyaard, Qi Dai, Jaehee Cho, E. Fred Schubert, Joong Kon Son and Cheolsoo Sone, "On the reverse leakage current in GaInN light-emitting diodes" *MRS Fall Meeting*, Boston, Massachusetts, Nov. 28 – Dec. 2 (2011)
20. David J. Poxson, Frank W. Mont, Jaehee Cho, E. Fred Schubert, and Richard W. Siegel "Optical Coatings Utilizing Nanoporous Thin Films Fabricated on Flexible Polymer Substrates" *MRS 2011 Fall Meeting*, Boston, Massachusetts, Nov. 28 – Dec. 2 (Dec 2011)

**2012**

1. (**Invited short course**) E. Fred Schubert "Light-emitting diodes and solid-state lighting" *SPIE Photonic West*, San Francisco CA, January 21 – 26 (January 2012)
2. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "The Efficiency Droop in GaInN Light-Emitting Diodes" *SPIE Photonic West*, San Francisco CA, January 21 – 26 (January 2012)
3. Jiuru Xu, Martin F. Schubert, Di Zhu, Jaehee Cho, and E. Fred Schubert, Hyunwook Shim and Cheolsoo Sone "Effects of polarization-field tuning in GaInN light-emitting diodes" *SPIE Photonic West*, San Francisco CA, January 21 – 26 (January 2012)
4. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "The seed of a revolution in lighting: Light-emitting diodes" Institute of Optical Sciences, University of Toronto, Toronto, Canada, March 15 (March 2012)
5. (**The Boris P. Stoicheff Lecture; Invited keynote presentation**) E. Fred Schubert "The Seed of a Revolution in Lighting: Light-Emitting Diodes" University of Toronto, Toronto, Canada, March 16 (March 2012)
6. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "High-injection phenomena in GaN-based LEDs" *Coffee / Desert Hour of the Energy Frontiers Research Center on Solid-State Lighting Sciences*; Sandia National Laboratories, Albuquerque NM, March 29, (March 2012)
7. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "The seed of a revolution in lighting: Light-emitting diodes" *Conference on Opto and Microelectronics* (*CMOC*), Storrs, CT, April 11 (April 2012)
8. (**Keynote presentation**) E. Fred Schubert and Jaehee Cho "The seed of a revolution in lighting: Light-emitting diodes" *Compound Semiconductor Manufacturing Technologies* (*CSMantech*), Boston, MA, April 23-26 (April 2012)
9. Guan-Bo Lin, Q. Shan, A. J. Birkel, J. Cho, and E. F. Schubert, D. D. Koleske and M. H. Crawford "Internal quantum efficiency in light-emitting diodes based on the width of efficiency-versus-carrier-concentration curve" *Conference on Lasers and Electro-optics* (*CLEO*), San Jose, California, May 6 – 11 (May 2012)

10. David S. Meyaard, Guan-Bo Lin, Qifeng Shan, Jaehee Cho, E. Fred Schubert, Hyun Wook Shim, Min-Ho Kim, Cheolsoo Sone, Hyun Wook Shim, Min-Ho Kim, and Cheolsoo Sone "Asymmetry of carrier transport leading to efficiency droop in GaInN based light-emitting diodes" *Conference on Lasers and Electro-optics* (*CLEO*), San Jose, California, May 6 – 11 (May 2012)
11. J. Kim, S. Hwang, J. Park, D. Kim, J. Cho, and E. F. Schubert "Efficiency Droop in GaN-based Light-Emitting Diodes: Mechanisms and Solutions" PRiME 2012, State-of-the-Art Program on Compound Semiconductors 54 (SOTAPOCS 54), Honolulu, Hawaii, October 7 – 12, 2012 (October 2012)
12. Yong Suk Cho, M. Evans, S. Chowdhury, D. Meyaard, M. Ma, X. Yan, J. Cho, and E. Fred Schubert "GaN growth on ion-implanted patterned sapphire substrates" *International Workshop on Nitride Semiconductors*, IWN 2012, Sapporo, Japan, October 14 – 19, 2012 (October 2012)
13. Sunyong Hwang, Junhyuk Park, Dong-Yeong Kim, Woo Jin Ha, Jong Kyu Kim, Jiuru Xu, Jaehee Cho, and E. Fred Schubert "Promotion of hole injection enabled by GaInN/GaN light-emitting triodes and its effect on the efficiency droop" *International Workshop on Nitride Semiconductors*, IWN 2012, Sapporo, Japan, October 14 – 19, 2012 (October 2012)
14. Jaehee Cho, David S. Meyaard, Sang-Heon Han, Min-Ho Kim, Cheolsoo Sone, and E. Fred Schubert "Temperature dependence of the efficiency droop in GaInN light-emitting diodes" *International Workshop on Nitride Semiconductors*, IWN 2012, Sapporo, Japan, October 14 – 19, 2012 (October 2012)
15. (**Invited presentation**) E. Fred Schubert "Unraveling the mystery of the efficiency droop in GaInN LEDs" *International Workshop on Nitride Semiconductors*, IWN 2012, Sapporo, Japan, October 14 – 19, 2012 (October 2012)
16. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "Tunable-refractive-index materials – A new class of optical thin-film materials with applications in solid-state lighting and solar photovoltaics" *AVS 59th International Symposium and Exhibition*, AVS 2012, Tampa, Florida, October 28 – November 2 (October 2012)
17. (**Invited presentation**) "Light-emitting diodes for lighting applications" E. Fred Schubert, *Lutron Company*, Coopersburg, Pennsylvania, November 5 and 6 (November 2012)
18. Roger E. Welser, Adam W. Sood, Jaehee Cho, E. Fred Schubert, Jennifer L. Harvey, Nibir K. Dhar, and Ashok K. Sood "Nanostructured Transparent Conductive Oxides for Photovoltaic Applications" *MRS 2012 Fall Meeting*, Boston, Massachusetts, November 26 – 30 (November 2012)

**2013**

1. (**Plenary presentation**) E. Fred Schubert "A revolution in lighting: Light-emitting diodes" *Workshop on "Phosphor-free white LEDs for solid-state lighting" McGill University, Montreal, Canada,* January 11 (January 2013)
2. (**Invited short course**) E. Fred Schubert "Light-emitting diodes" *SPIE Photonic West*, San Francisco CA, February 2 – 7 (February 2013)
3. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "Analytic model for the efficiency droop, in light-emitting diodes made of semiconductors with asymmetric carrier-transport properties, based on drift-induced reduction of injection efficiency" *SPIE Photonic West*, San Francisco CA, February 2 – 7 (February 2013)
4. (**Invited presentation**) Jaehee Cho, David S. Meyaard, Jong Kyu Kim, Cheolsoo Sone, and E. Fred Schubert "Temperature-dependent efficiency droop in GaInN light-emitting diodes *SPIE Photonic West*, San Francisco CA, February 2 – 7 (February 2013)
5. (**Invited presentation**) Jaehee Cho and E. Fred Schubert "Temperature dependence of the efficiency droop in GaInN light-emitting diodes" Connecticut Microelectronics and Optoelectronics Consortium (CMOC), Yale University, New Haven, Connecticut, March 13 (March 2013)
6. (**Invited presentation, Shell Graduate Seminar**) E. Fred Schubert "Enabling a Revolution in Lighting: Light-Emitting Diodes" Shell Graduate Seminar, University of Houston, Houston, Texas, April 11 (April 2013)
7. (**Invited presentation**) E. Fred Schubert "Band-edge discontinuities in semiconductor heterostructures – The fundamental building blocks of modern devices" Superlattice Workshop: Development of Man Made Electronic Materials and Devices – Past and Future; University of North Carolina – Charlotte; Symposium in honor of Distinguished Professor Raphael (Ray) Tsu; Charlotte, North Carolina, May 6 (May 2013)
8. (**Plenary presentation**) E. Fred Schubert "Enabling a revolution in lighting: Light-emitting diodes" *Photonics North*, Ottawa, Canada, June 3 – 5 (June 2013)

9. David S. Meyaard, Guan-Bo Lin, Jaehee Cho, E. Fred Schubert, Hyunwook Shirn, Sang-Heon Han, Min-Ho Kim, Young Sun Kim, and Cheolsoo Sone "Correlation between the onset of high injection and the onset of efficiency droop in GaInN light-emitting diodes" *International Conference on Nitride Semiconductors* (ICNS), Washington DC, August 25–30 (August 2014)
10. (**Invited rump-session presentation**) E. Fred Schubert "What causes droop and what are potential solutions?" *Rump Session*, *International Conference on Nitride Semiconductors* (ICNS), Washington DC, August 25–30 (August 2014)
11. (**Invited presentation**) E. Fred Schubert "Challenges in solid-state lighting associated with materials research" *246th American Chemical Society National Meeting*, September 8–12 (September 2013)
12. (**Invited presentation**) E. Fred Schubert and Jaehee Cho "Unraveling mystery of efficiency droop in III-V LEDs" *Second International Conference on Advanced Electromaterials* (ICAE 2013), ICC Jeju, Jeju, South Korea, November 12 – 15 (November 2013)

**2014**

1. Ming Ma, Jaehee Cho, E. Fred Schubert, Gi Bum Kim, and Cheolsoo Sone "Optically functional structures on GaN-based light-emitting diodes for emission pattern control and light-extraction efficiency enhancement" *SPIE Photonic West*, San Francisco CA, February 1 – 6 (February 2014)
2. David S. Meyaard, Guan-Bo Lin, Jaehee Cho, E. Fred Schubert, Hyunwook Shim, Sang-Heon Han, Min-Ho Kim, Cheolsoo Sone, and Young Sun Kim "Identifying the cause of the efficiency droop in GaInN light-emitting diodes by correlating the onset of high injection with the onset of the efficiency droop" *SPIE Photonic West*, San Francisco CA, February 1 – 6 (February 2014)
3. (**Invited short course**) E. Fred Schubert "Light-emitting diodes" *SPIE Photonic West*, San Francisco CA, February 1 – 6 (February 2014)
4. (**Invited presentation**) E. Fred Schubert "The efficiency droop in III-V semiconductor light-emitting diodes" *SPIE Photonic West*, San Francisco CA, February 1 – 6 (February 2014)
5. (**Invited presentation**) Guan-Bo Lin, David S. Meyaard, Jaehee Cho, E. Fred Schubert, Hyunwook Shim, Min-Ho Kim, and Cheolsoo Sone "Correlation between high injection and efficiency droop in GaInN light-emitting diodes" *Connecticut Symposium on Microelectronics and Optoelectronics* (CMOC), University of Connecticut, Storrs CT, April 9 (April 2014)
6. (**Invited presentation**) E. Fred Schubert and Guan-Bo Lin "The efficiency droop in III-V semiconductor light-emitting diodes" Luminus Company, Billerica MA, July 9 (July 2014)
7. (**Invited short course**) E. Fred Schubert and Guan-Bo Lin "Light-emitting diodes" Hualei Optoelectronics Company, Chenzhou, Hunan Province, PR China, August 11 and 12 (August 2014)
8. (**Invited presentation**) E. Fred Schubert and Guan-Bo Lin "The efficiency droop in III-V semiconductor light-emitting diodes" Hualei Optoelectronics Company, Chenzhou, Hunan Province, PR China, August 11 and 12 (August 2014)
9. (**Plenary presentation**) E. Fred Schubert "Progress in understanding and overcoming the efficiency droop in III-V light-emitting diodes" *International Symposium on Semiconductor Light-Emitting Diodes* (ISSLED), Kaohsiung, Republic of China (Taiwan), December 15 – 19 (December 2014)

**2015**

1. Jaehee Cho, E. Fred Schubert, et al. "Temperature dependence of efficiency in GaInN/GaN light-emitting diodes with a strain-control layer" *SPIE Photonic West*, San Francisco CA, February 7 – 12 (February 2015)
2. (**Invited short course**) E. Fred Schubert "Light-emitting diodes" *SPIE Photonic West*, San Francisco CA, February 7 – 12 (February 2015)
3. Guan-Bo Lin and E. Fred Schubert "Efficiency re-climbing in high-current droop regime for GaN-based light-emitting diodes" *Connecticut Symposium on Microelectronics and Optoelectronics* (CMOC), University of Bridgeport, Bridgeport, CT, April 1 (2015)
4. Jaehee Cho, Jong Kyu Kim, E. Fred Schubert "On the temperature dependence of efficiency in III-Nitride light-emitting diodes" *International Conference on Materials for Advanced Technologies*, ICMAT-2015, Suntec, Singapore, June 28 – July 3 (2015)
5. Ashok K. Sood, Gopal Pethuraja, Roger E. Welser, Yash R. Puri, Nibir K. Dhar, Priyalal S. Wijewarnasuriya, Jay Lewis, Harry Efstathiadis, Pradeep Haldar, and E. Fred Schubert "Development of large-area nanostructured

Antireflection coatings for EO/IR sensor applications" *SPIE Optics and Photonics Conference*, San Diego Convention Center, San Diego, California, USA, 9 – 13 August (2015)

**2016**

1. (**Invited short course**) E. Fred Schubert "Light-emitting diodes" *SPIE Photonic West*, San Francisco CA, USA, February 13 – 18 (February 2016)
2. Kyurin Kim, Jun Hyuk Park, Hyunsoo Kim, Jong Kyu Kim, E. Fred Schubert, and Jaehee Cho "Optical and electrical properties of nanostructured indium tin oxide fabricated by oblique-angle deposition" *SPIE Photonic West*, San Francisco CA, USA, February 13 – 18 (February 2015)
3. (**Invited**) E. Fred Schubert "Solid state lighting – The remaining challenges" *CREOL's Industrial Affiliates Symposium 2016*, University of Central Florida, Orlando, Florida, USA, March 10 – 11 (March 2016)

**2017**

4. (**Invited short course**) E. Fred Schubert "Light-emitting diodes" Short Course SC-052, *SPIE Photonic West*, San Francisco CA, USA, January 28 – February 2 (January 2016)