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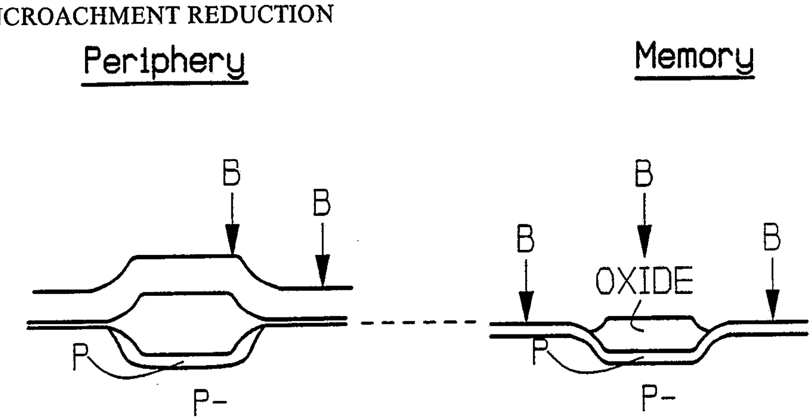

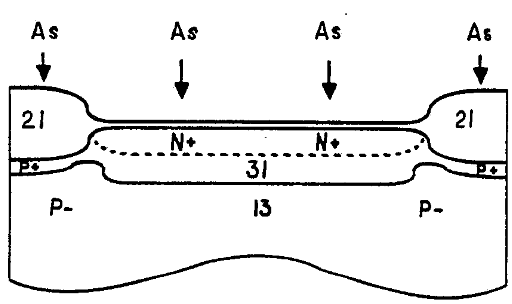

(57) Abstract

Local Encroachment Reduction (LER) is described, in which a fraction of field oxide is selectively etched. A high energy boron implant is used to maintain adequate active area isolation after the removal. This implant also doubles as an LER high ... a carrier to minority substrate electrons. After the high energy boron implant, an N-type bottom plate

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LOCAL ENCROACHMENT REDUCTION

Field of the Invention

This invention relates to fabrication of semiconductor circuit devices and more particularly to techniques for reducing encroachment of field oxide into active area of a semiconductor array during the growth of field oxide. The invention has particular utility in memory arrays such as dynamic random access memories (DRAMs).

Background of the Invention

This invention relates to the manufacture of semiconductor circuit devices. More specifically the invention relates to manufacture of multilayer semiconductor circuit devices in which photomasking steps are used in the manufacture.

The invention uses various materials which are electrically either conductive, insulating or semiconducting, although the completed semiconductor circuit device itself is usually referred to as a "semiconductor". One of the materials used is silicon, which appears as either single crystal silicon or as polycrystalline silicon material, referred to as polysilicon or "poly" in this disclosure.

This invention describes a technique to maximize cell capacitor area in a high density/high volume DRAM (dynamic random access memory) fabrication process. It is called "local encroachment reduction"

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or "LER" for short. The invention is applicable to all high density DRAM planar processes from the 16Kbit to the 4Megbit generations and beyond.

It is well known for high density DRAM process/cell design, that maximum cell capacitor active area must be obtained as a percentage of repeating geometry area in a DRAM array. This active region/repeating region ratio determines the overall die size for a given feature size capability. This then translates directly into cost per bit. The active capacitor region must be large enough to insure proper sensing of data by the bitline sense amps and to insure strong immunity to single event upsets such as alpha particles.

One key factor in maximizing cell capacitor active area is in reducing field oxide encroachment into active area during field oxidation. Encroachment can case a loss of active width up to twice the field ox thickness. As geometries shrink in more advanced generation DRAMs, this effect becomes a dominant factor. A common method of approaching this problem involves use of some sort of field oxidation encroachment reduction technique. Several techniques are discussed in the literature including SWAMI, SILO, BOX, Poly Buffer, Nitrox, trench isolation, and others. Each has their advantages and disadvantages, but all involve adding a great deal of added complexity to the process.

Some prior art processes result in undue crystal stress leading to junction leakage to levels intolerable on DRAM circuits. Others result in large angle abrupt profiles (or even re-entrant profiles in some cases), making anisotropic etch of subsequent

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thin films difficult. Prior art proposed solutions require a gate oxide strip and regrow (or double strip and regrow) to form the final gate oxide. This has a disadvantage of thinning the field isolation oxide and adds extra process steps. Some of the other methods involve a Si etch into Si substrate, which requires extra precaution during subsequent process steps to avoid generation of stacking faults and other crystal defects.

Other encroachment reduction schemes are more susceptible to isolation leakage due to the reduction in the active area N+ space. Increasing the standard field implant has other performance degradation implications and is therefore not desirable. These degradations include increased N+ junction capacitance and aggravated transistor narrow W effects. The LER approach embodied here suffers from none of the above limitations.

The purpose of this invention is to describe a simple yet extremely effective means of increasing cell capacitor area in an advanced DRAM process called "local encroachment reduction" or "LER". It involves reducing the encroachment of the field ox into the cell active area only locally in the cell active regions. It avoids all the pitfalls of prior art encroachment reduction schemes.

<u>Summary of the Invention</u>

The invention utilizes photomasking to define only the regions where the capacitor active area is to be and all field ox isolation regions between cell capacitor active regions. A wet oxide etch is then

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