200 mm Process Integration for a 0.15 μm Channel-Length CMOS Technology Using Mixed X-Ray / Optical Lithography

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ABSTRACT

In this work, an integrated 0.35 μm CMOS technology with 0.15 μm effective channel length (L_{EFF}) is demonstrated in a 200 mm line. X-ray lithography is used for the critical gate level, along with conventional deep-UV and mid-UV lithography for other levels. Shallow Trench Isolation (STI) is used to achieve 0.35 μm design rules. The NFET and PFET devices are designed for operation with a scaled power supply of 1.8 V. This technology provides 50% performance improvement relative to a 2.5V, 0.5 μm design rule, 0.25 μm L_{EFF} high-performance CMOS technology.

INTRODUCTION

Achieving a technology with nominal electrical channel length (L_{EFF}) of 0.15 μm [1] requires gate lithography with a nominal dimension of 0.20-0.25 μm. In addition, for 0.35 μm high-performance, high-density logic, the key technology issues to be considered are 0.35-0.40 μm isolation, 4.0-5.0 nm gate dielectric integrity, shallow implanted S/D junction formation for acceptable device rolloff, gate conductor resistance and borderless contact/ local interconnect formation for high density [2][3].

PROCESS

A shallow-trench process (STI) [4] is used to achieve an isolation thickness of 0.35 μm from infinite width down to 0.40 μm spaces. After the isolation trench is etched in the silicon and filled with LPCVD TEOS, a combination of resist planarization, RIE, and chemo- mechanical polish is used to form the oxide isolation. After growing the screen oxide, the wells are implanted. Non-uniform well profiles are used in order to obtain acceptable on-current and threshold voltage rolloff [1].

For the critical gate-level lithography, we have employed X-ray lithography using a synchrotron source and a 200mm wafer aligner with a stage capable of < 0.20 μm mix and match overlay. A 1.0 μm chemically-amplified positive resist (APEX) is used. This X-ray exposure facility allows routine integration of a single-level X-ray exposure for images down to 0.125 μm with conventional 0.35 μm DUV process capability at a much higher level of throughput than electron-beam lithography systems can provide. The X-ray mask was fabricated using a 0.6 μm gold absorber with pattern sizes down to 0.125 μm on a 18 mm x 32 mm field size. Fig. 1 shows the resultant resist profile for a typical 0.20 μm line. Table 1 summarizes image CD data for 0.125 and 0.20 μm features. Fig. 2 shows an image placement error plot for demonstrating an average overlay error less than 100nm with a worst case overlay of 124nm for a 123 site measurement sample. Fig. 3 shows an SEM view of the 0.2 μm gates (with sidewall spacer). Fig. 4 shows a TEM cross-section of a completed device (L_{MASK} = .20 μm) Figure 5 shows excellent across-wafer L_{EFF} distribution for NFETs achieved for a nominal effective channel length of 0.15 μm with X-ray lithography. A W-stud local interconnect (< 1 Ω/sq.) with borderless contact to isolation provides wiring for embedded SRAM and high-density logic applications [2],[3].

For an effective channel length of 0.15 μm, a gate oxide thickness of about 5 nm and shallow source-drain junctions with a depth of 60-80 nm are required. The corresponding power-supply voltage would be 1.8V [5]. The viability of a 5 nm gate oxide in a fully integrated process is demonstrated by the gate leakage histograms for NFET and PFET shown in Figure 6. One of the challenging integration issue for 0.15 μm CMOS is the controlled fabrication of sub-100 nm S/D junctions.

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We have chosen to explore the extension of conventional ion-implantation techniques in order to fully utilize existing fabrication capabilities for this generation. Figure 7 shows resultant SIMS profiles for shallow n-type and p-type junctions fabricated using Ge pre-amorphization to control channelling and annealed with a 1000°C rapid thermal anneal. This figure also shows the halo implants that are used for short channel effect (SCE) control. Fig. 8 shows short channel threshold voltage ($V_{T,SAT}$, V_{DD} = 1.8V) for NFETs and PFETs respectively. Both NFET and PFET devices exhibit $V_{T,SAT}$ rolloff of less than 225 mV down to channel lengths of about 0.12 μm. The halo implants also sharpen the dopant profile on the shallow S/D as a means to both improve short channel behavior and reduce the parasitic resistance.

Key concerns for 0.15 μm devices using implanted S/D extensions is their leakage behaviour with limited annealing cycles and silicidation for series resistance reduction. Figure 9 shows the leakage current histograms for N-junctions with only a 1000°C anneal. Figure 10 shows the leakage current histogram for P-junctions, with a larger tail. The overall leakage contribution to off-current is still negligible, however. Figure 11 shows the $I_{ON} - I_{OFF}$ tradeoff for NFETs and PFETs and indicates acceptable off-current behavior for nominal 0.15 μm NFET and PFET devices, with on-currents of 0.45 mA/μm and 0.22 mA/μm respectively ($V_{DD} = 1.8V$). We have used a thick sidewall to position deep junctions which can be salicided to reduce device series resistance and contact resistance. The resultant transconductance $G_{M,SAT}$ at 1.8V is 350 mS/mm for NFET and 180 mS/mm for PFET while the external resistances are 340 and 570 ohm-μm respectively. The gate conductor sheet resistance distribution for both $TiSi_2$ salicide and polycide device structures at 0.25 μm linewidth is shown in Fig. 12. Here, the performance improvement for the polycide structure must be balanced against the additional process complexity of the gate stack.

The delay vs. supply voltage behavior shown in Figure 13 for both standard CMOS and pass-transistor logic gates demonstrate the low-voltage and low-power performance potential for this technology. Figure 14 shows the delay for unloaded (FI=FO=1, C_L = 0) and loaded (FI=FO=3, C_L = 165fF) ring oscillators as a function of channel length. The minimum delays of 30 ps unloaded and 150 ps loaded at 1.8V represent about 50% performance improvement relative to a state-of-the-art 2.5 V, 0.25 μm L_{EFF} high-performance CMOS technology [2] These results highlight the application of mixed X-ray/DUV lithography for evaluation of 200mm process integration for 0.15μm L_{EFF} CMOS devices.

SUMMARY

In summary, we have used X-ray lithography for the gate level to enable fabrication of CMOS devices with 0.15 μm nominal effective channel length, integrated with shallow trench isolation using 0.35 μm design rules in a 200mm process targeted for operation with a scaled power supply of 1.8 V. This technology provides about 50% performance improvement relative to a 2.5V, 0.5 μm design rule, 0.25 μm L_{EFF} CMOS technology [2]. This technology is suitable for high-end microprocessors with embedded high-speed SRAM cache.

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† On business leave of absence to LORAL, FSC.

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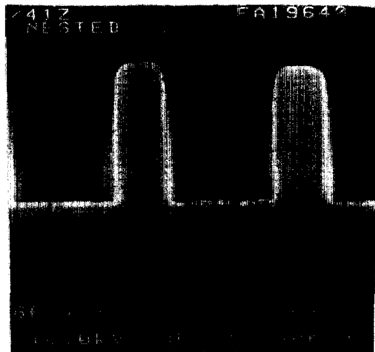


Fig. 1. SEM image of 0.20um features in 1.0um APEX.

Table 1. SEM Data/ 8 chips per wafer			
Wafer	**Design**	**Actual**	**3 σ**
3	125nm	137nm	15nm
19	125nm	132nm	22nm
3	200nm	175nm	19nm
19	200nm	175nm	8nm
4	200nm	181nm	12nm
8	200nm	181nm	23nm
10	200nm	184nm	21nm
16	200nm	182nm	18nm
18	200nm	179nm	8nm
20	200nm	180nm	10nm

Table 1. Image CD data summary for 0.125 μm and 0.20 μm features.

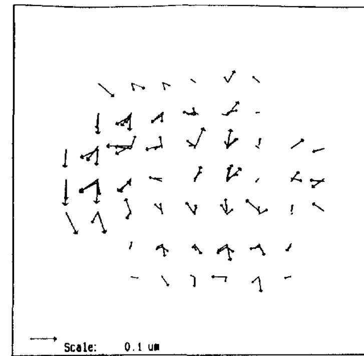


Fig. 2. Overlay vectors XRAY/DUV mix-and-match.

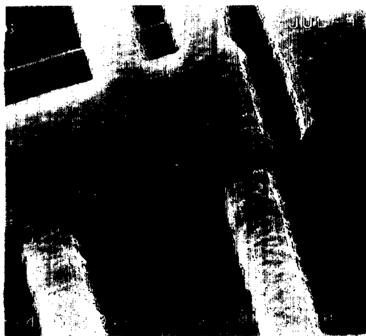


Fig. 3. SEM showing 0.2μm gates crossing over STI to silicon (with 0.12 μm spacer).

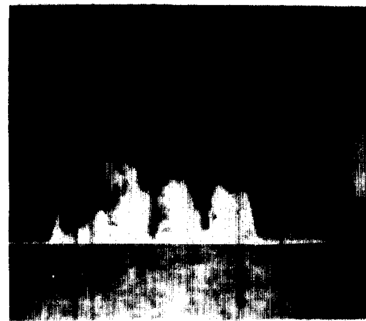


Fig. 4. Cross-section TEM of completed 0.20 μm L_{MASK} device.

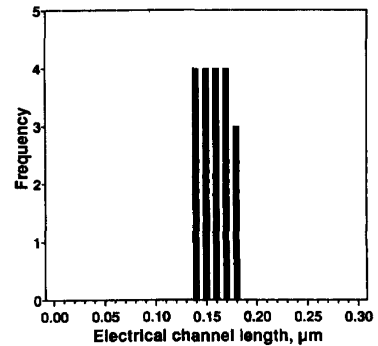
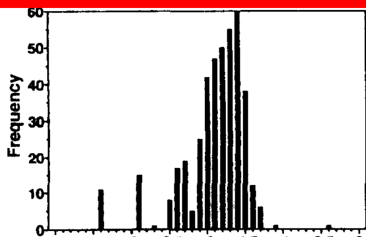


Fig. 5. Electrical channel-length distribution (20 chips, across wafer).



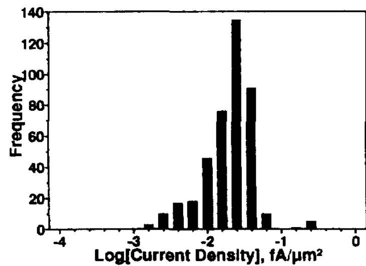
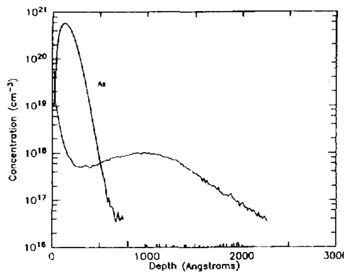


Fig. 6. Gate oxide leakage histograms for N (top) and P (bottom) capacitors.



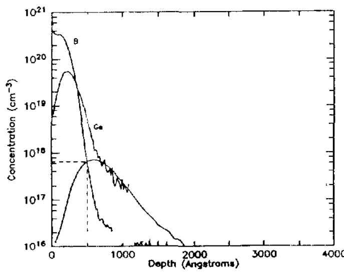
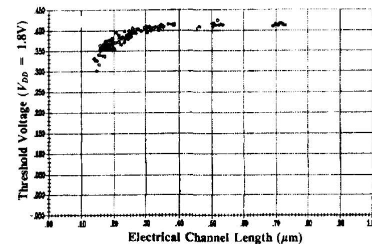


Fig. 7. SIMS profiles of N-extension (top) and P-extension (bottom).



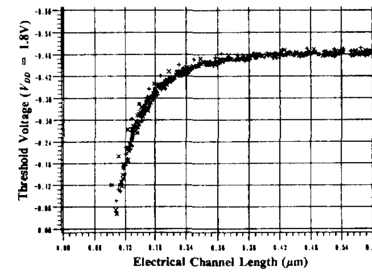


Fig. 8(a). Threshold voltage as a function of channel length for NFETs (top) and PFETs (bottom).

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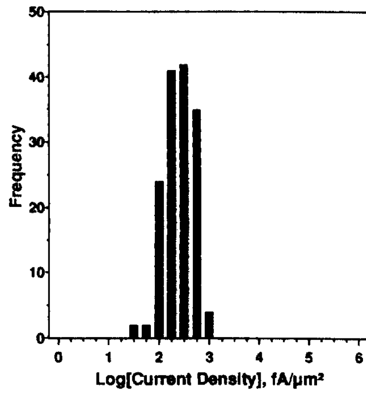


Fig. 9. Junction leakage histogram for N-junction.

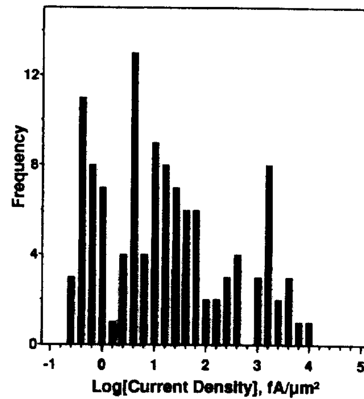
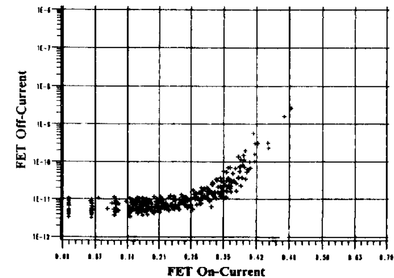


Fig. 10. Junction leakage histogram for P-junction.



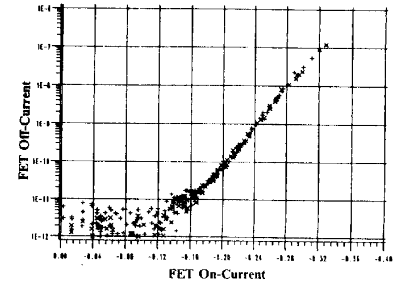


Fig. 11. Off current as a function of on-current for NFETs (top) and PFETs (bottom).

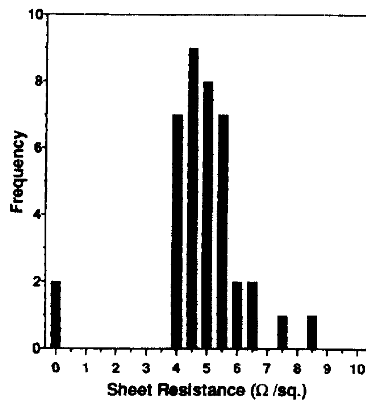


Fig. 12(a). Gate conductor Sheet resistance for 0.25 μm **Salicide** lines.

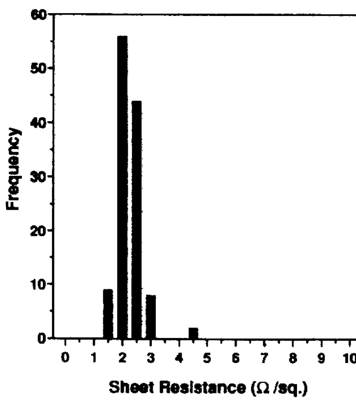


Fig. 12(b). Gate conductor Sheet resistance for 0.25 μm **Polycide** lines.

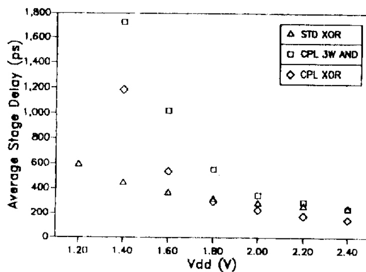


Fig. 13. Ring-oscillator delay for standard and pass-transistor logic ring oscillators.

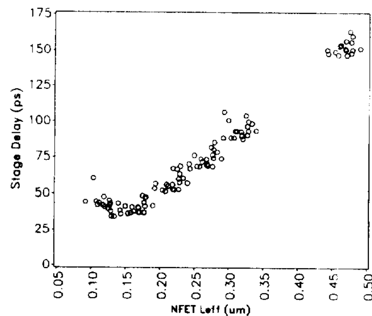


Fig. 14(a). Ring-oscillator delay for unloaded inverters (FI = FO = 1)

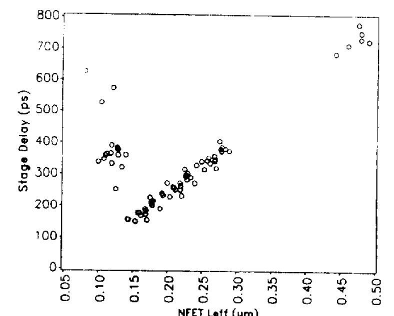


Fig. 14(b). Ring-oscillator delay for loaded gates (2-way NAND, FI = FO = 3, C_L = 165 fF).

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