

Figure 3.5.11 shows the TEM-EDS spectrum of the NiSi used on the polysilicon gates.

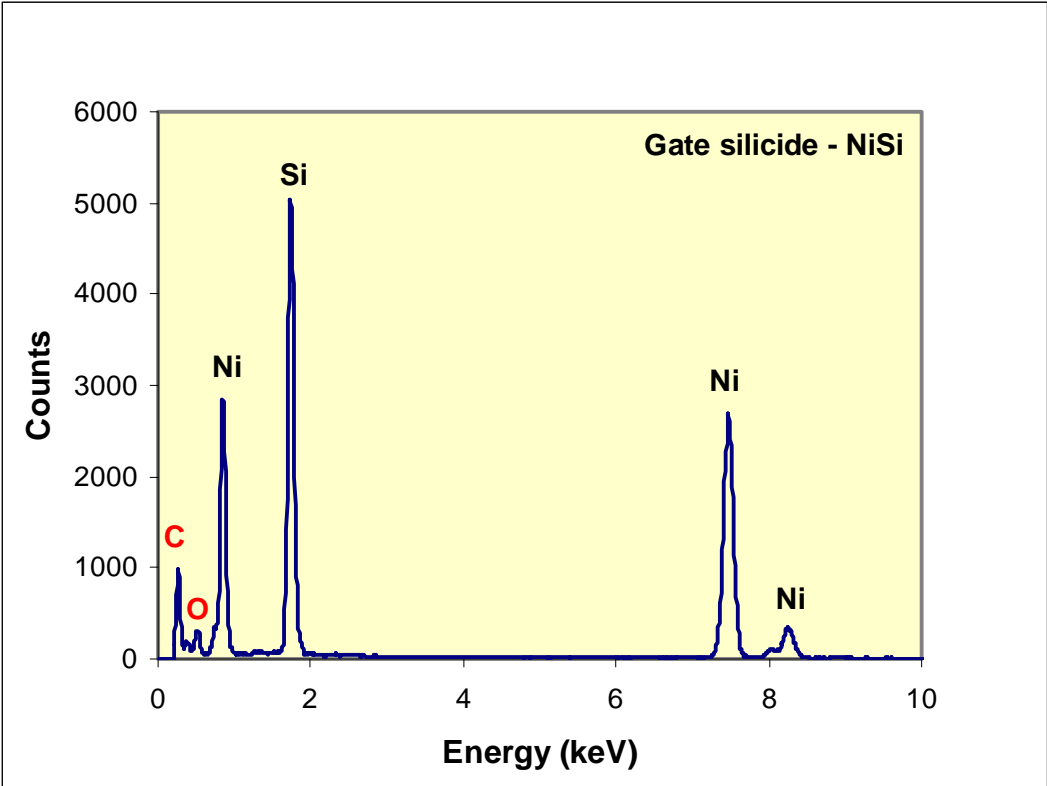


Figure 3.5.11 TEM-EDS Spectrum of Gate Silicide

### 3.6 Isolation

The XXXX uses shallow trench isolation (STI). The minimum width STI used on the part is 0.10  $\mu\text{m}$  wide. The observed dimensions of the STI are listed in [Table 3.6.1](#).

Feature	Size ( $\mu\text{m}$ )
Minimum width STI	0.10
STI thickness - beneath poly	0.32
STI thickness - beneath field	0.27

**Table 3.6.1 Observed Isolation Dimensions**

Figure 3.6.1 shows a TEM image of the 0.10  $\mu\text{m}$  minimum width STI.

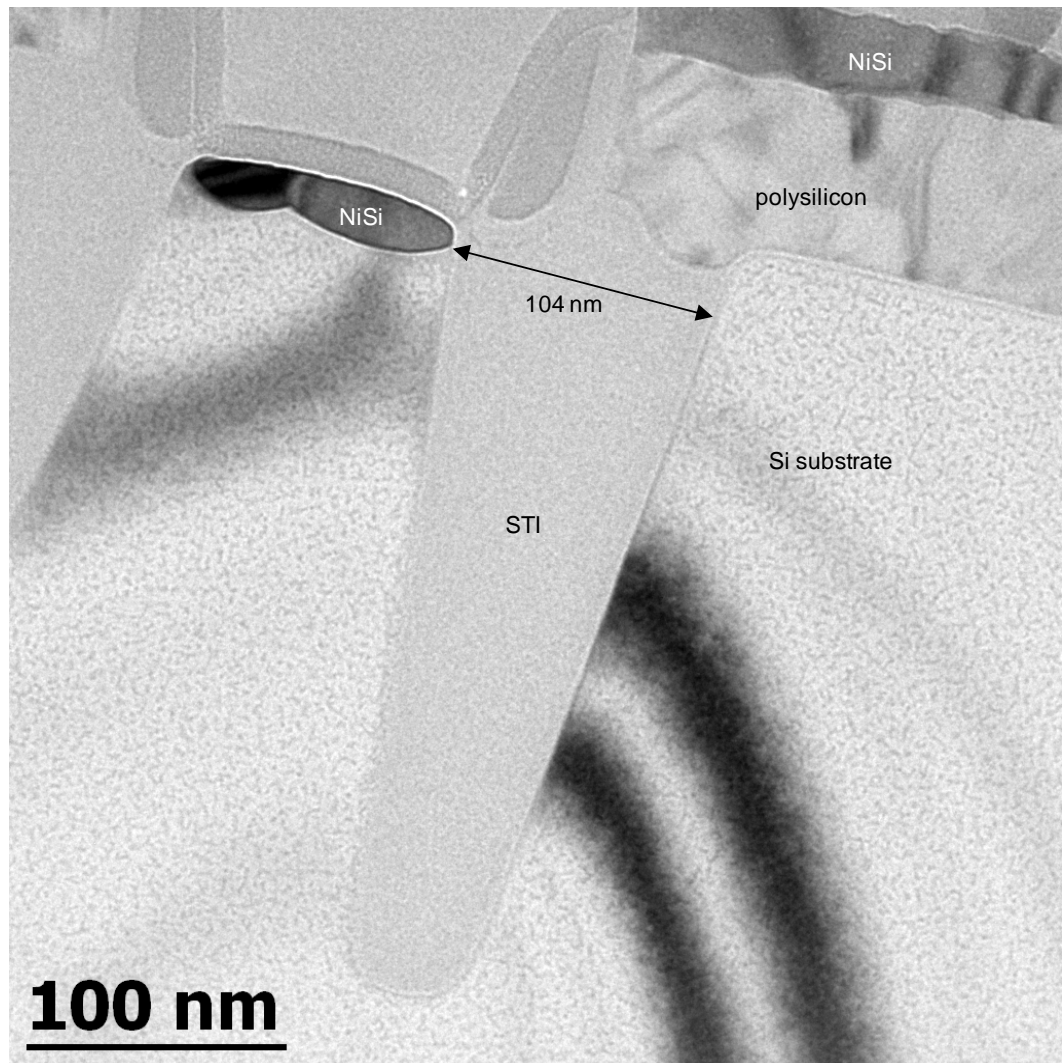


Figure 3.6.1 Minimum Width STI – TEM

Figure 3.6.2 shows the STI thickness. The STI is 0.32  $\mu\text{m}$  thick beneath the polysilicon lines, and 0.27  $\mu\text{m}$  thick where it was not protected during the sidewall spacer over etch.

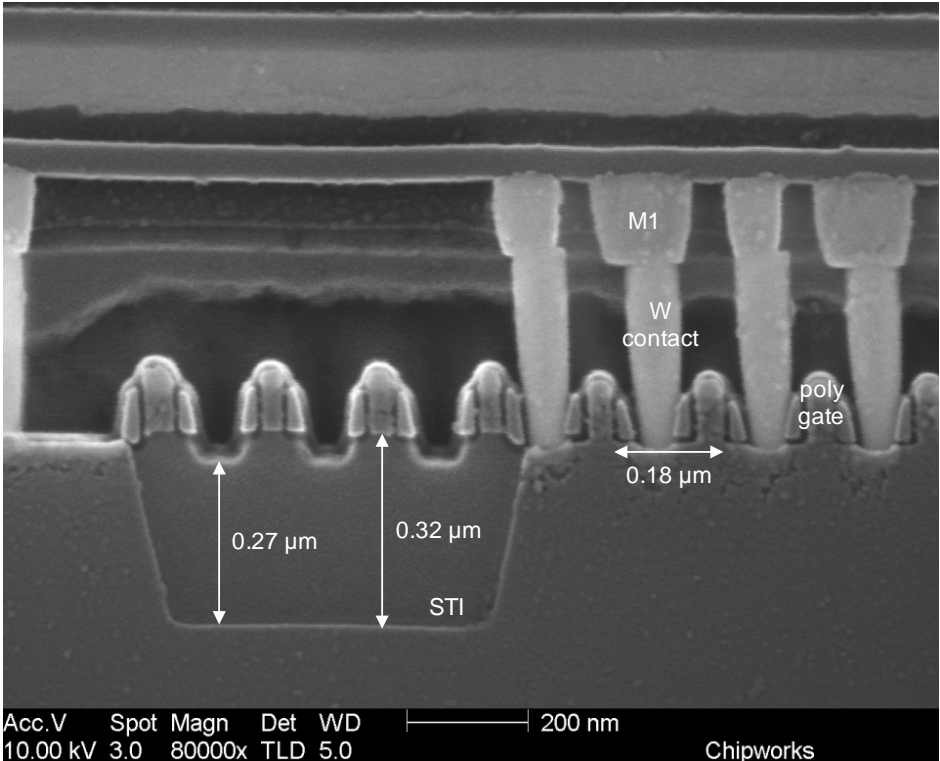


Figure 3.6.2 STI Thickness – TEM

Figure 3.6.3 shows a TEM view of poly over the 0.32  $\mu\text{m}$  thick STI.

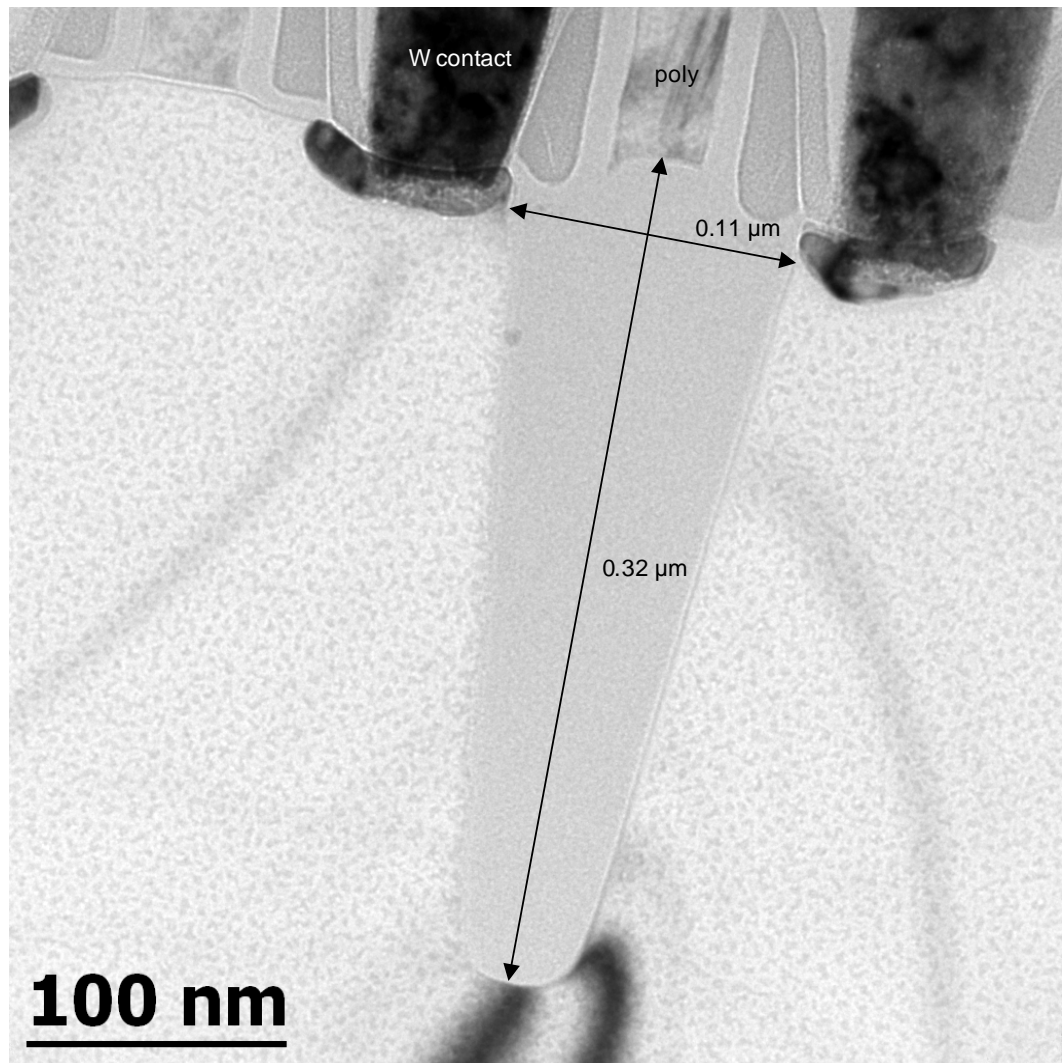


Figure 3.6.3 STI Beneath Poly – TEM

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