Figure 3.3.9 shows a TEM view of a metal 3 line. The liner is about 7 nm thick along the trench sidewalls and trench bottom. The timed metal trench etch has produced a notched profile along the trench bottoms.

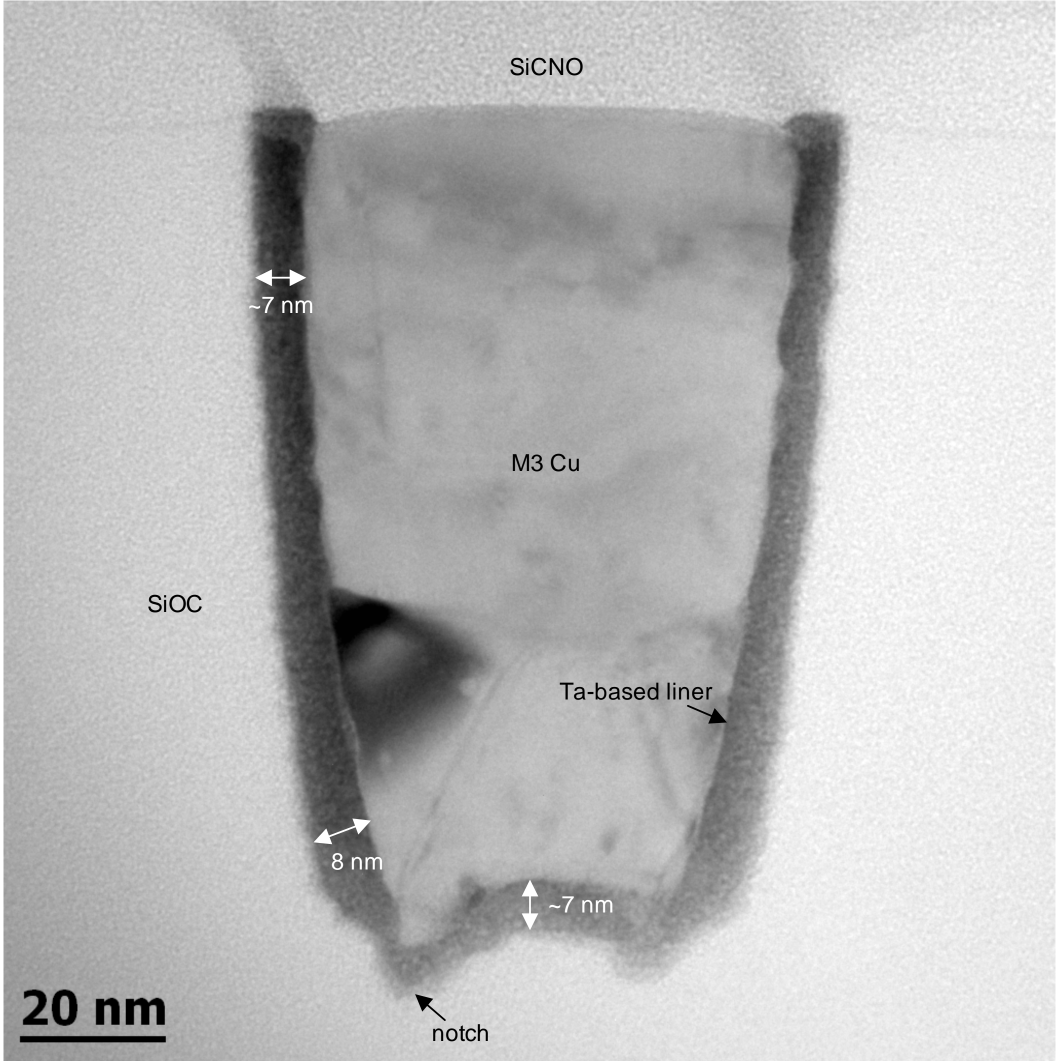

Figure 3.3.9 Metal 3 Liner – TEM

Figure 3.3.10 shows the 0.14 μm minimum pitch metal 2 and metal 4 lines. The metal 4 lines are slightly thinner than the underlying metal 1 through metal 3 lines.

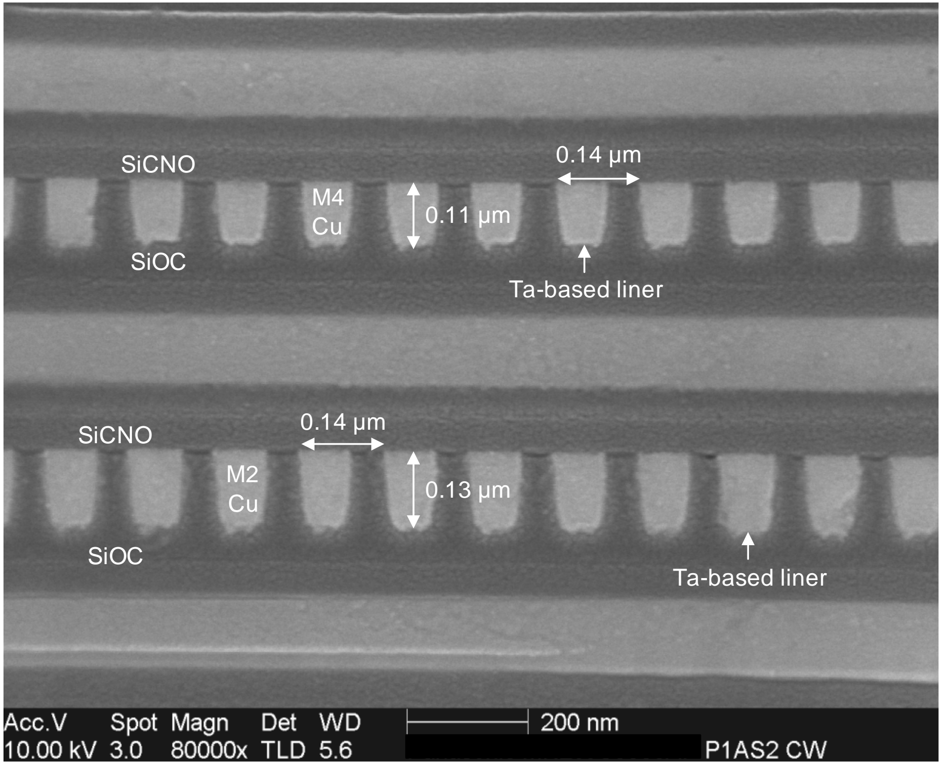

Figure 3.3.10 Minimum Pitch Metal 2 and 4

Figure 3.3.11 shows a TEM view of a pair of metal 2 lines. The Ta-based liner is about 8 nm thick along the trench sidewalls and trench bottom. The metal trench etch has also produce a notched profile on the bottom of these lines.

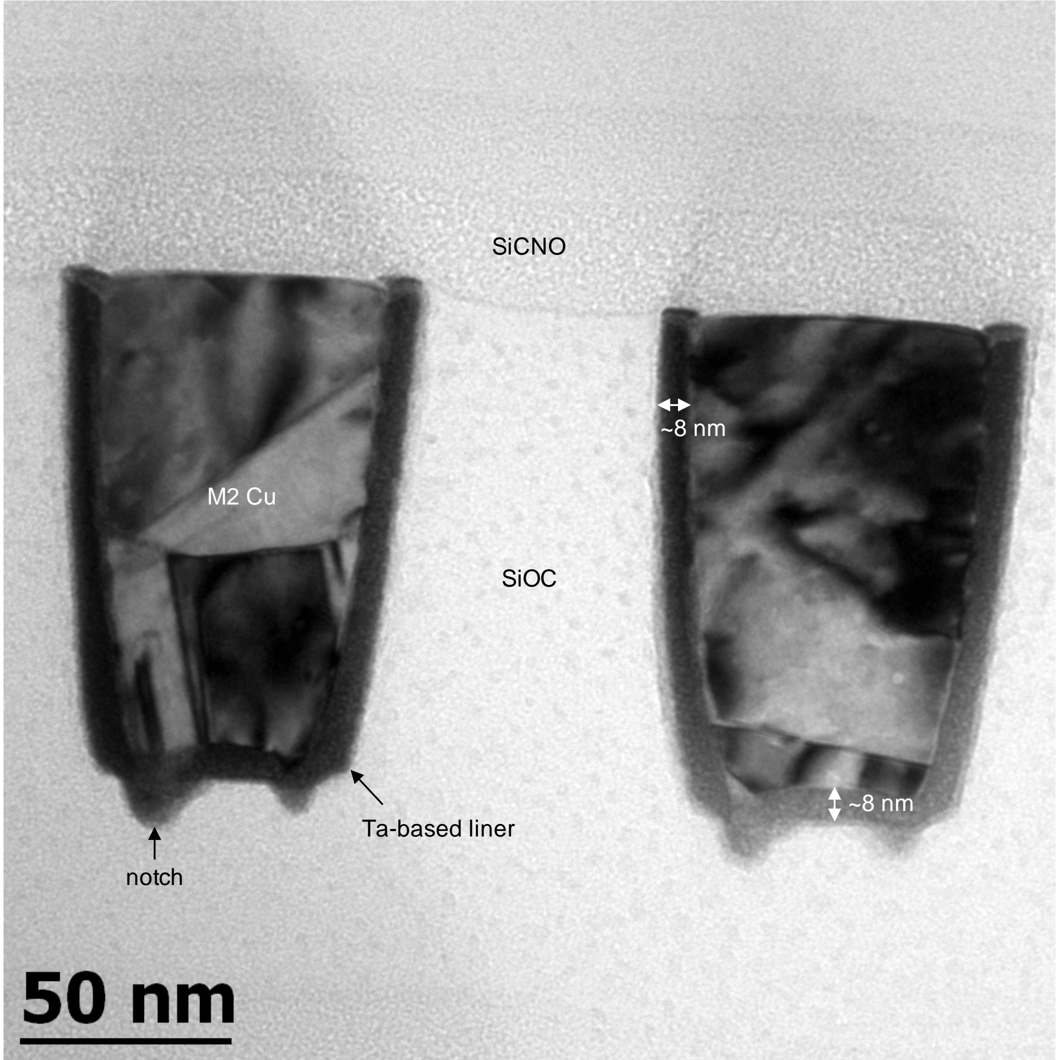

Figure 3.3.11 Metal 2 Liner – TEM

Figure 3.3.12 shows a series of 0.14 µm minimum pitch metal 1 lines. Metal 1 uses the PMD 5 SiOC as the line dielectric, and is capped with SiCNO after the CMP polish. A timed etch was used for the dielectric trench etch ending in the oxide PMD 4.

The Ta-based liners are very thin, and it is not entirely clear as to how effective a barrier they will be to Cu diffusion, so the long term reliability of the device may be in question. The liner thickness on this part is, however, consistent with the liner metal 1 liner thickness used on Intel's 45 nm process.

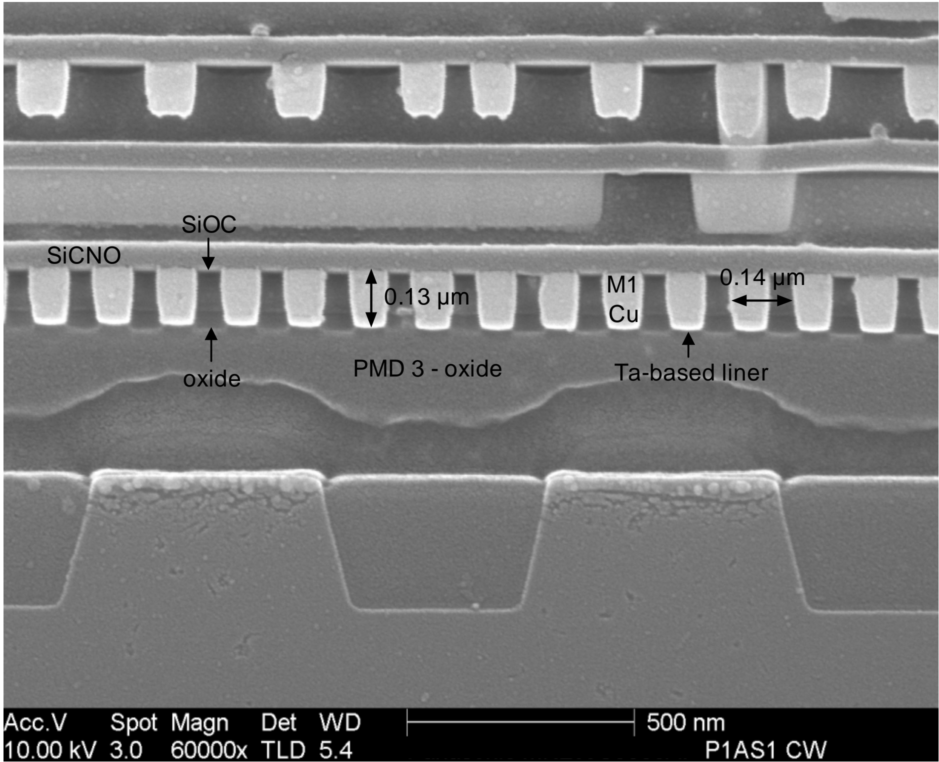

Figure 3.3.12 Minimum Pitch Metal 1

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Figure 3.3.13 shows a TEM image of a pair of metal 1 lines. The Ta-based liner ranges from about 2 nm thick along the sidewalls to about 10 nm thick along the trench bottom.

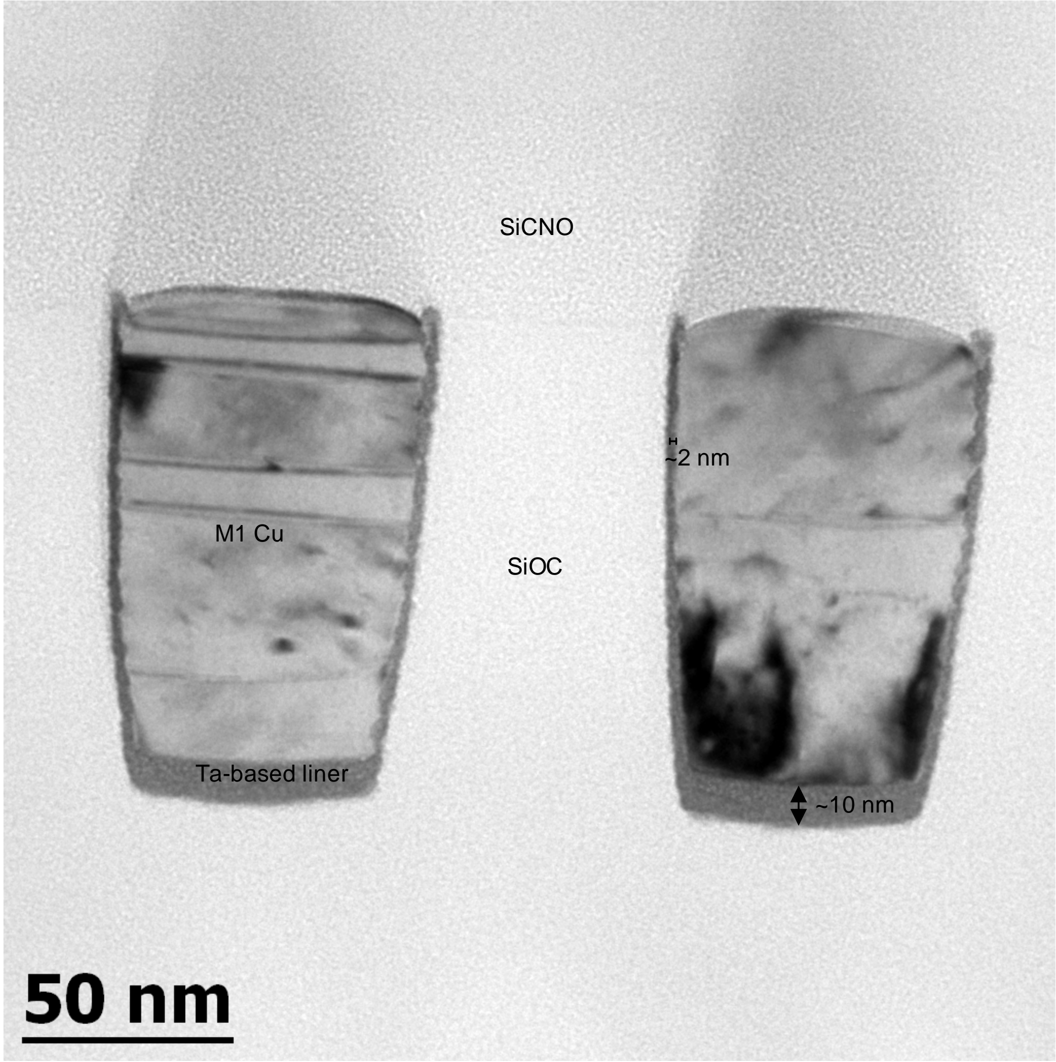

Figure 3.3.13 Metal 1 Liner

Figure 3.3.14 shows the TEM-EDS spectrum of the metal 9 Al body.

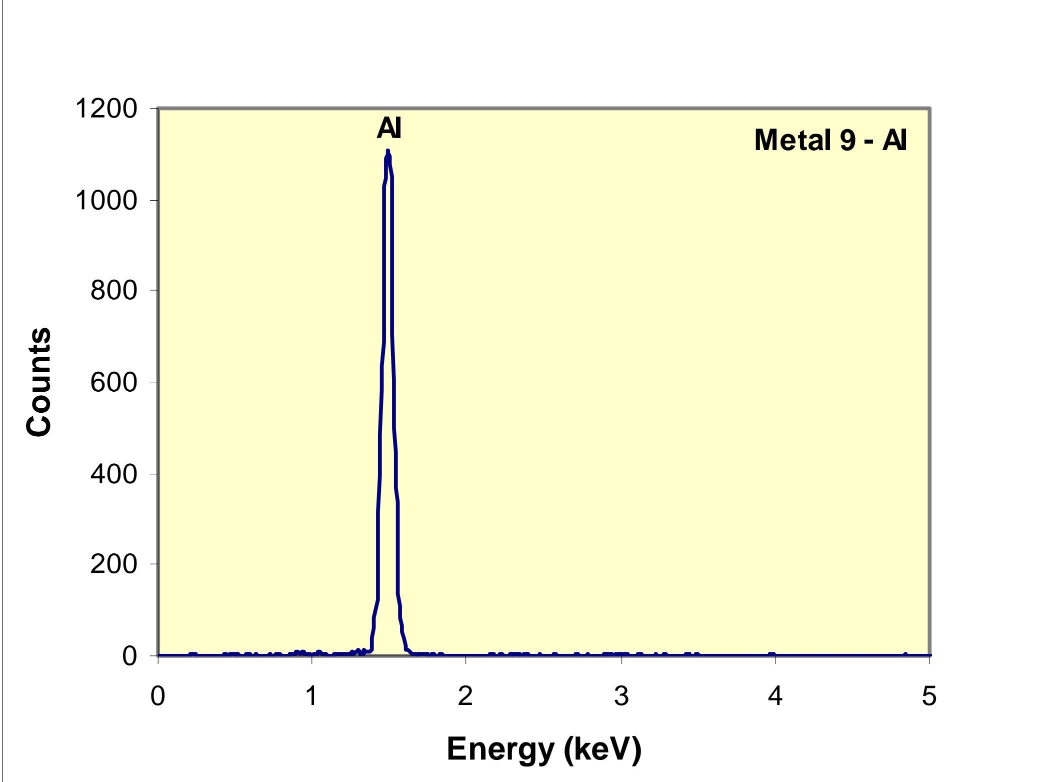

Figure 3.3.14 TEM-EDS Spectrum of Metal 9 Body

Figure 3.3.15 shows the TEM-EDS spectra of the metal 9 TiN/Ti barrier metals.

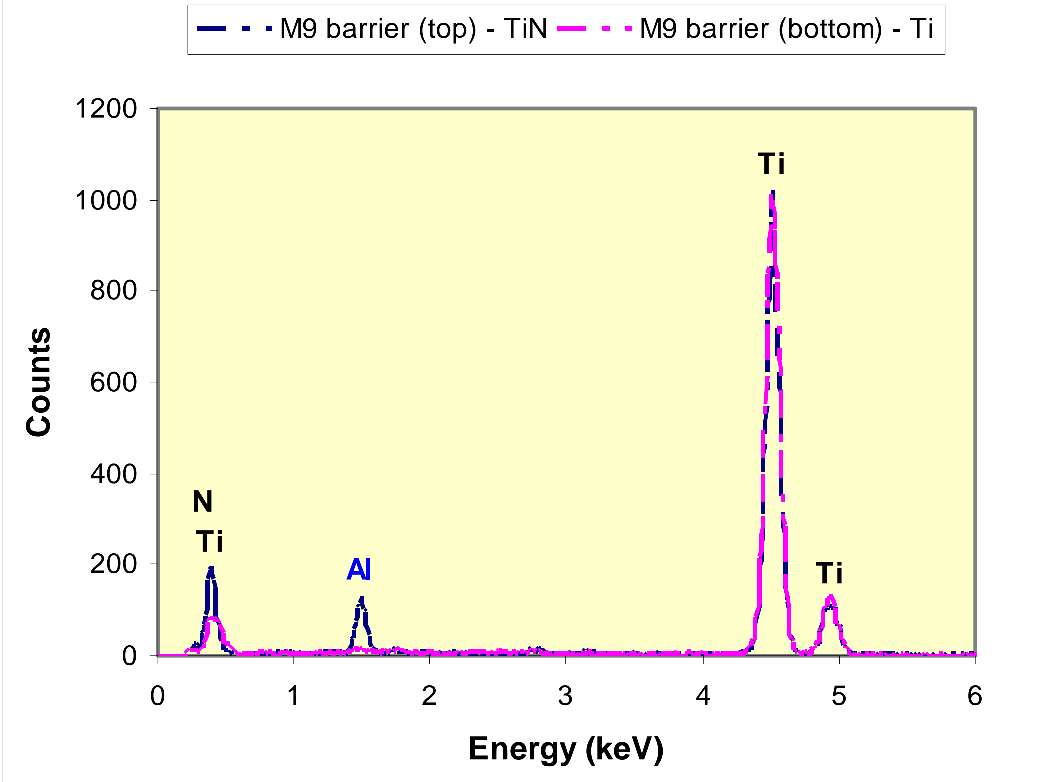

Figure 3.3.15 TEM-EDS Spectra of Metal 9 Barrier Layers

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Figure 3.3.16 shows the TEM-EDS spectra of the metal 1 Ta-based liner, likely TaN. This spectrum is representative of the metal 1 through metal 8 liners.

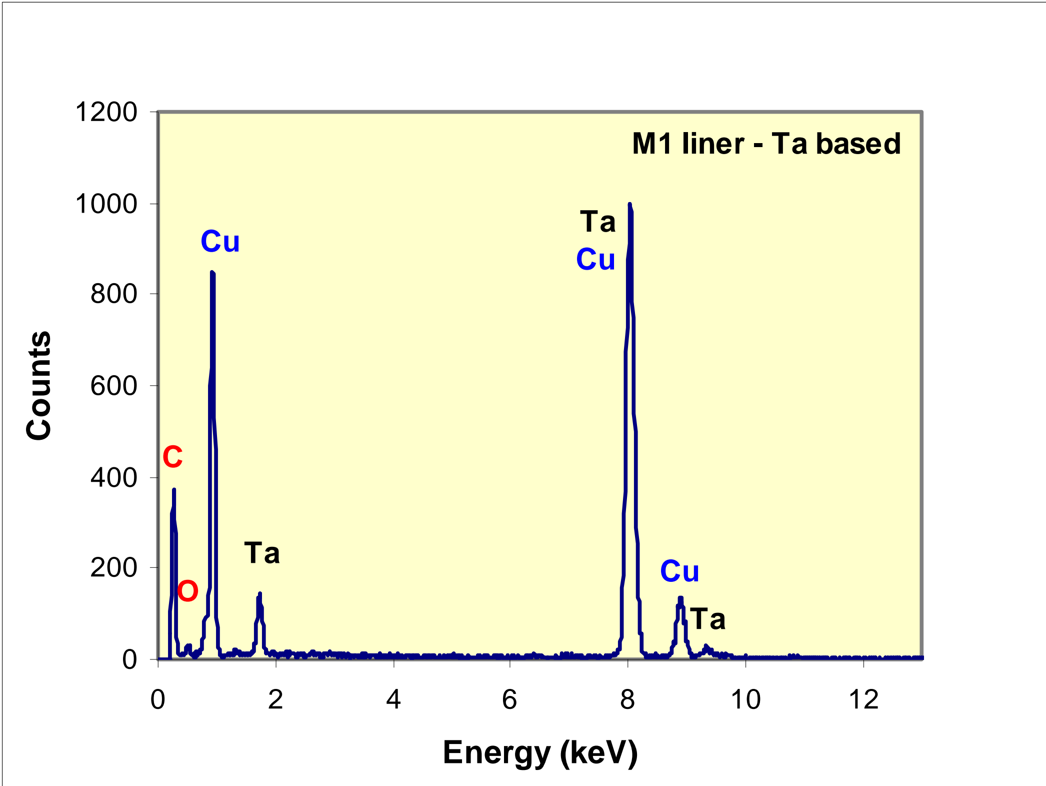

Figure 3.3.16 TEM-EDS Spectrum of Metal 1 Barrier

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3.4 Vias and Contacts

The XXXX uses conventional Al vias to interconnect metal 8 and 9. Cu vias are used for the via 1s through via 7s, using a via first process as part of the dual damascene Cu line formation. The contacts to poly and diffusion are comprised of TiN lined, W filled contact studs. Butted contacts are used in the 6T SRAM to reduce the unit cell size. Plan view images of these are presented in Section X.

Table 3.4.1 lists the minimum width and pitch of the vias and contacts. These values were derived from measurements made at the via/contact interface with the underlying metal or diffusion.

Layer	Width (µm)	Space (µm)	Pitch (µm)
Via 8	6.0	6.8	12.8
Via 7	0.54	1.29	1.83
Via 6	0.51	1.23	1.74
Via 5	0.16	0.18	0.34
Via 4	0.08	0.09	0.17
Via 3	0.08	0.07	0.15
Via 2	0.08	0.06	0.14
Via 1	0.08	0.06	0.14
Contacts	0.07	0.07	0.14

Table 3.4.1 Via and Contact Horizontal Dimensions

Figure 3.4.1 shows the 6.0 μm wide, 12.8 μm minimum pitch via 8s.

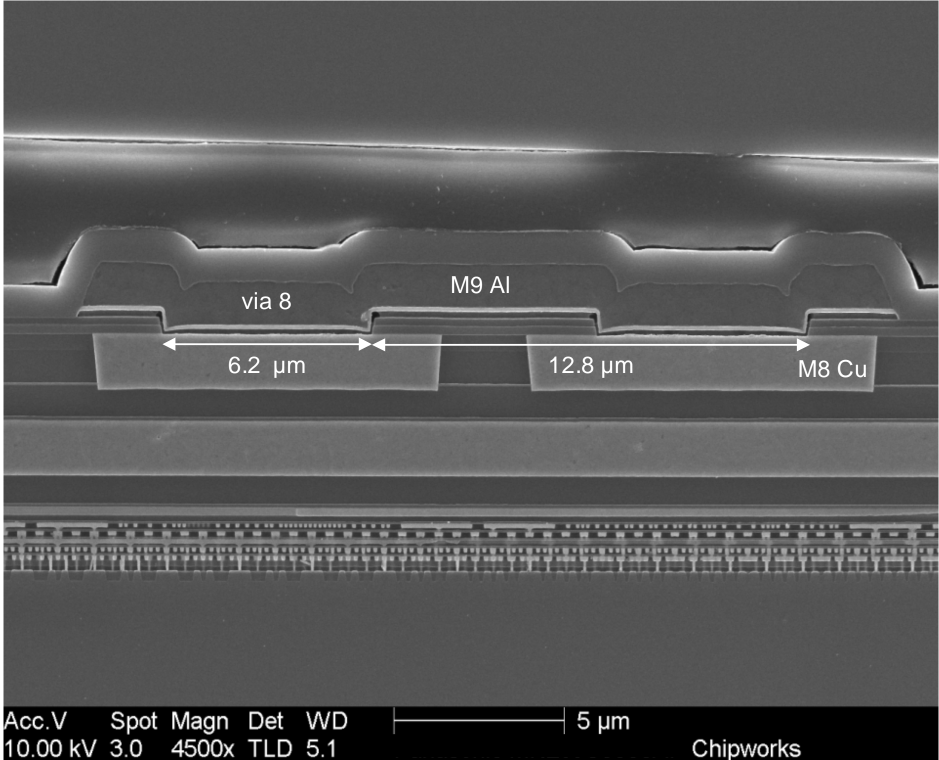

Figure 3.4.1 Minimum Pitch Via 8s

Figure 3.4.2 shows the 0.54 µm wide, 1.83 µm minimum pitch via 7s. While these are the minimum observed pitch, the lithography is capable of quite finer pitches, as small as perhaps 1 µm.

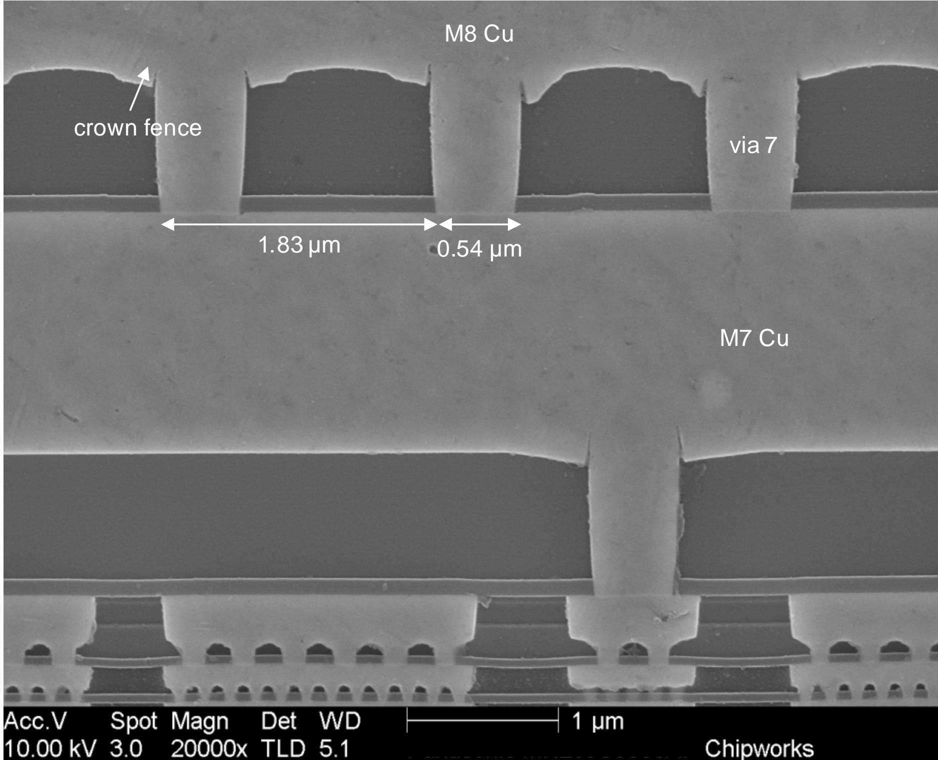

Figure 3.4.2 Minimum Pitch Via 7s

Figure 3.4.3 shows the 0.51 µm wide, 1.74 µm minimum pitch via 6s. Like the via 7s, the via 6 lithography is likely capable of finer pitches.

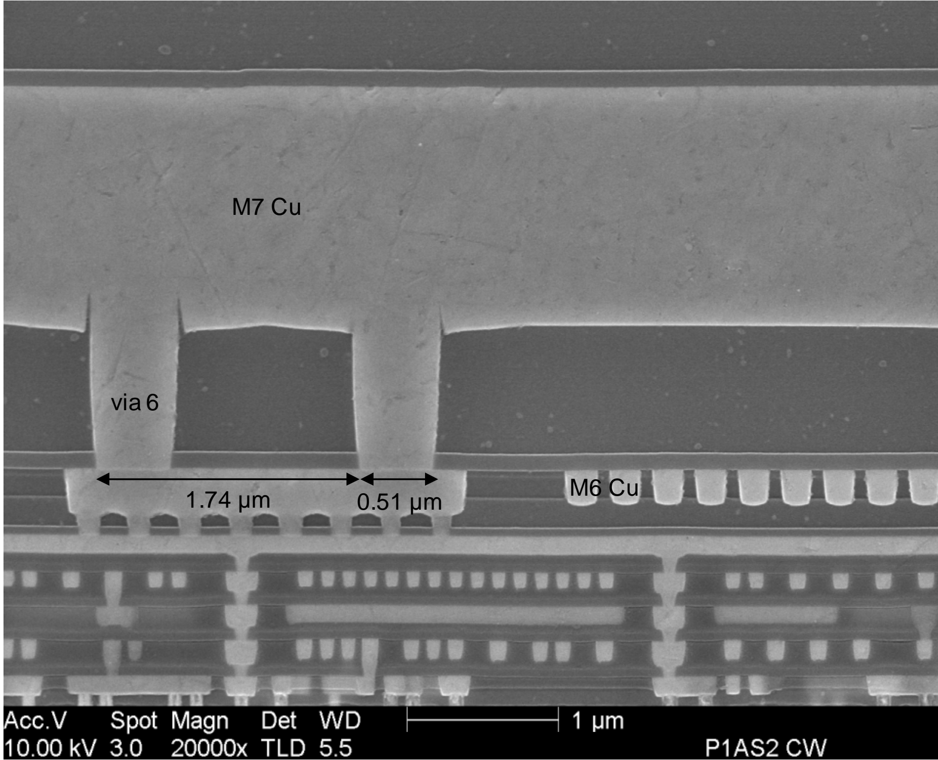

Figure 3.4.3 Minimum Pitch Via 6s

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Figure 3.4.4 shows the 0.16 µm wide, 0.34 µm minimum pitch via 5s.

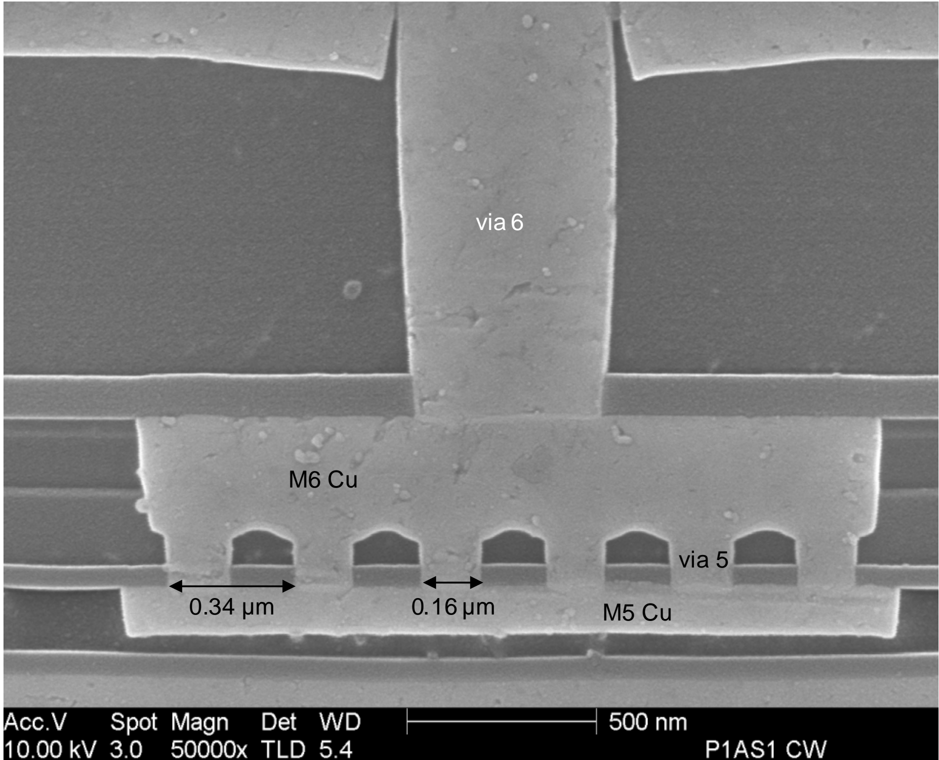

Figure 3.4.4 Minimum Pitch Via 5s

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Figure 3.4.5 shows a TEM image of a single via 5. The via 5 etch has just penetrated the surface of the metal 5 line.

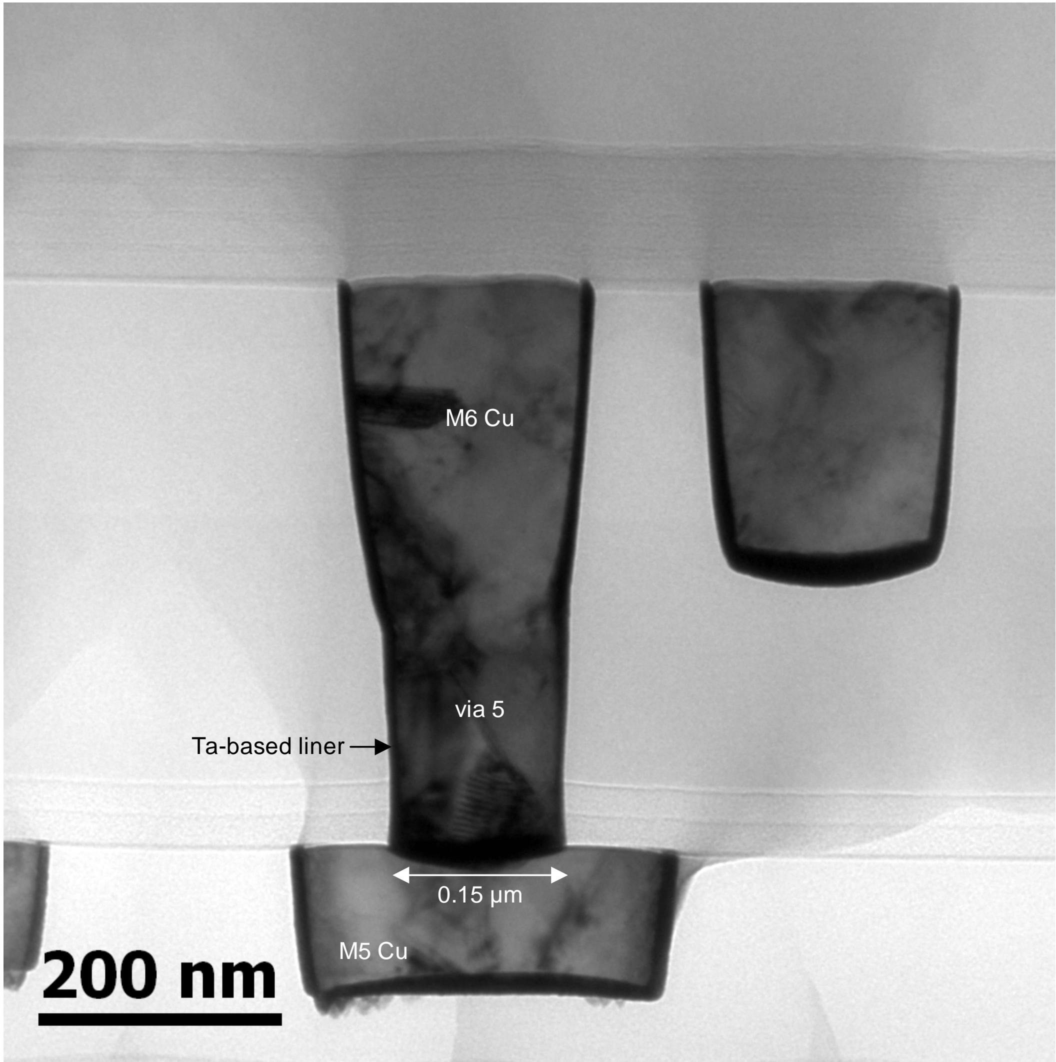

Figure 3.4.5 Via 5 – TEM

Figure 3.4.6 shows the 0.15 µm minimum pitch via 3s and 0.17 µm minimum pitch via 4s.

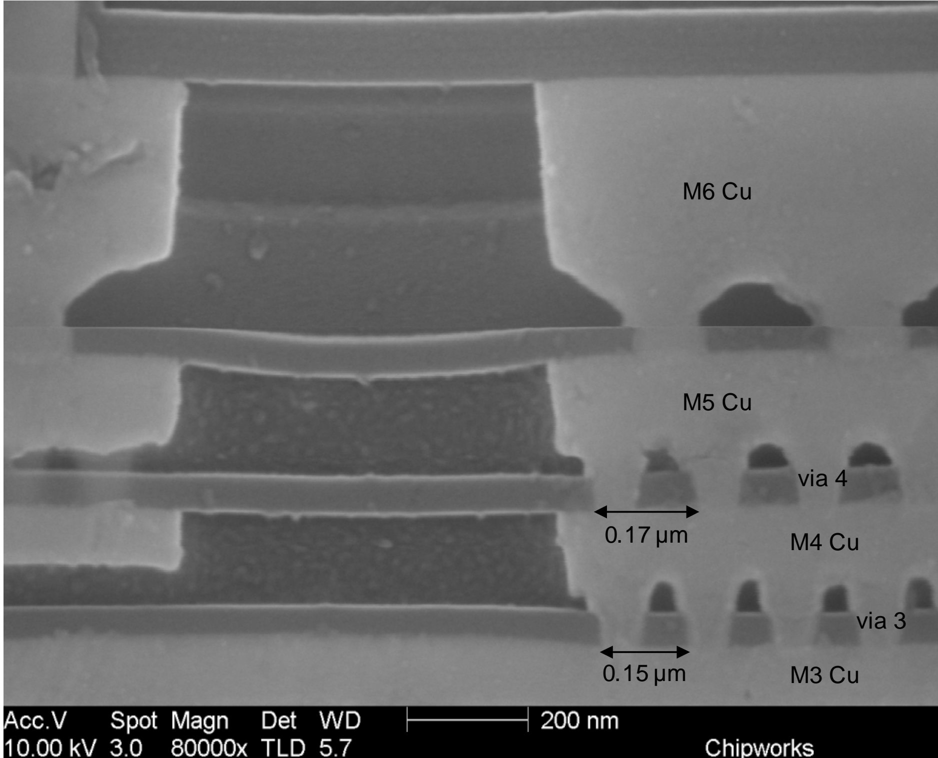

Figure 3.4.6 Minimum Pitch Via 3s and 4s

Figure 3.4.7 shows a TEM image of a single via 4. The via 4 etch has penetrated about 25 nm into the surface of metal 4.

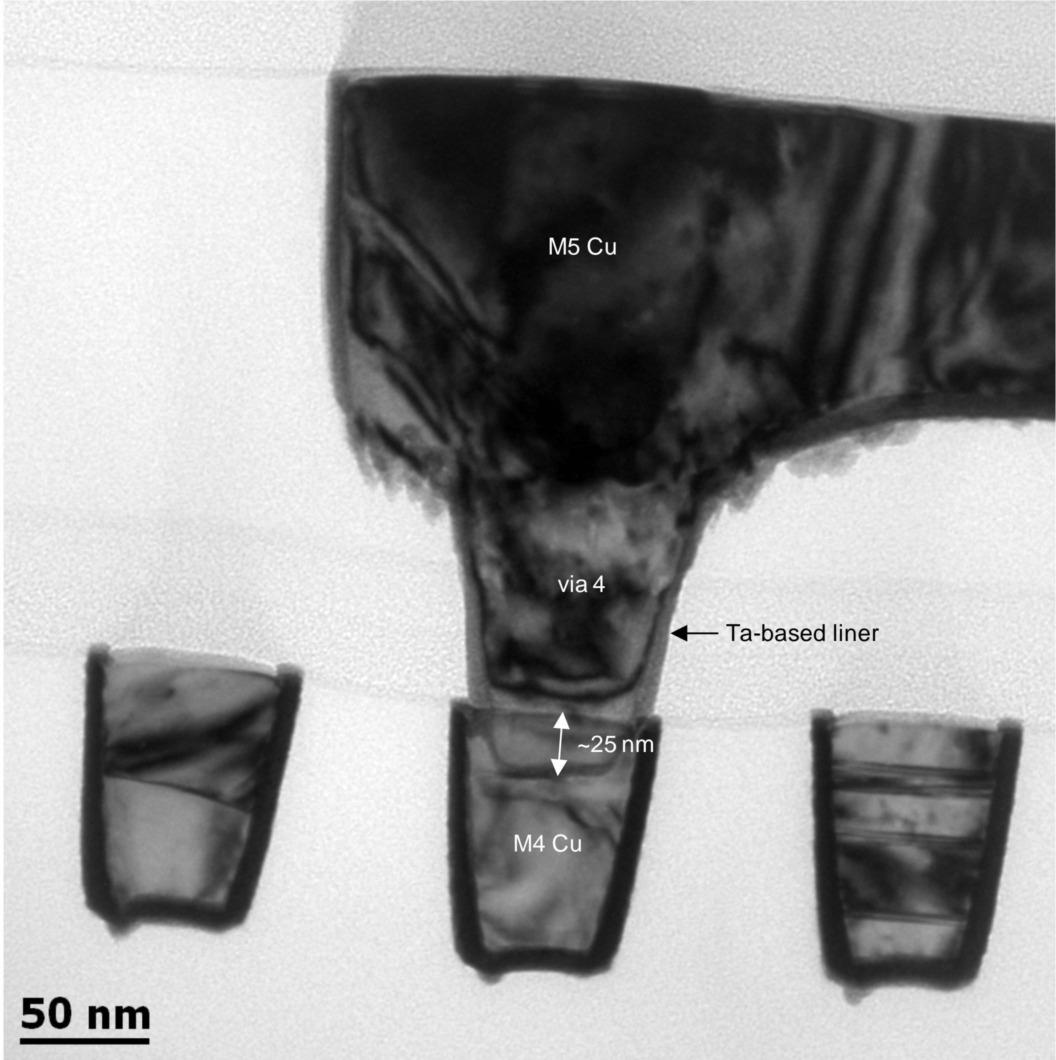

Figure 3.4.7 Via 4 – TEM

Figure 3.4.8 shows the 0.14 µm minimum pitch via 1s and 2s.

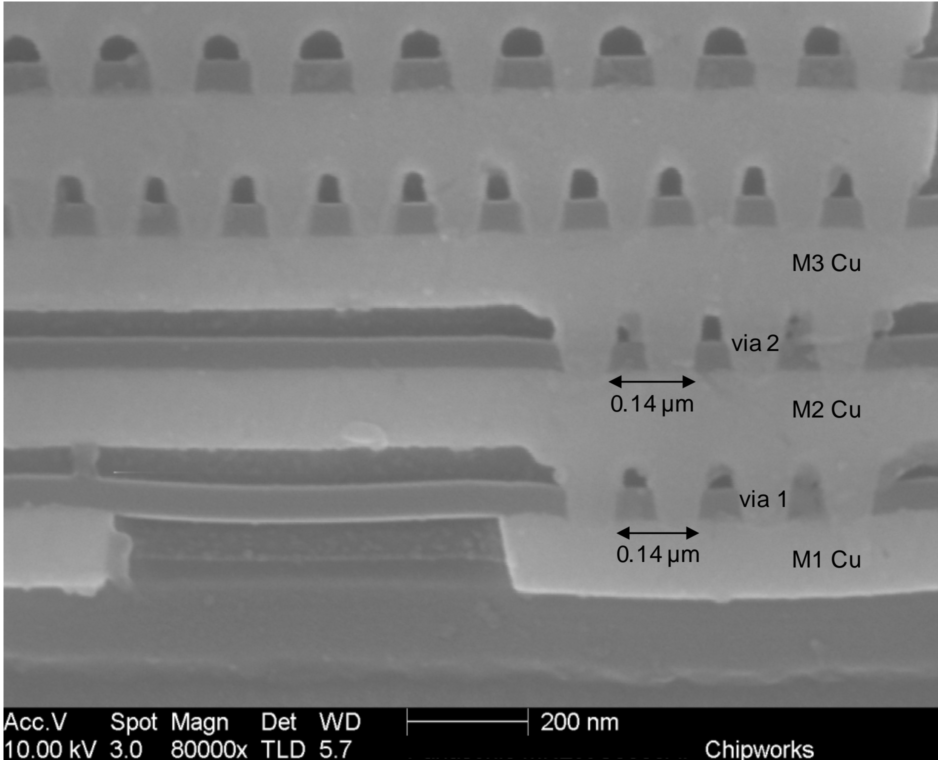

Figure 3.4.8 Minimum Pitch Via 1s and 2s

Figure 3.4.9 shows a TEM image of a pair of via 2s. The via 2 etch has penetrated about 25 nm into the surface of metal 2.

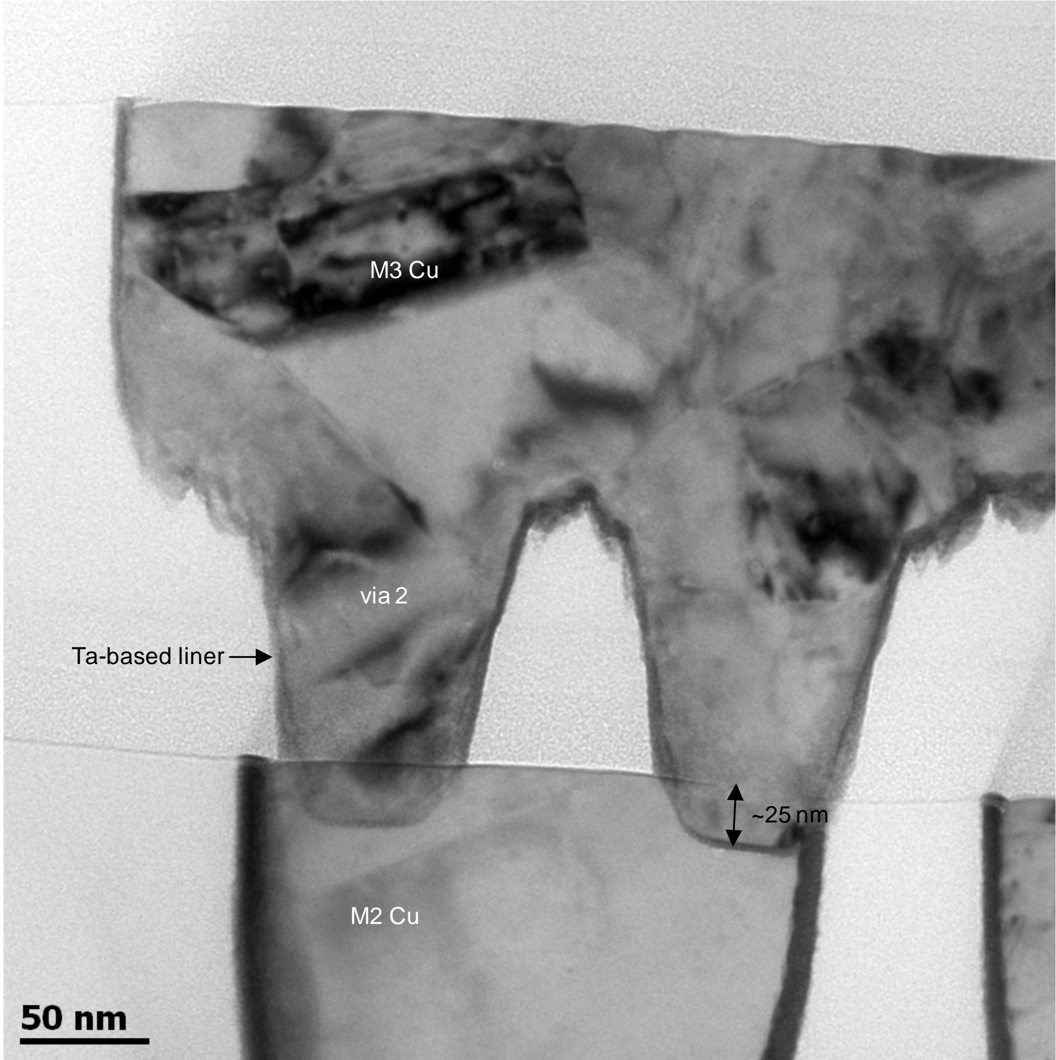

Figure 3.4.9 Via 2s – TEM

Figure 3.4.10 shows the 0.07 µm wide, 0.14 µm minimum pitch contacts. NiSi is used on the source drain diffusions.

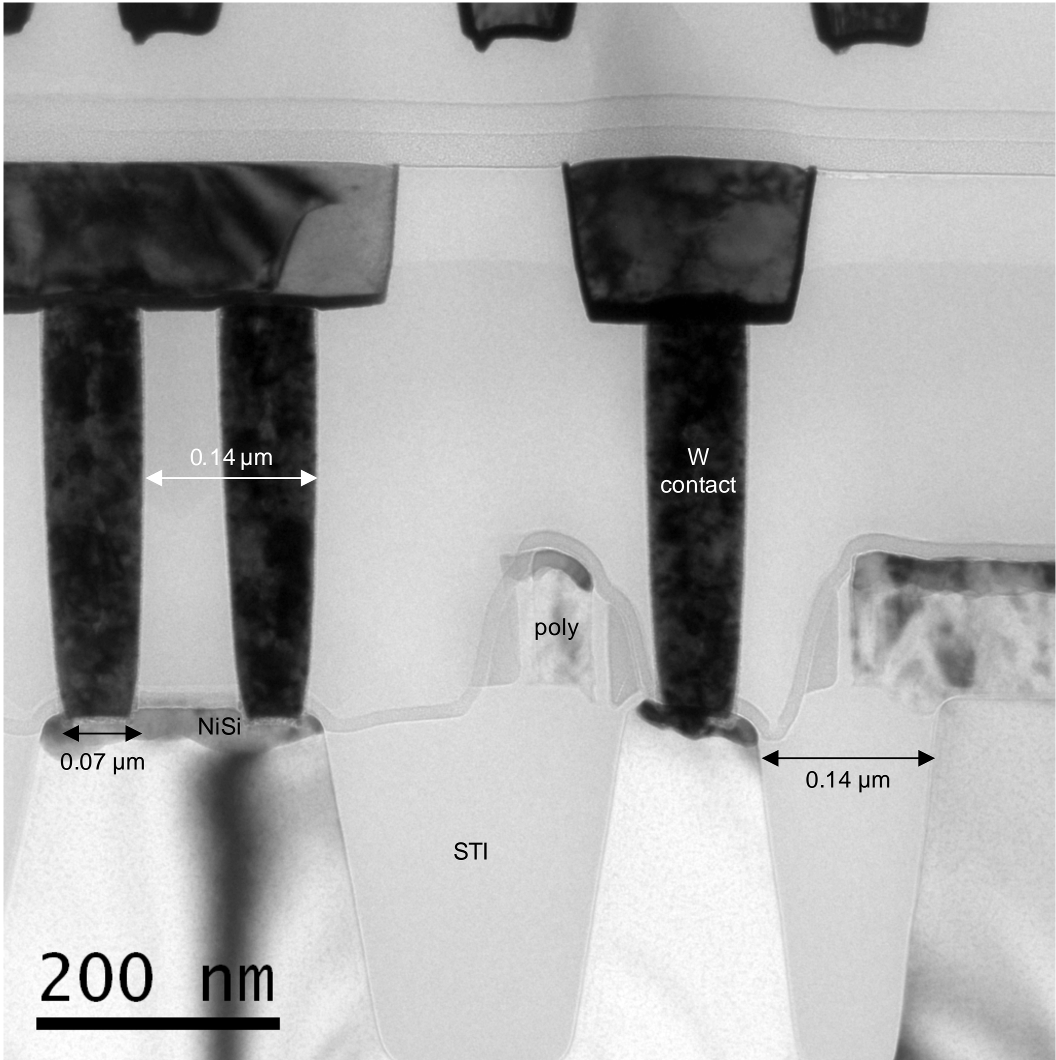

Figure 3.4.10 Minimum Pitch Contacts – TEM

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Figure 3.4.11 shows a 0.07 µm wide contact to poly. The contact etch has just penetrated the NiSi on top of the polysilicon.

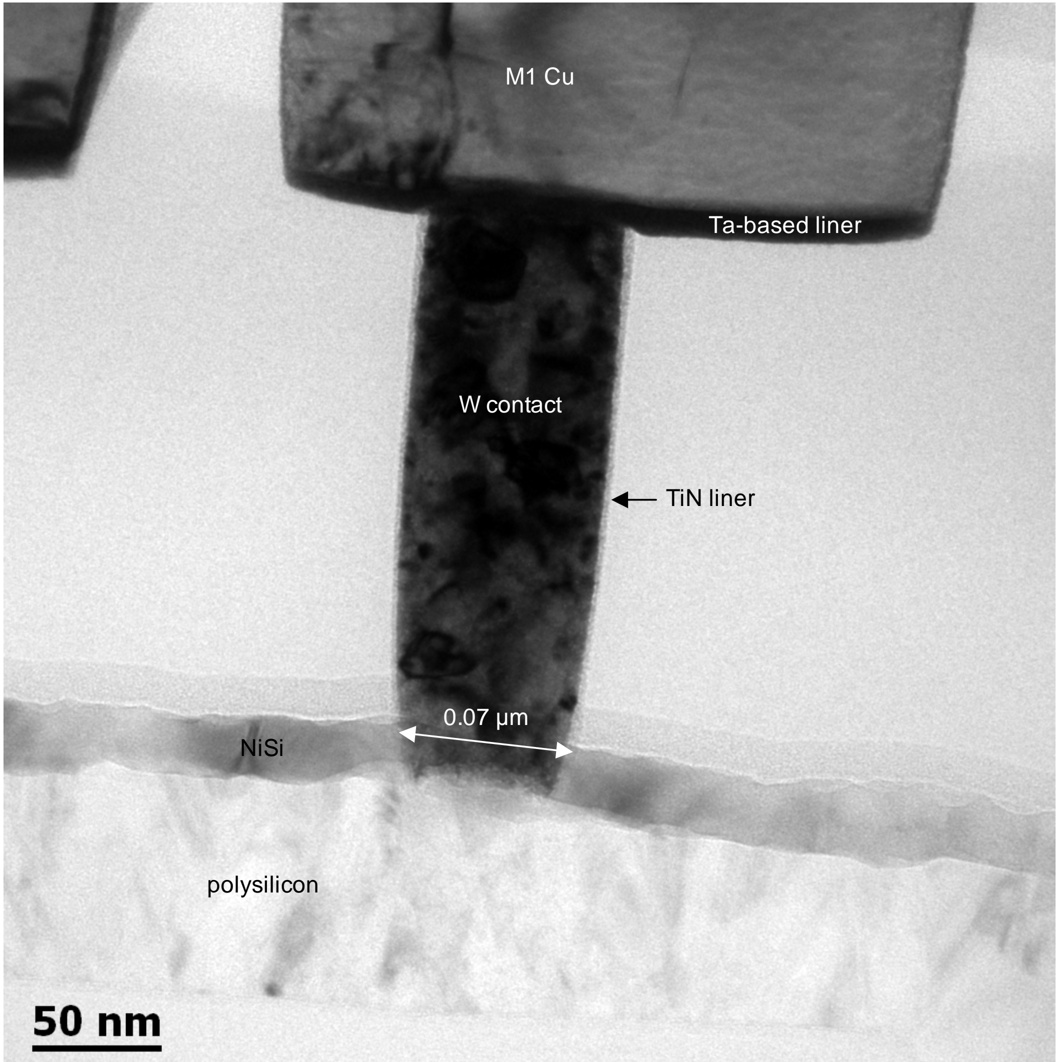

Figure 3.4.11 Contact to Poly – TEM

Figure 3.4.12 shows the top of a W contact. The TiN liner is about 4 nm thick at the top of the contact. The contacts were subjected to CMP, and sealed with the 27 nm thick oxide PMD 4 and SiOC PMD 5 prior to the metal 1 trench etch.

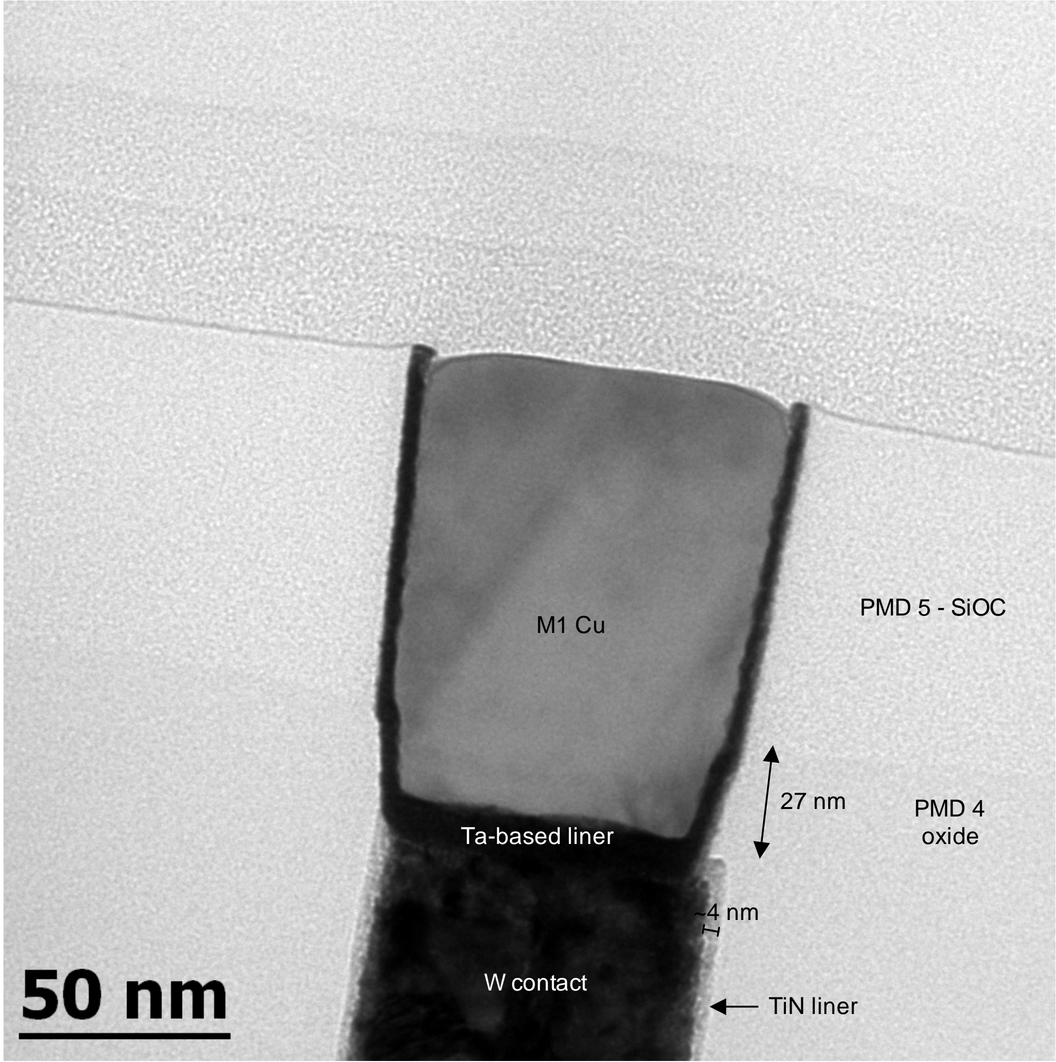

Figure 3.4.12 Top of Contact – TEM

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Figure 3.4.13 shows the bottom of a W stud, contacting the approximately 12 nm thick NiSi. The contact etch has just penetrated into the NiSi. The TiN liner is about 8 nm thick on the contact bottom.

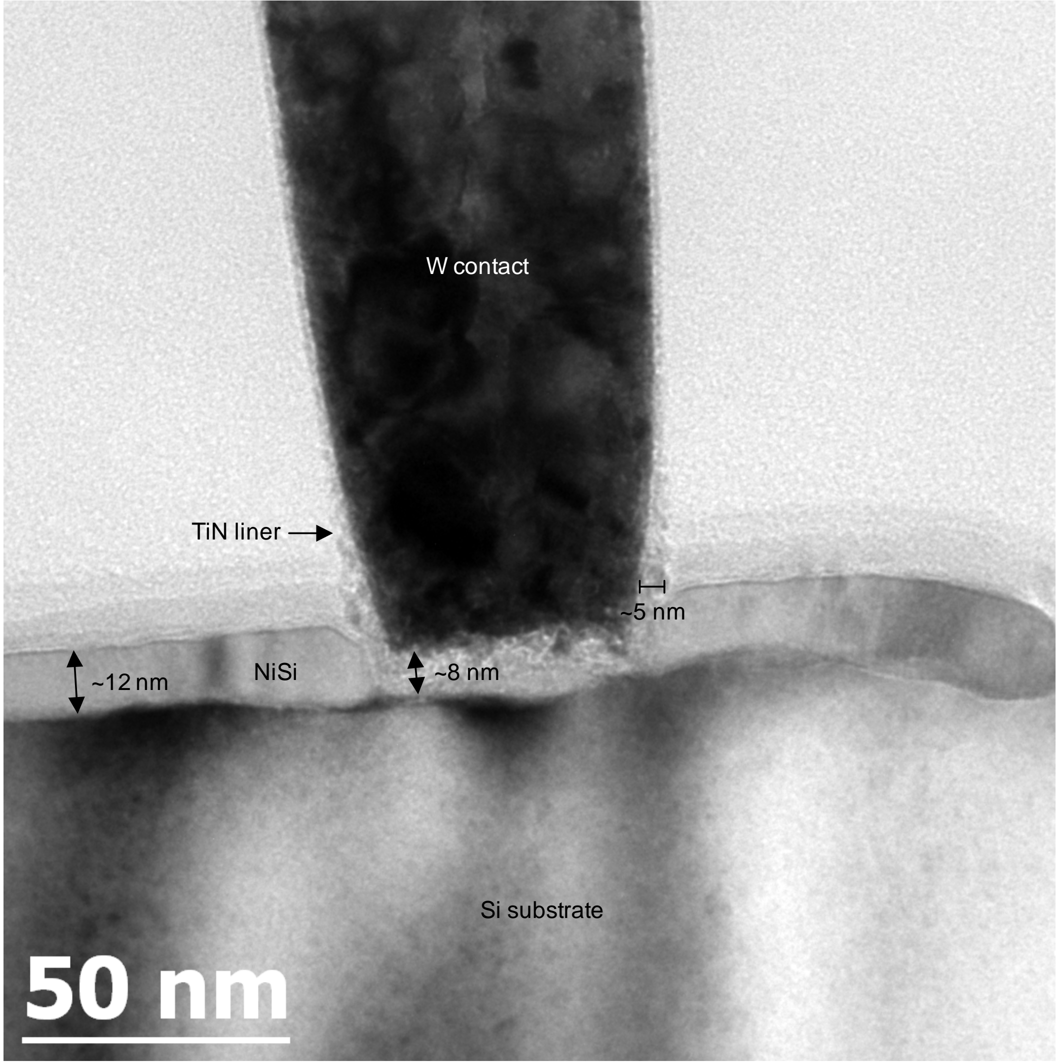

Figure 3.4.13 Bottom of Contact – TEM

Figure 3.4.14 shows the TEM-EDS spectrum of the Ti-based contact liner, likely TiN.

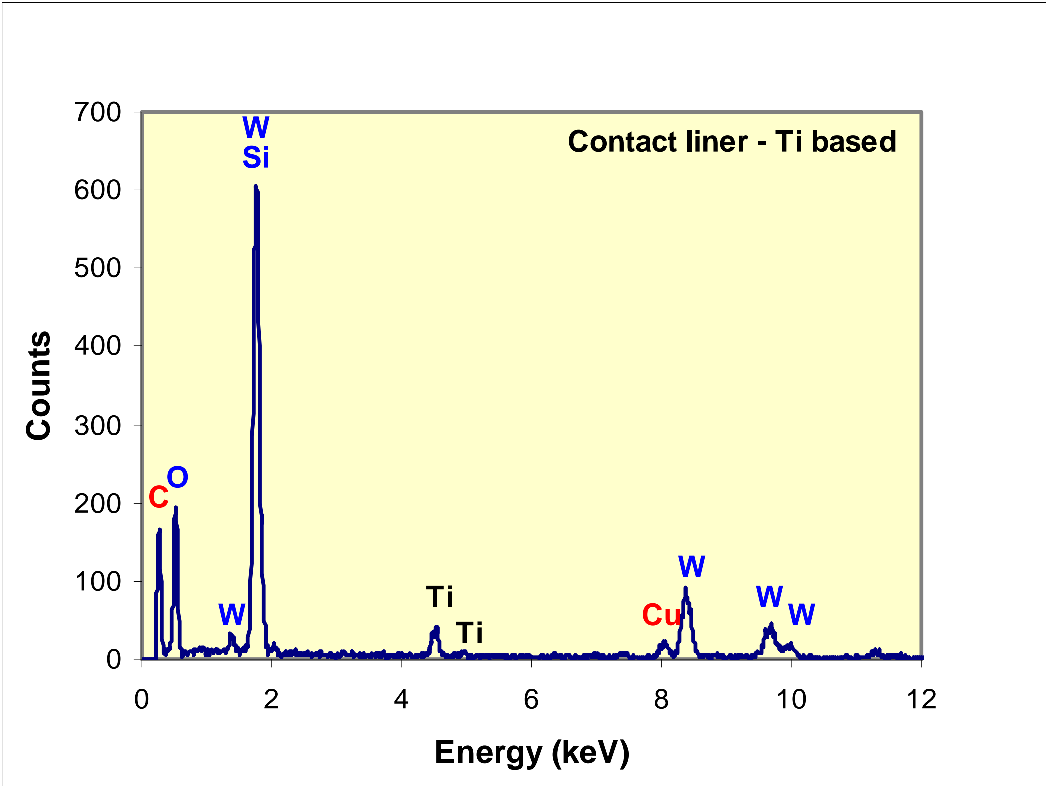

Figure 3.4.14 TEM-EDS Spectrum of Contact Liner

Figure 3.4.15 shows the TEM-EDS spectrum of the NiSi used on the diffusions.

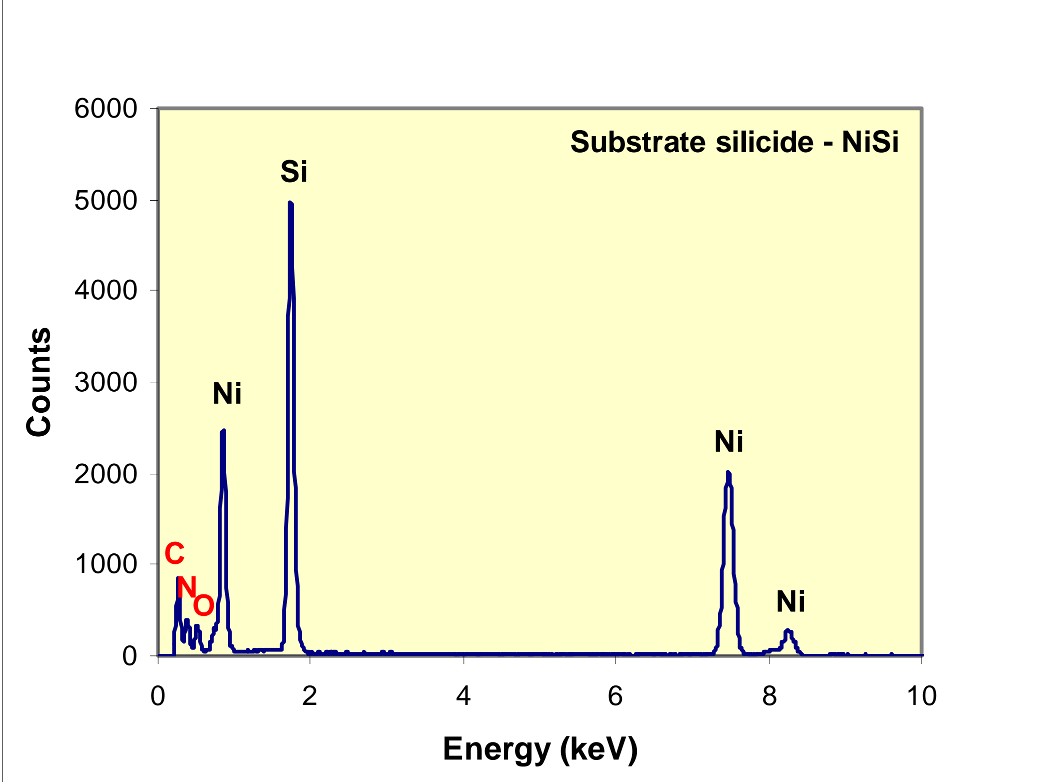

Figure 3.4.15 TEM-EDS Spectrum of Contact Silicide

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3.5 Logic MOS Transistors

The XXXX features 36 nm typical gate length MOS transistors, fabricated using a single level of Ni silicided polysilicon. The minimum gate length observed was 32 nm. These transistors, fabricated using a 45 nm process, appear to have the identical structure to XXXX's 65 nm transistors. A simple buffer oxide and silicon nitride sidewall spacer (SWS) continues to be used, along with Ni silicided poly gates. The 65 nm part did use Pt-doped Ni but, XXXX has used conventional Ni silicide with no Pt doping for this device. The 65 nm part also used a conventional gate oxide, while this 45 nm part uses a nitrided gate dielectric.

Like XXXX's 65 nm part, we do not see any evidence of strain engineering or memorized stress techniques employed on this 45 nm part. This 45 nm part is, however, manufactured using rotated wafers to improve the PMOS channel mobility.

The dimensions of the minimum observed features are summarized in Table 3.5.1 and Table 3.5.2.

Feature	Size (nm)
Contacted gate pitch	180
MOS minimum physical gate length	32
MOS gate to contact space	~30
Transistor sidewall spacer width	38
NiSi to gate edge space	22 - 33

Table 3.5.1 MOS Transistor Horizontal Dimensions

Feature	Size (nm)
MOS gate electrode thickness (NiSi/polysilicon)	108 (~16/92)
Gate dielectric thickness (oxide/nitride/oxide)	2.0
N^+ S/D depth	~0.06 µm (estimate)
P^+ S/D depth	~0.06 µm (estimate)

Table 3.5.2 MOS Transistor Vertical Dimensions

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Figure 3.5.1 shows a SEM image of a cross section through a series of logic MOS transistors. The contacted gate pitch is 0.18 µm.

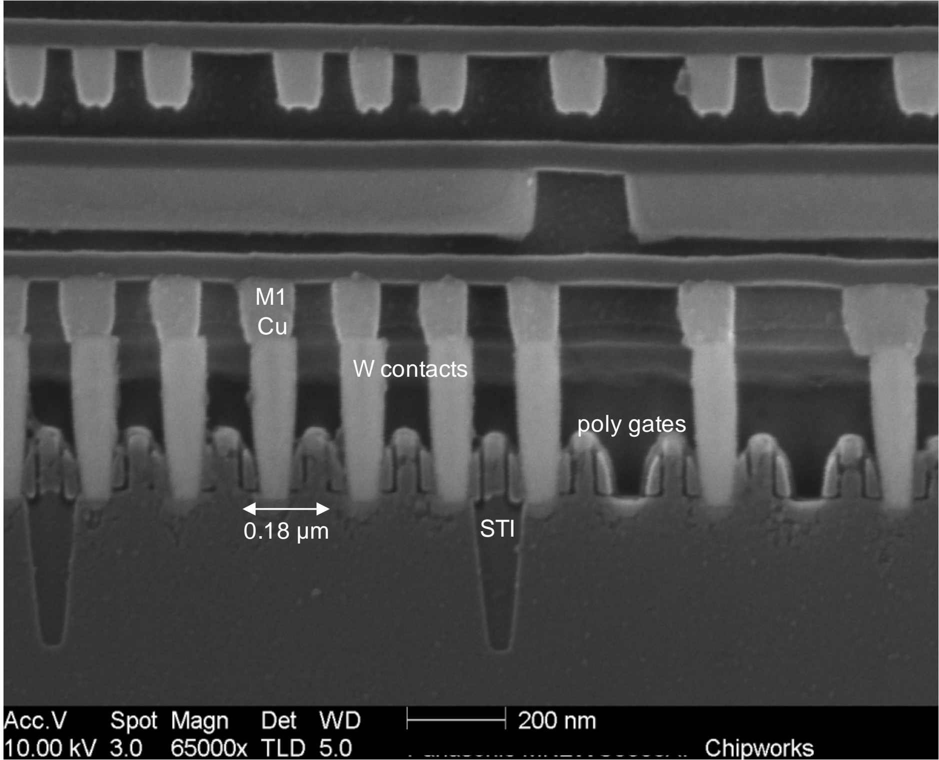

Figure 3.5.1 Minimum Contacted Gate Pitch

Figure 3.5.2 shows a SEM image of a series of NMOS transistors with a Si etch applied to delineate the approximately 0.06 µm deep N^+ S/D diffusions.

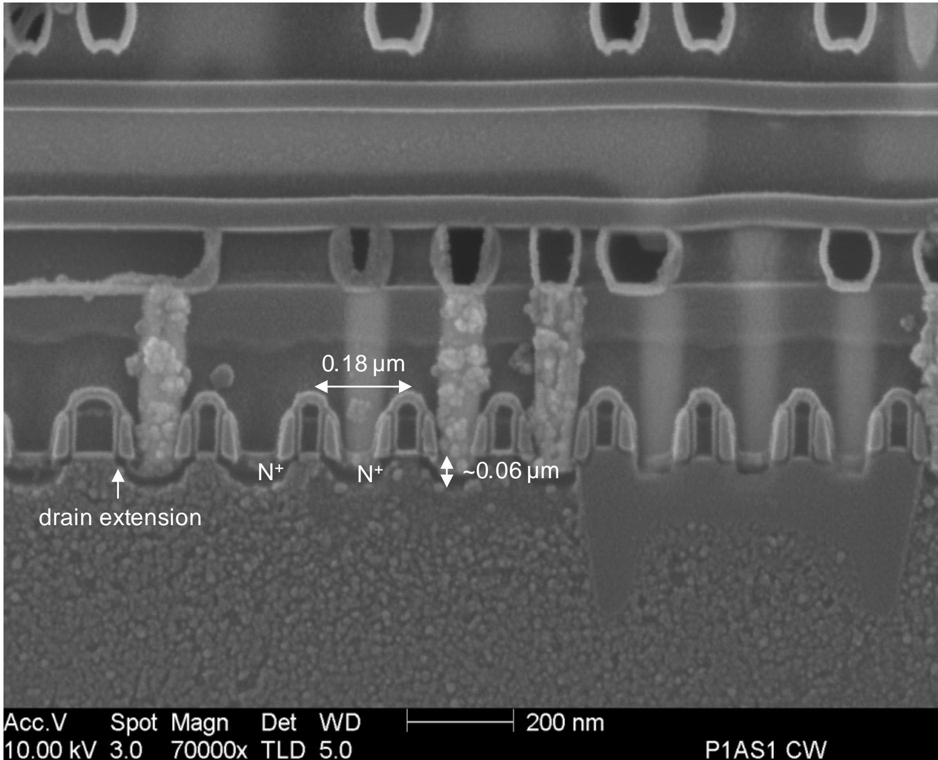

Figure 3.5.2 NMOS Transistors – Si Etch

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Figure 3.5.3 shows a SEM image of a series of PMOS transistors, with a Si etch applied. The delineation etch has over-etched the P^+ S/D diffusions. They are estimated to be about 0.06 µm deep.

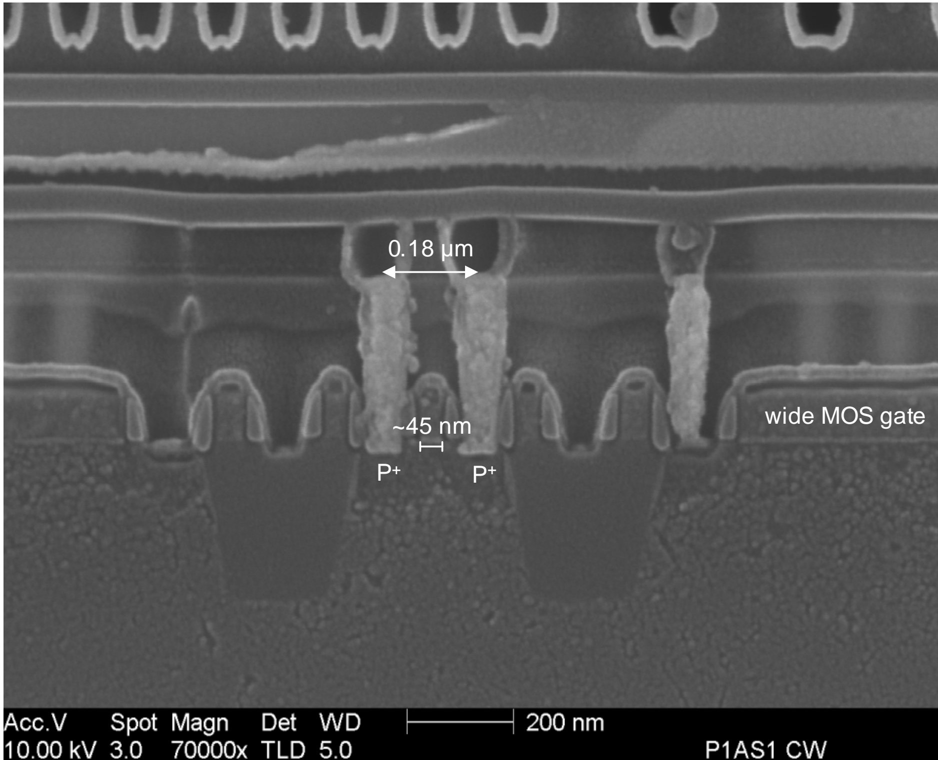

Figure 3.5.3 PMOS Transistors – Si Etch

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Figure 3.5.4 shows the 32 nm minimum gate length MOS transistor observed during this analysis.

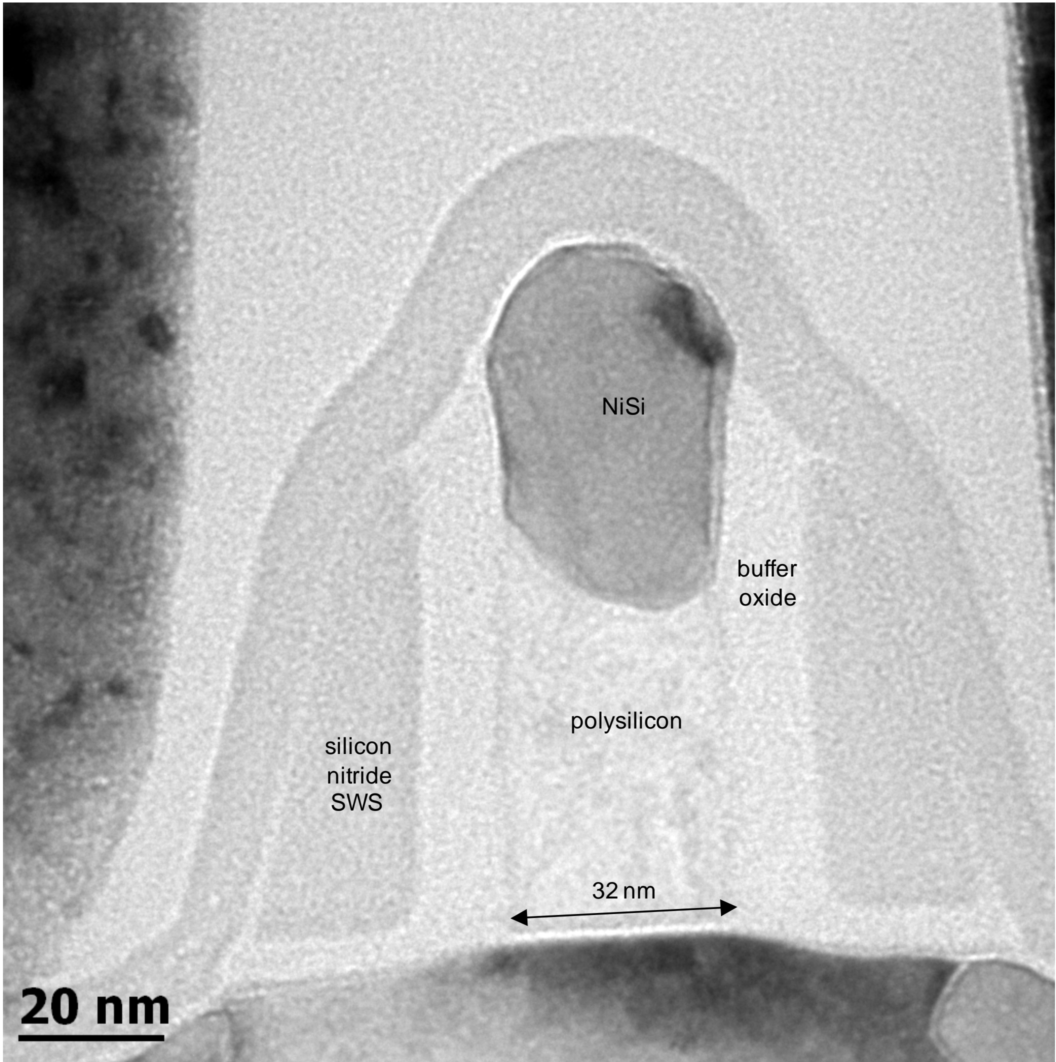

Figure 3.5.4 Minimum Gate Length MOS Transistor

Figure 3.5.5 shows a TEM image of a pair of MOS gates. The gates have a notched profile just above the gate dielectric. This gate profile is reminiscent of some of XXXX's notched gate transistors seen around the 0.18 μm node. The gate to contact spacing is variable, with a minimum spacing of about 30 nm. The Ni silicide to gate edge spacing also varies from about 22 nm to 33 nm. No discernable difference between the NMOS and PMOS gate structures was noted during the TEM analysis.

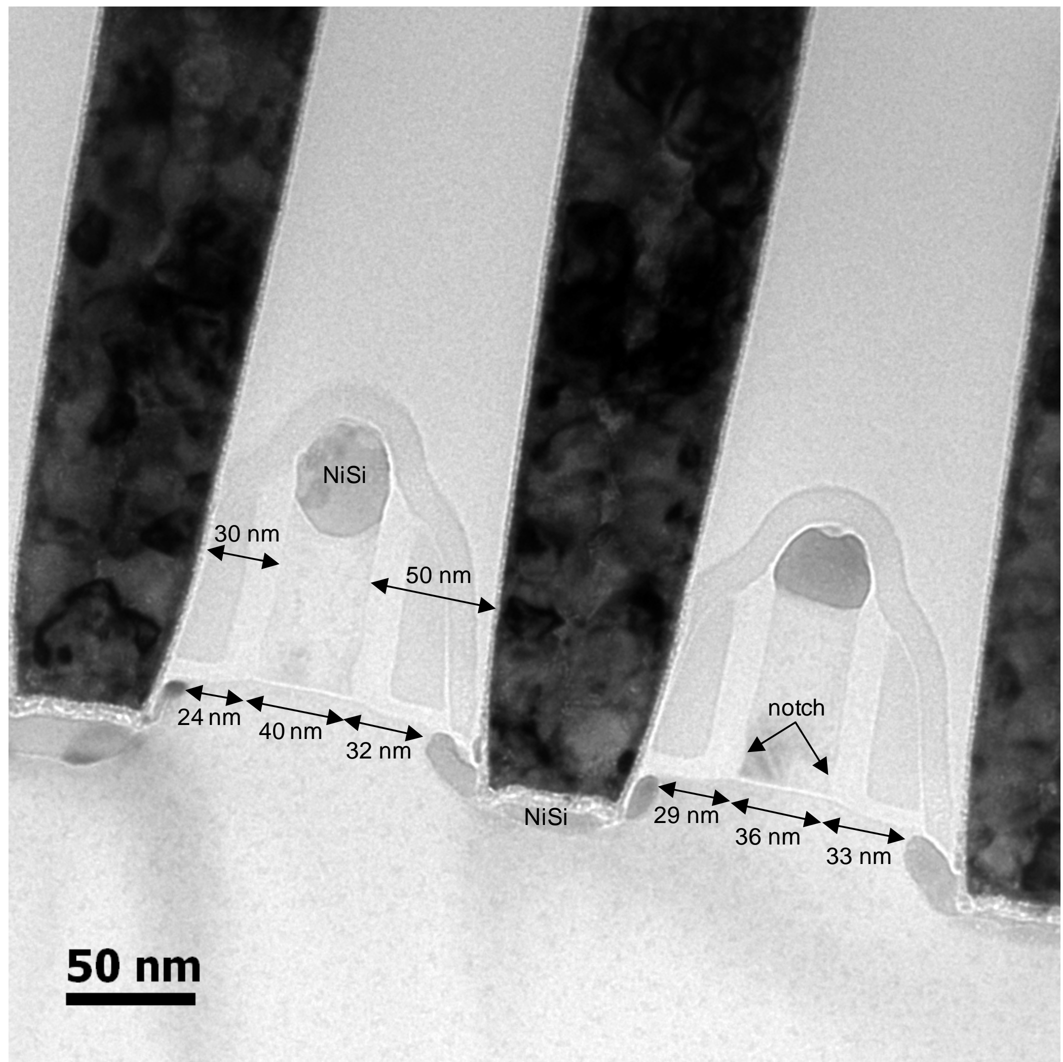

Figure 3.5.5 Minimum Gate Length MOS Transistor – TEM

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Figure 3.5.6 shows the 2.0 nm thick oxide/nitride/oxide (ONO) logic gate dielectric.

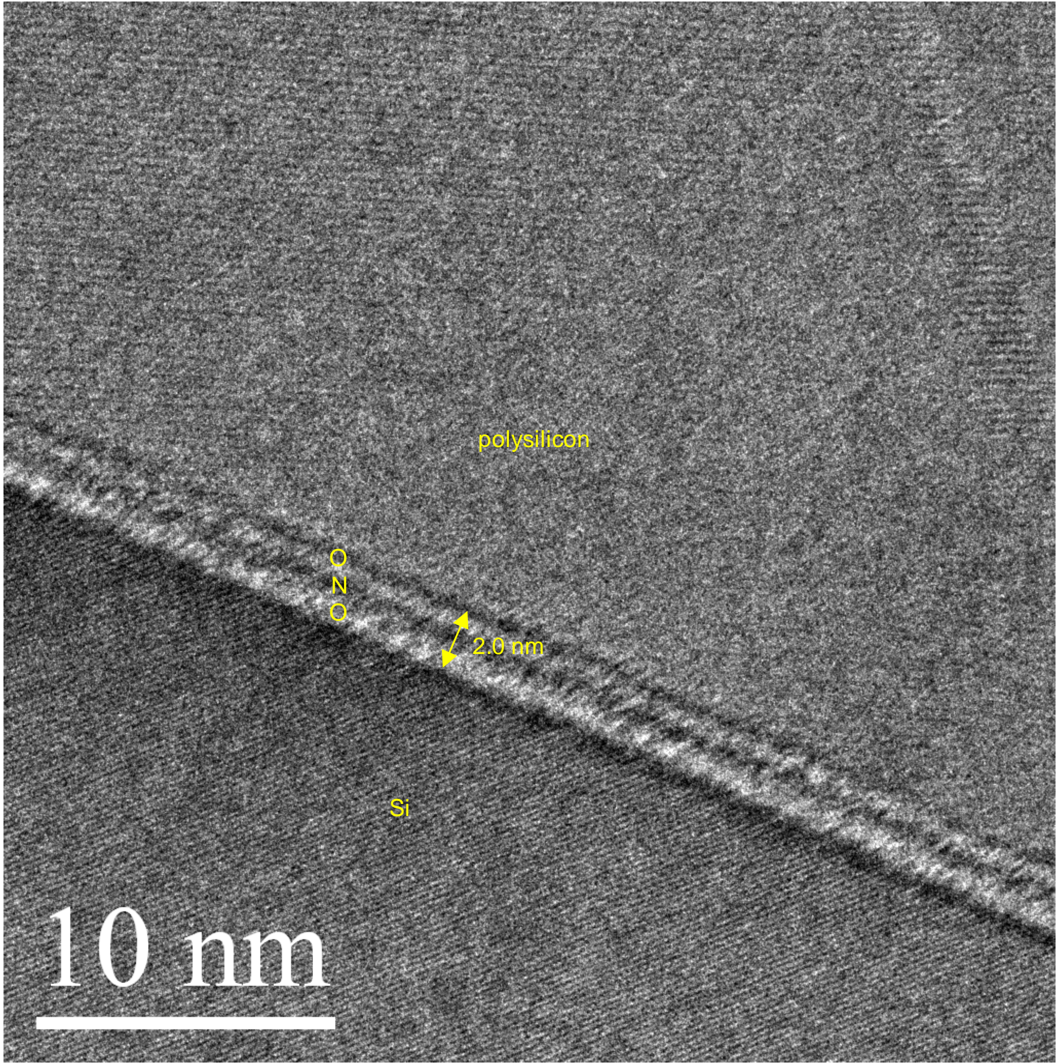

Figure 3.5.6 Gate Dielectric – TEM

Figure 3.5.7 shows a pair of narrow and wide gates. As mentioned, the ~12 nm thick SiON appears to be too thin to be used for applying tensile strain. However, stress memorization techniques may be used to boost the NMOS transistor drive current. Here, stress is transferred from a disposable dielectric layer to the silicon substrate. This strain is retained by the transistors after the disposable dielectric layer is removed.

The bottom of the S/D contact is about 30 nm below the Si surface.

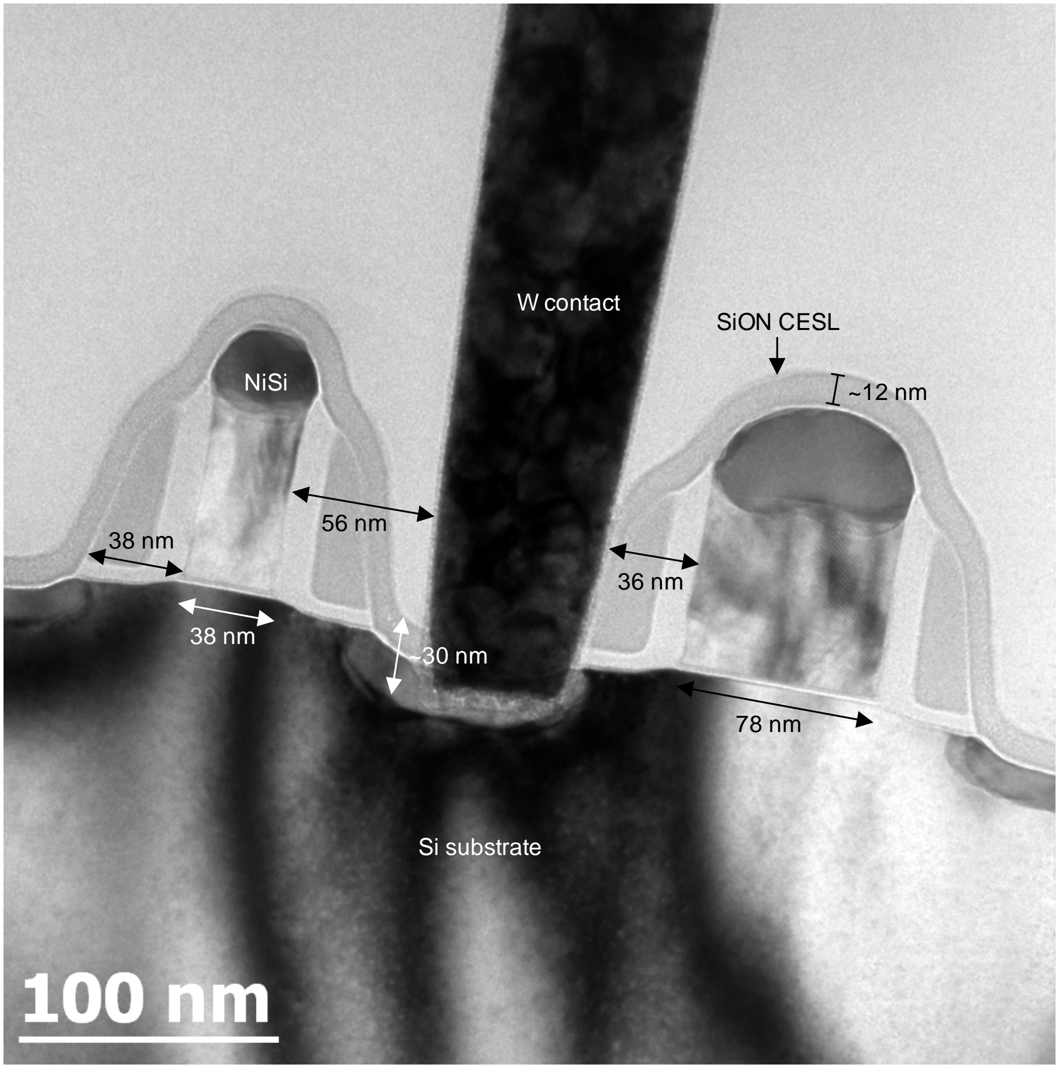

Figure 3.5.7 Wide and Narrow Gate Length Transistors – TEM

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Figure 3.5.8 shows a detailed TEM view of the bottom of a transistor. The buffer oxide is 13 nm thick along the gate sidewall and 7 nm thick beneath the nitride SWS. The Ni silicide on the S/D diffusion is spaced 22 nm from the gate edge.

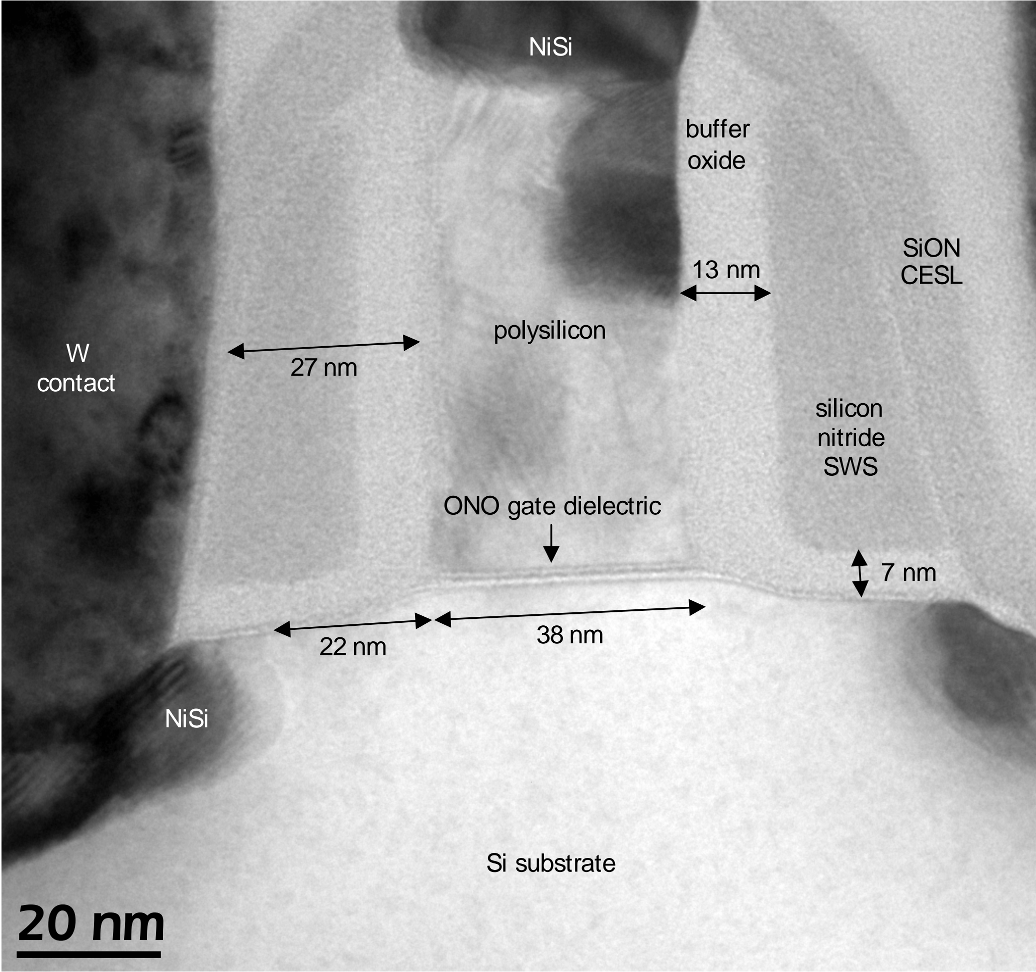

Figure 3.5.8 Gate Dielectric Overview – TEM

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Figure 3.5.9 shows the edge of a gate in the gate width direction. The 108 nm gate thickness includes a 16 nm thick layer of NiSi.

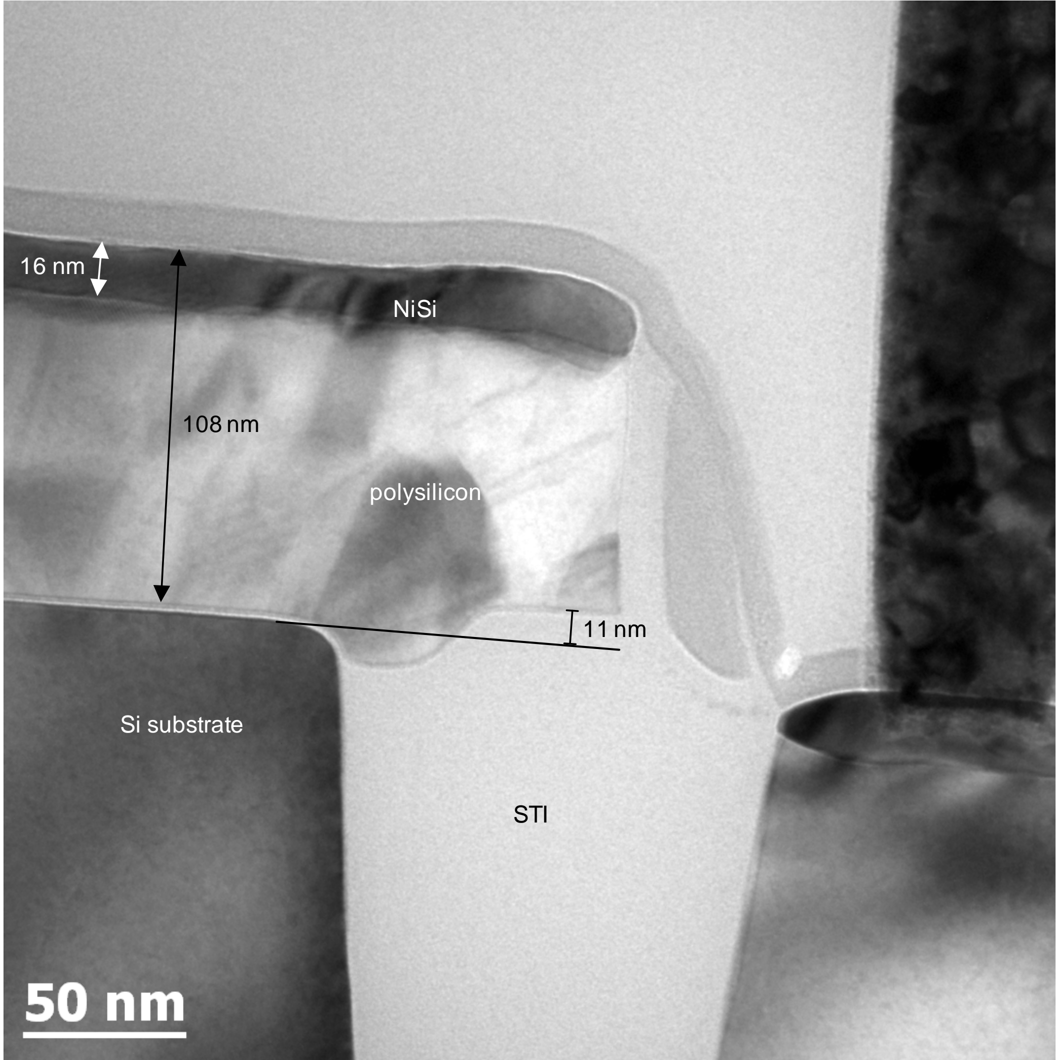

Figure 3.5.9 Poly Thickness – TEM

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Figure 3.5.10 shows a detailed view of the transistor gate wrap. The Si corner has been rounded to provide smoother transition of the gate dielectric to STI. The radius of the Si corner is about 13 nm.

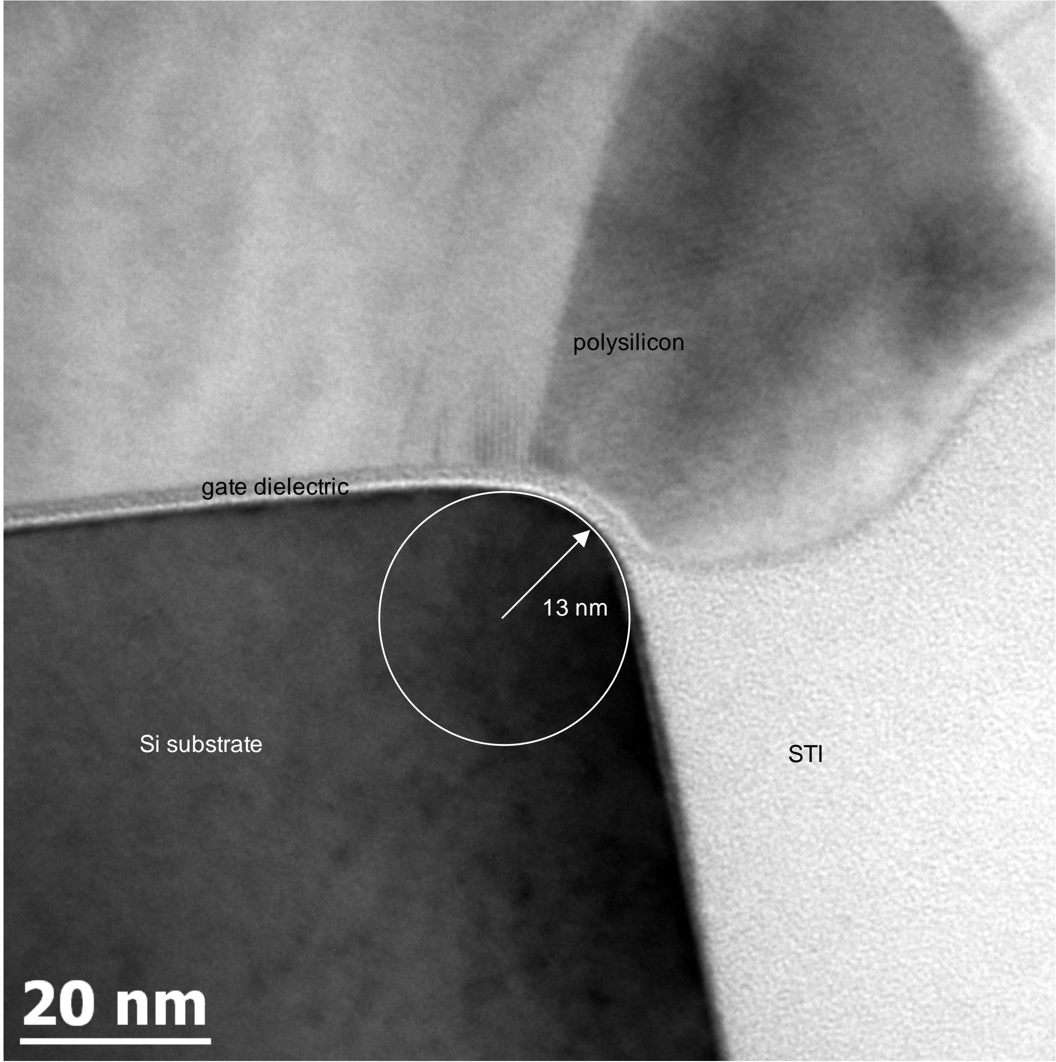

Figure 3.5.10 Poly Gate Wrap – TEM