STEEP SUBTHRESHOLD CHARACTERISTIC AND ENHANCED TRANSCONDUCTANCE OF FULLY-RECESSED OXIDE (TRENCH) ISOLATED 1/4 μm WIDTH MOSFETS

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ABSTRACT

This paper describes the dependence of MOSFET gate-controllability on the field isolation scheme. It is found that a fully-recessed oxide (trench) isolated MOSFET has a sharp cutoff characteristic and high transconductance in comparison with a non-recessed one. These features of the fully-recessed oxide MOSFET are due to the crowding of the gate's fringing field at the channel edge. It is also found that the gate and diffused line capacitances for the fully-recessed oxide isolation are small so that high switching speed operation can be expected.

INTRODUCTION

Reduction of the field isolation area is a major concern in achieving a high performance and high packing density VLSI. Several bird's-beak free isolation methods have been proposed, e.g., BOX [1],[2] and SWAMI [3]. However, lower submicron device characteristics in relation to the field isolation scheme have been seldomly reported.

In previous works [1]-[10], attention has been paid mainly to the threshold voltage dependence on the field isolation scheme. It was found that the MOSFET threshold voltage and subthreshold characteristic strongly depended on the field isolation scheme. In a non-recessed oxide MOSFET shown in Fig. 1 (a), the threshold voltage becomes higher with decreasing channel width, the so-called narrow-channel effect [4],[5]. This results from the extra bulk charge stored under a thick oxide region. In a fully-recessed oxide MOSFET shown in Fig. 1 (b), however, the threshold voltage becomes lower for the narrower width case, which is referred to as the inverse narrow-channel effect [6]-[9]. This phenomenon is explained by the crowding of the gate's fringing field at the channel edge due to its convex shape, as shown in Fig. 1 (b). It was also reported that an anomalous subthreshold current hump can be observed for a fully-recessed oxide MOSFET due to the parasitic edge MOSFET [1],[3],[10]. However, there has been no publication concerning the dependence of gate-controllability on the field oxide scheme.

The purpose of this paper is to investigate which field isolation scheme is advisable for 1/4 μm feature size VLSIs from the viewpoint of device performance, such as the subthreshold swing S and the transconductance gm, using a three-dimensional device simulator TOPMOST [6],[7],[10],[11].

EXPERIMENTAL RESULTS

A series of trench and LOCOS isolated MOSFETs have been fabricated.

Figure 2 shows the experimental results of the subthreshold swing S which is defined by $dV_G/d(\log I_D)$. The effective channel length L_{eff} is 10 μm and drain voltage V_D is 0.05 V to eliminate the short-channel effect. For LOCOS isolation, the subthreshold swing is almost constant for channel widths down to the submicron region. On the other hand, the subthreshold swing of the fully-recessed oxide (trench) MOSFET is decreased with a reduction of the channel width, i.e., the fully recessed oxide MOSFET has a steep subthreshold characteristic.

THREE-DIMENSIONAL ANALYSIS

Two typical isolation schemes shown in Fig. 1 are used to analyze the field isolation scheme dependent MOSFET characteristics.

Subthreshold Swing S

Figure 3 shows the three-dimensionally simulated subthreshold swing dependence on the channel width. Simulations are carried out for the effective channel length L_{eff} = 2um and drain voltage V_D = 0.05 V to eliminate the short-channel effect. It is exhibited that the fully-recessed oxide MOSFET has a small subthreshold swing, i.e., a sharp cutoff characteristic. This is due to the large depletion layer at the channel edge, as schematically illustrated in Fig. 1 (b), which results from the gate's fringing field. A small depletion capacitance C_d results in a small subthreshold swing S, since the subthreshold swing S is approximately proportional to $1+C_d/C_{ox}$ [12], as shown in Fig. 4 (a).

Figure 5 shows the dependence of the subthreshold swing S on the gate oxide thickness t_{ox}. This figure suggests that, for a 0.25 μm channel width, a 12 nm gate oxide fully-recessed MOSFET is equivalent to a 6 nm gate oxide non-recessed one in regard to the subthreshold swing. It should be noted that the subthreshold swing S linearly depends on the gate oxide thickness t_{ox} in accordance with the equation shown in the inset of Fig. 5.

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A short-channel MOSFET with L_{eff} = 0.3 µm is examined, as shown in Fig. 6. Even for the short-channel case, the subthreshold swing of the fully-recessed MOSFET is smaller than that of the non-recessed one. The slope of the S-t_{ox} characteristic becomes steeper mainly due to an increase in substrate concentration, i.e., an increase of C_d. No significant short-channel effect is observed for the fully-recessed oxide MOSFET, because the influence of the drain to the channel is weakened by its high gate-controllability.

Transconductance gm

Figure 7 shows the gm-V_G characteristics, which are simulated using the field dependent mobility model [13]. The gm peak value of the fully-recessed oxide MOSFET is higher than that of the non-recessed one. The reason for a high gm peak is the small C_d of the fully-recessed oxide MOSFET, which can be explained by an analytical model of gm as shown in Fig. 4 (b). A hump of gm for t_{ox} over 20nm can be seen, which corresponds to the parasitic edge MOSFET [10].

Countermeasures for the Low Threshold Voltage V_{th}

A drawback of the fully-recessed oxide MOSFET is its low threshold voltage, which may cause a leakage drain current at V_G = 0 V. However, the leakage current is not as large as that inferred from the inverse narrow-channel effect, because of its steep subthreshold characteristic. In addition, the threshold voltage can be improved by sidewall implantation [1], [10], tapering the sidewall [7] and rounding the corner edge. However, these approaches cause high C_d so that the gate-controllability is reduced. An appropriate choice of the gate material, e.g., tungsten, is most favorable, since its midgap work function results in a desired threshold voltage without the need for channel implant into n- and p-channel devices [14] without losing its high gate-controllability. It should be noted that the origin for the lower threshold voltage of an n-channel MOSFET is the use of an n^+ poly-Si gate.

Circuit Operation Speed

The gate capacitance C_G of the fully-recessed oxide MOSFET is about 20 % smaller than that of the non-recessed one due to the smaller C_d. Furthermore, as shown in Fig. 8, the diffused line capacitance $C_{diffused\ line}$ of the fully-recessed oxide isolation is also 20 % smaller than that of the non-recessed one, which agrees with the experiments [2]. These small C_G and $C_{diffused\ line}$ with a high transconductance gm result in 40 % higher circuit operation compared with the non-recessed case, when the operation speed is simply estimated by gm^{-1} $(C_G + C_{diffused\ line})$.

CONCLUSION

The dependence of gate-controllability on the field isolation scheme has been analyzed. Advantages of the fully-recessed oxide isolation are summarized in Fig. 9. Small depletion capacitance C_d, due to the gate's fringing field, results in small S, high gm and small C_G. Because of its structure, $C_{diffused\ line}$ is also small. These lead to excellent gate-controllability and high speed circuit operation. These features push a fully-recessed oxide isolation to the main stream for lower submicron VLSIs.

A drawback of the fully-recessed oxide MOSFET is its low threshold voltage. However, the origin for the lower threshold voltage of an n-channel MOSFET is the use of an n^+ poly-Si gate. Owing to the high gate-controllability, the threshold voltage strongly reflects the gate material. The use of an tungsten gate realizes the desired threshold voltage without the need for channel implant into n- and p-channel devices while preserving the high gate-controllability. The adoption of the fully-recessed oxide (trench) isolation with tungsten gate CMOS is one of the most promising device features for the 1/4 µm VLSI era.

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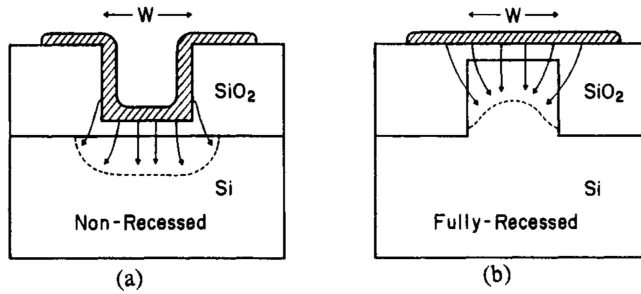


Fig. 1 (a) Non- and (b) fully-recessed oxide MOSFETs. The depletion capacitance C_d of the fully-recessed oxide MOSFET is small due to the gate's fringing field.

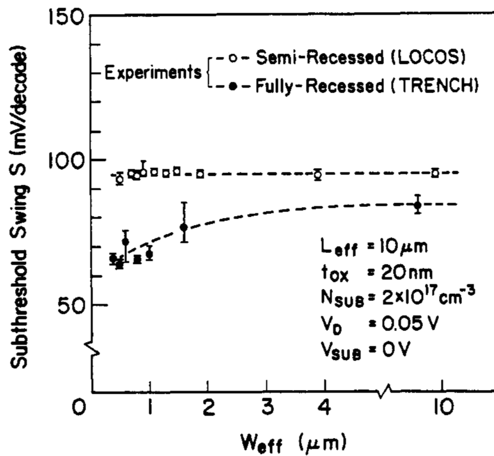


Fig. 2 Experimental results of subthreshold swing for trench and LOCOS isolations. The trench isolated MOSFET has a small subthreshold swing, i.e., a steep subthreshold characteristic.

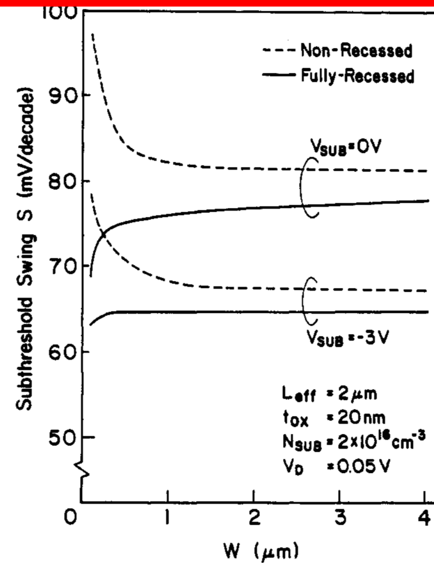
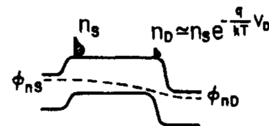


Fig. 3 Dependences of subthreshold swing on channel width and substrate bias.

Subthreshold Region



$$I_D = qD\frac{n_S - n_D}{L} \simeq qD\frac{n_S}{L}$$

$$S = \left[\frac{\partial(\log I_D)}{\partial V_G}\right]^{-1}$$

$$\simeq \left[\frac{\partial(\log n_S)}{\partial V_G}\right]^{-1}$$

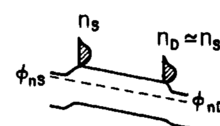
$$= \left[\frac{1}{\frac{kT}{q}\ln 10}\,\frac{\partial \psi_{SS}}{\partial V_G}\right]^{-1}$$

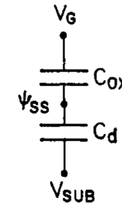
$$\simeq \frac{kT}{q}\ln 10\left(1 + \frac{C_d}{C_{ox}}\right)$$

where $n_S = n_i\, e^{\frac{q}{kT}(\psi_{SS} - \phi_{nS})}$

(a)

Linear Region





$$I_D = q\, n_S\, \mu \frac{V_D}{L}$$

$$g_m = \frac{\partial I_D}{\partial V_G}$$

$$\simeq q\frac{V_D}{L}\left[\frac{\partial n_S}{\partial V_G}\mu + n_S\frac{\partial \mu}{\partial V_G}\right]$$

$$= q\frac{V_D}{L} n_S\left[\mu\frac{q}{kT}\frac{\partial \psi_{SS}}{\partial V_G} + \frac{\partial \mu}{\partial V_G}\right]$$

where

$$n_S\frac{\partial \psi_{SS}}{\partial V_G} = \begin{cases} n_S \dfrac{1}{1 + \frac{C_d}{C_{ox}}} & \text{(depletion)} \\ \dfrac{kT}{q}\dfrac{C_{ox}}{q} & \text{(strong inversion)} \end{cases}$$

(b)

Fig. 4 Analytical model of (a) subthreshold swing and (b) transconductance. Both S and gm depend on C_d. Small C_d results in small S and high gm.

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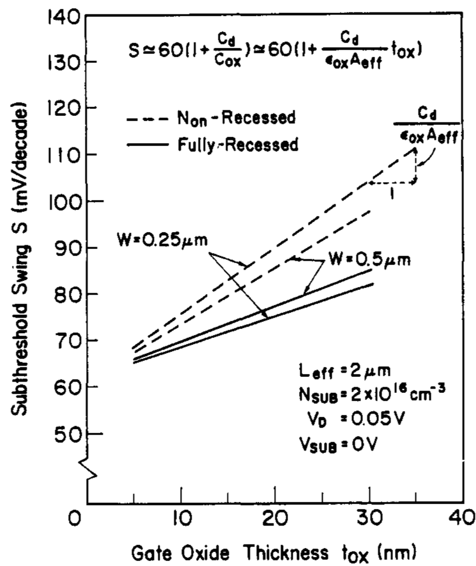

Fig. 5 Dependence of subthreshold swing on oxide thickness for L_{eff} = 2 μm.

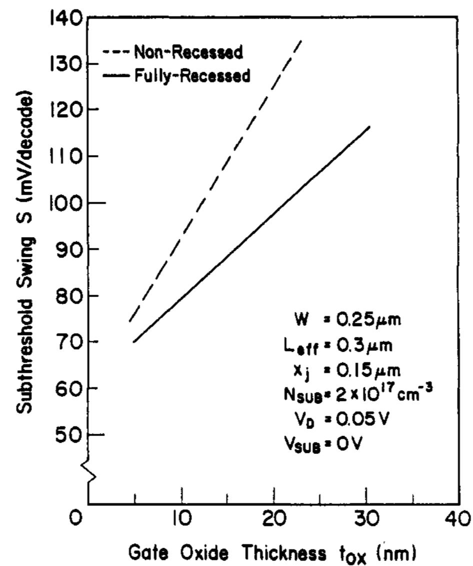

Fig. 6 Dependence of subthreshold swing on oxide thickness for L_{eff} = 0.3 μm.

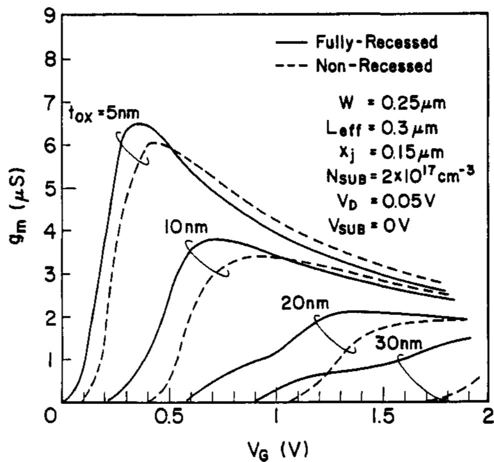

Fig. 7 Field isolation scheme dependent transconductance for L_{eff} = 0.3 μm. The gm peak value of the fully-recessed oxide MOSFET is higher than that of the non-recessed one.

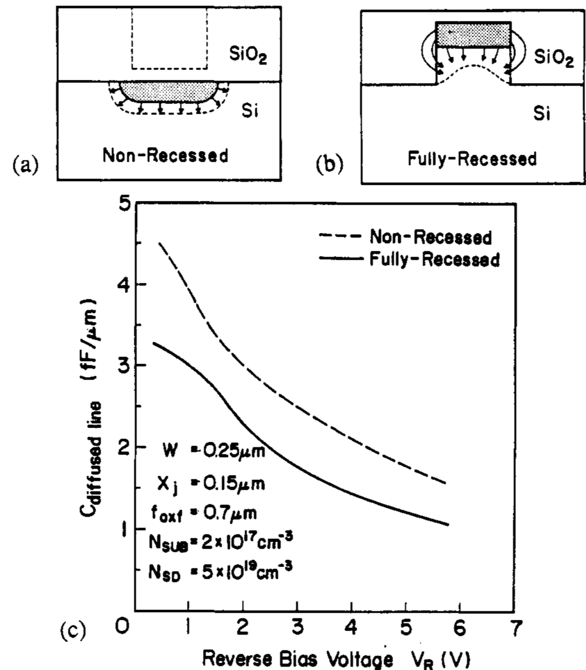

Fig. 8 (a) Non- and (b) fully-recessed oxide isolated diffused line and (c) its capacitances.

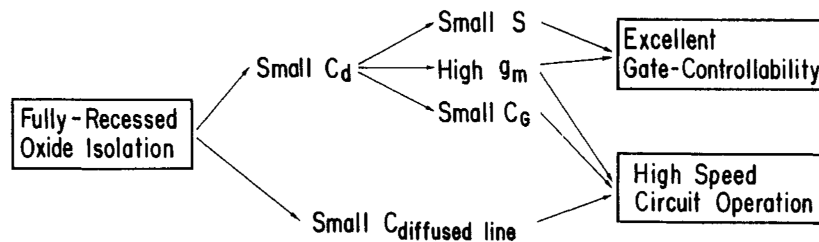

Fig. 9 Advantages of fully-recessed oxide isolation.

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