



US005314843A

United States Patent [19]

[11] Patent Number: **5,314,843**

Yu et al.

[45] Date of Patent: **May 24, 1994**

[54] **INTEGRATED CIRCUIT POLISHING METHOD**

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **858,670**

[22] Filed: **Mar. 27, 1992**

[51] Int. Cl.⁵ **H01L 21/302**

[52] U.S. Cl. **437/225; 437/974; 156/636**

[58] Field of Search **156/636; 51/281 R, 283 R; 437/225, 228, 974**

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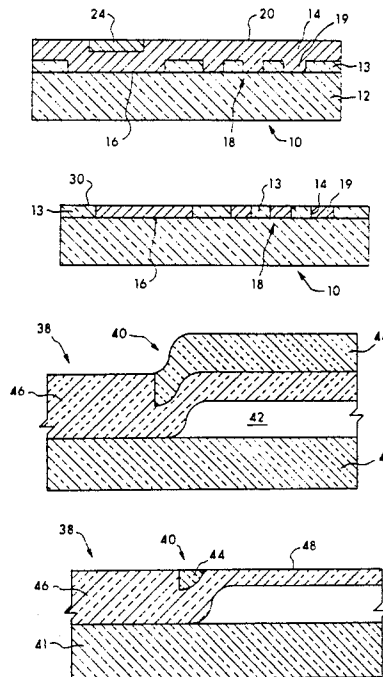
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[57] **ABSTRACT**

A semiconductor wafer has a surface layer to be planarized in a chemical mechanical polishing (CMP) process. An area of the layer that is higher than another area is altered so that the removal rate is higher. For example, if the surface layer is TEOS oxide, the higher layer may be bombarded with boron and phosphorus to produce BPSG, which has a polishing rate 2-3 times that of the TEOS. Upon CMP planarization, the higher area erodes faster resulting in improved planarization. Alternatively, the lower area may be doped with nitrogen to produce a nitride which is more resistant to CMP, with the same result. Likewise areas, such as tungsten troughs, which tend to be dished by CMP, may be changed to WN_x which is more resistant to the tungsten CMP than the adjacent tungsten, eliminating the dishing upon planarization.

23 Claims, 4 Drawing Sheets



IP Bridge Exhibit 2015
TSMC v. IP Bridge

Fig. 1
(Prior Art)

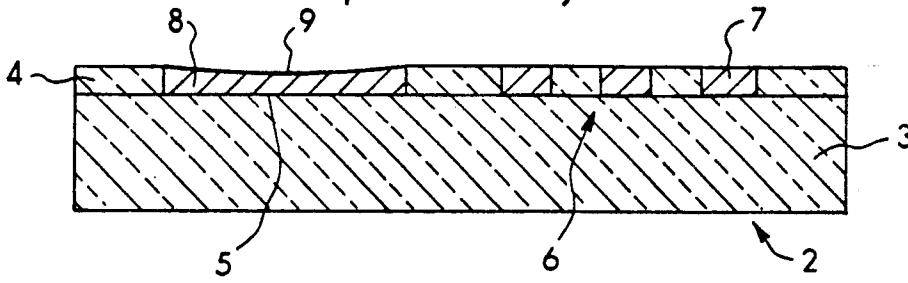


Fig. 2

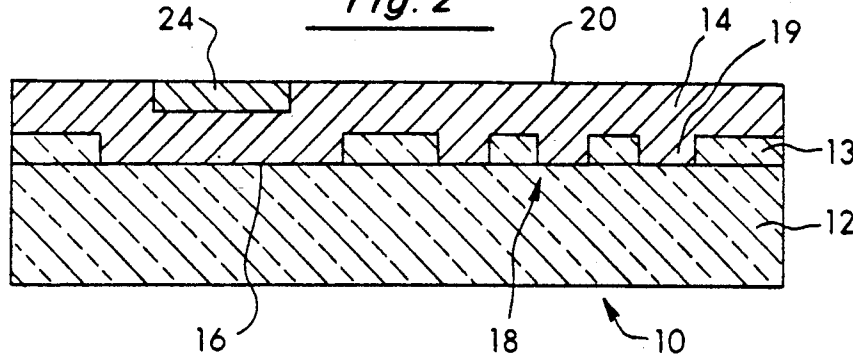


Fig. 3

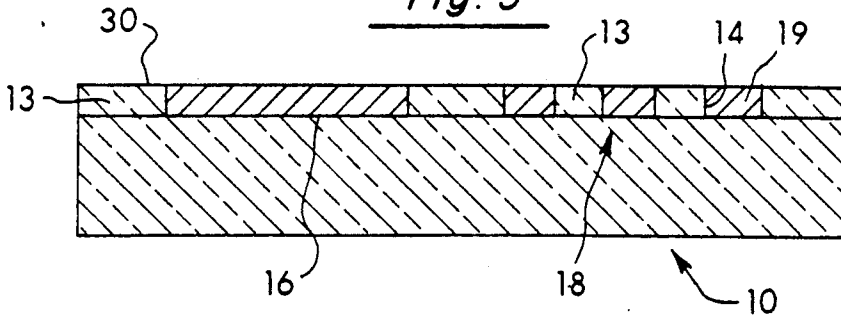


Fig. 4

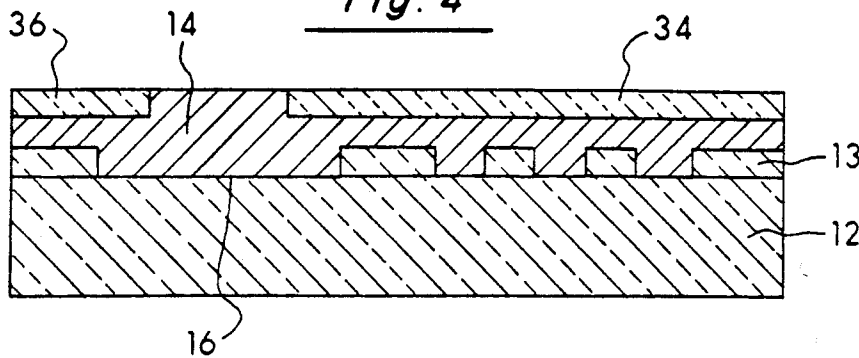


Fig. 5

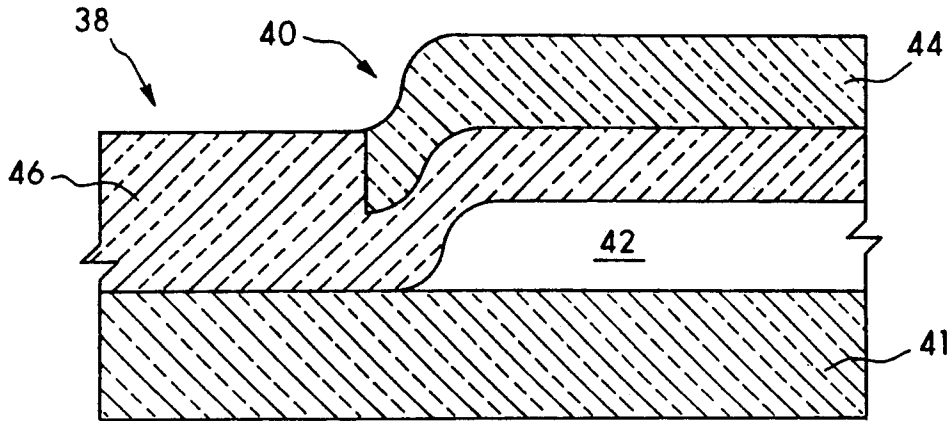


Fig. 6

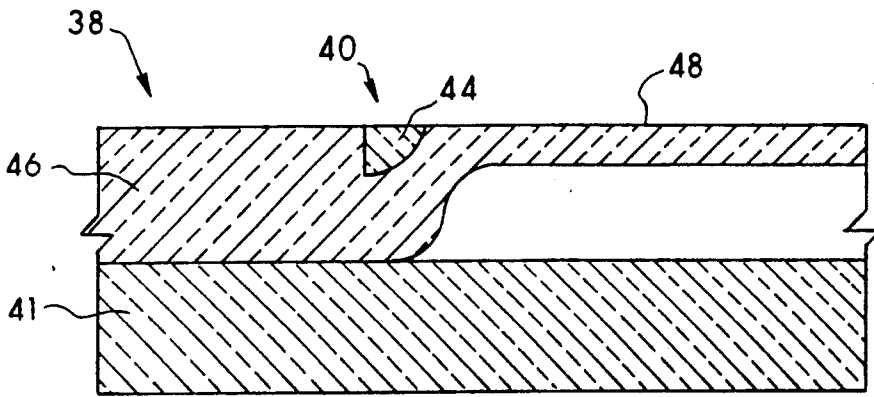


Fig. 7

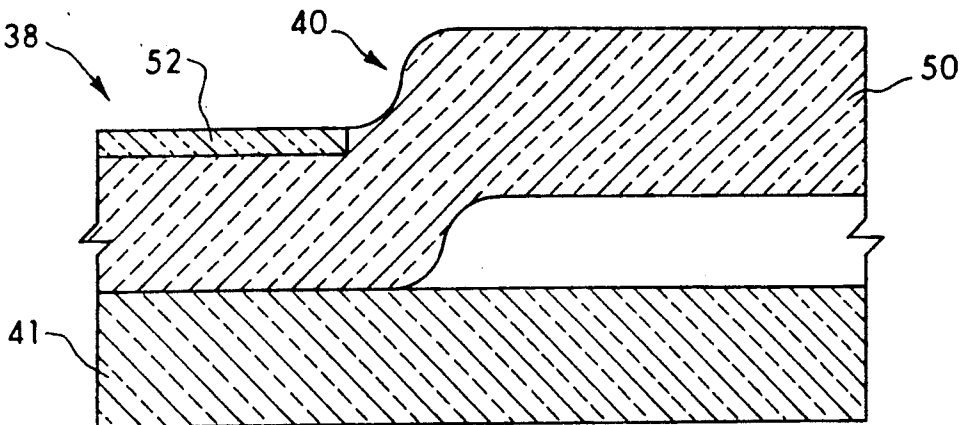


Fig. 8

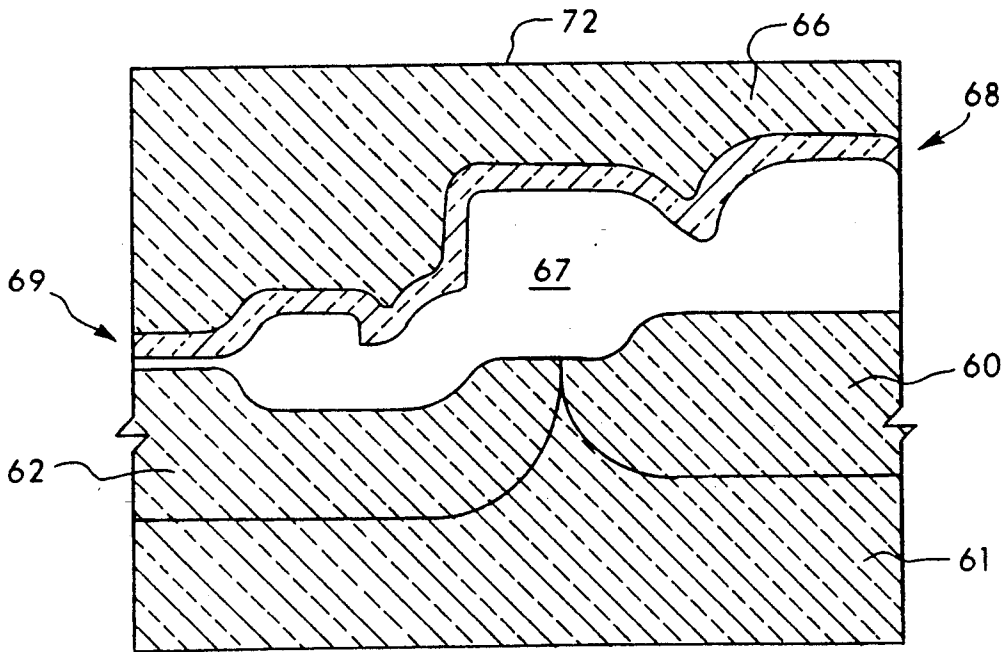
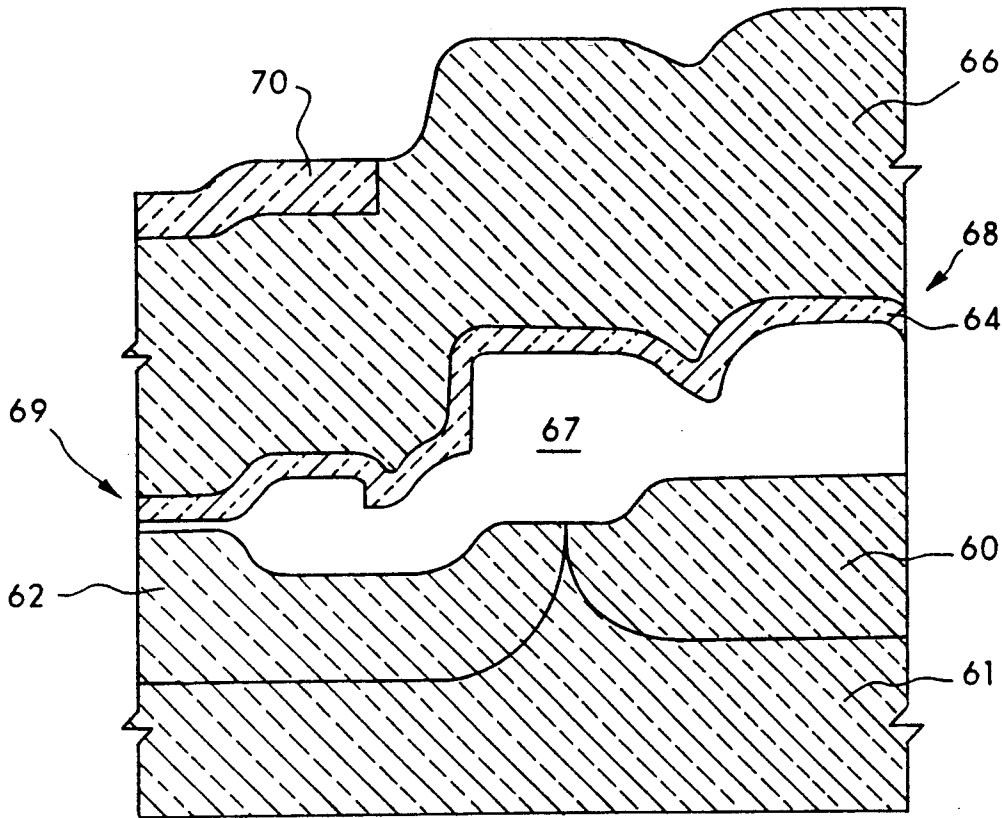


Fig. 9

Fig. 10A

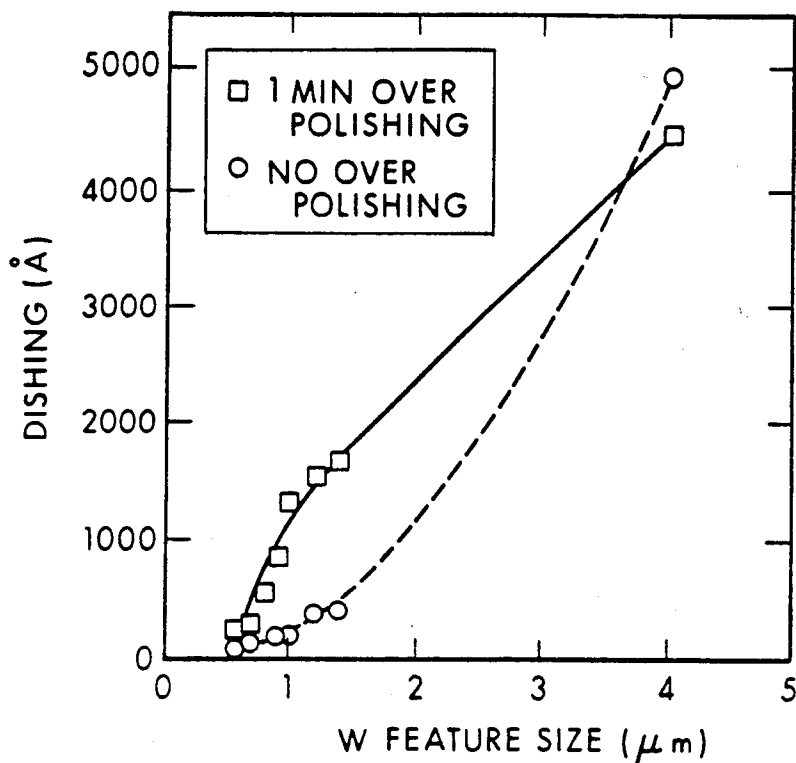
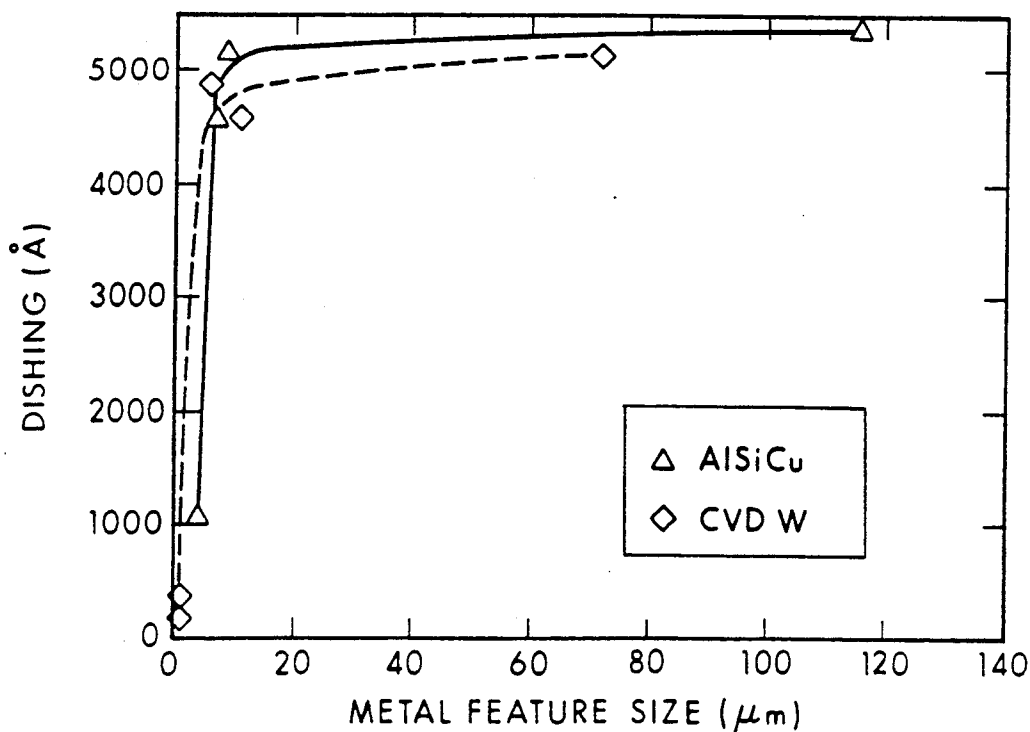


Fig. 10B



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