UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01246[1]
Patent 7,126,174 B2

PETITIONER'S UPDATED EXHIBIT LIST

[1] Case IPR2016-01247 has been consolidated with this proceeding.

In accordance with 37 C.F.R. § 42.63(e), Petitioner hereby submits a current listing of Taiwan Semiconductor Manufacturing Company, Ltd.'s exhibits to the Board and counsel for Patent Owner.

LIST OF EXHIBITS

Exhibit No.	Description	Previously Submitted
Exhibit 1001	U.S. Patent No. 7,126,174 to Segawa et al.	x
Exhibit 1002	U.S. Patent No. 5,153,145 to Lee et al.	x
Exhibit 1003	U.S. Patent No. 3,617,824 to Shinoda et al.	x
Exhibit 1004	Corrected Declaration of Dr. Sanjay Kumar Banerjee, Ph.D. in Support of Petition for *Inter Partes Review* of United States Patent No. 7,126,174 (IPR2016-01246).	x
Exhibit 1005	J.A. Appels et al., "Some Problems of MOS Technology," Philips Tech. Rev. vol. 31 nos. 7–9, pp. 225–36, 276 (1970).	x
Exhibit 1006	U.S. Patent No. 4,110,899 to Nagasawa et al.	x
Exhibit 1007	U.S. Patent No. 3,787,251 to Brand et al.	x
Exhibit 1008	B.B.M. Brandt et al., "LOCMOS, a New Technology for Complementary MOS Circuits," Philips Tech. Rev. vol. 34 no. 1, pp. 19–23 (1974).	x
Exhibit 1009	U.S. Patent No. 5,702,976 to Schuegraf et al.	x
Exhibit 1010	U.S. Patent No. 4,506,434 to Ogawa et al.	x
Exhibit 1011	U.S. Patent No. 4,957,590 to Douglas.	**x**

Exhibit No.	Description	Previously Submitted
Exhibit 1012	U.S. Patent No. 5,976,939 to Thompson et al.	x
Exhibit 1013	U.S. Patent No. 6,165,826 to Chau et al.	x
Exhibit 1014	U.S. Patent No. 5,733,812 to Ueda et al.	x
Exhibit 1015	U.S. Patent No. 5,539,229 to Noble, Jr. et al.	x
Exhibit 1016	U.S. Patent No. 5,521,422 to Mandelman et al.	x
Exhibit 1017	U.S. Patent No. 5,021,353 to Lowrey et al	x
Exhibit 1018	U.S. Patent No. 4,638,347 to Iyer	x
Exhibit 1019	Japanese Patent Application No. 7-192181 to Segawa et al.	x
Exhibit 1020	Certified Translation of Japanese Patent Application No. 7-192181 to Segawa et al.	x
Exhibit 1021	File History of U.S. Patent No. 7,126,174 to Segawa et al.	x
Exhibit 1022	File History of Japanese Patent Application No. 7 330112 to Segawa et al.	x
Exhibit 1023	Certified Translation of Portions of the File History of Japanese Patent Application No. 7 330112 to Segawa et al.	x
Exhibit 1024	Corrected Declaration of Dr. Sanjay Kumar Banerjee, Ph.D. in Support of Petition for *Inter Partes* Review of United States Patent No. 7,126,174 (IPR2016-01247).	x

Exhibit No.	Description	Previously Submitted
Exhibit 1025	E. Adler et al., "The Evolution of IBM CMOS DRAM Technology," IBM J. Res. Develp., vol. 39, no. 1/2, pp. 167-88 (Jan/Mar. 1995).	x
Exhibit 1026	Japanese Patent Application No. H03-379033 to Sumi et al.	x
Exhibit 1027	Certified Translation of Japanese Patent Application No. H03-379033 to Sumi et al.	x
Exhibit 1028	Japanese Patent Application No. S59-181062 to Horiguchi.	x
Exhibit 1029	Certified Translation of Japanese Patent Application No. S59-181062 to Horiguchi.	x
Exhibit 1030	Japanese Patent Application No. H07-183518 to Ueda et al.	x
Exhibit 1031	Certified Translation of Japanese Patent Application No. H07-183518 to Ueda et al.	x
Exhibit 1032	U.S. Patent No. 4,651,411 to Konaka et al.	x
Exhibit 1033	Japanese Patent Application No. S58-73163 to Konaka et al.	x
Exhibit 1034	U.S. Patent No. 6,218,266 to Sato et al.	x
Exhibit 1035	U.S. Patent No. 5,445,996 to Kodera et al.	x
Exhibit 1036	U.S. Patent No. 4,511,430 to Chen et al.	x
Exhibit 1037	U.S. Patent No. 4,599,789 to Gasner.	x
Exhibit 1038	U.S. Patent No. 4,855,247 to Ma et al.	x

Exhibit No.	Description	Previously Submitted
Exhibit 1039	U.S. Patent No. 5,102,816 to Manukonda et al.	x
Exhibit 1040	U.S. Patent No. 5,512,771 to Hiroki et al.	x
Exhibit 1041	U.S. Patent No. 5,648,284 to Kusunoki et al.	x
Exhibit 1042	S. Deleonibus et al., "Optimization of a Shallow Trench Isolation Refill Process for High Density Non Volatile Memories Using 100% Chemical-Mechanical Polishing: The BOX-ON Process," Extended Abstracts of the Spring 1994 Electrochem. Soc. Meeting, abstract no. 171, vol. 94-1, pp. 267-77 (May 22-27, 1994).	x
Exhibit 1043	J.M. Pierce et al., "Oxide-Filled Trench Isolation Planarized Using Chemical/Mechanical Polishing," Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology, vol. 91-11, pp. 650-56 (1991).	x
Exhibit 1044	Excerpts from C.Y. Chang & S.M. Sze, "ULSI Technology" (1996).	x
Exhibit 1045	Excerpts from S. Wolf, "Silicon Processing for the VLSI Era: Volume 1: Process Technology" (1986).	x
Exhibit 1046	Excerpts from S. Wolf, "Silicon Processing for the VLSI Era: Volume 2: Process Integration" (1990).	x
Exhibit 1047	H.W. Fry et al., "Applications of APCVD TEOS/O3 Thin Films in ULSI IC Fabrication," Solid State Tech., pp. 31-40 (Mar. 1994).	x

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