Filed on behalf of Godo Kaisha IP Bridge 1
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
and GLOBALFOUNDRIES U.S. INC.,
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01246[1]
U.S. Patent No. 7,126,174

PATENT OWNER'S CURRENT EXHIBIT LIST
(As of August 3, 2017)

Mail Stop PATENT BOARD, PTAB
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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[1] Case IPR2016-01247 has been consolidated with this proceeding. GlobalFoundries U.S. Inc.'s motions for joinder in Cases IPR2017-00925 and IPR2017-00926 were granted.

PATENT OWNER'S CURRENT EXHIBIT LIST
(As of August 3, 2017)

Exhibit No.	Description	Newly Submitted
2001	Substitute Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Preliminary Response filed in IPR2016-01246 on October 5, 2016.	Served on January 27, 2017
2002	Schematic illustration of the Chemical Mechanical Polishing process from Steigerwald, Murarka, and Gutmann, *Chemical Mechanical Planarization of Microelectronic Materials* (1997).	
2003	Schematic illustration of the Chemical Mechanical Polishing process from the Motorola Company. SCSolutions.com. Accessed September 30, 2016. http://www.scsolutions.com/chemical-mechanical-planarization-cmp-controllers-0.	
2004	Photograph of a Chemical Mechanical Polishing Tool from the Applied Materials Company. BusinessWire.com. Accessed October 5, 2016. http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion.	
2005	Troxel, Boning, McIlrath "Semiconductor Process Representation." *Wiley Encyclopedia of Electrical and Electronics*, pp.139 –147 (1999).	
2006	U.S. Patent No. 6,052,319 to Jacobs.	
2007	U.S. Patent No. 6,952,656 to Cordova et al.	

Exhibit No.	Description	Newly Submitted
2008	Hunt, "Low Budget Undergraduate Microelectronics Laboratory." *University Government Industry Microelectronics Symposium*, pp.81-87 (2006).	
2009	U.S. Patent No. 7,074,709 to Young.	
2010	Burckel, "3D-ICs created using oblique processing." *Advanced in Patterning Materials and Processes XXXIII*, pp. 1–12 (2016).	
2011	Substitute Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Preliminary Response filed in IPR2016-01247 on October 7, 2016.	Served on January 27, 2017
2012	Corrected Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Response filed in IPR2016-01246 on March 24, 2017.	
2013	Thompson, L. F. "An Introduction to Lithography." *Introduction to Microlithography*, ACS Symposium Ser., American Chemical Society, pp. 1-13 (1983).	
2014	CA1275846 C to Roland et al.	
2015	U.S. Patent No. 5,314,843 to Yu et al.	
2016	U.S. Patent No. 5,231,306 to Meikle et al.	
2017	U.S. Patent No. 4,529,621 to Ballard.	
2018	U.S. Patent No. 5,310,624 to Ehrlich.	
2019	U.S. Patent No. 5,097,422 to Corbin, II et al.	
2020	Declaration of Amanda Dove.	
2021	U.S. Patent No. 4,952,524 to Lee et al.	

Exhibit No.	Description	Newly Submitted
2022	Bryant, A.; Haensch, W.; Geissler, S; Mandelman, Jack; Poindexter, D.; and Steger, M. "The Current-Carrying Corner Inherent to Trench Isolation." *IEEE Electron Device Letters*, Vol. 14, No. 8, pp. 412-414 (1993).	
2023	Ohe, Kikuyo; Odanaka, Shinji; Moriyama, Kaori; Hori, Takashi; and Fuse, Genshu. "Narrow-Width Effects of Shallow Trench-Isolated CMOS with n+-Polysilicon Gate." *IEEE Transactions on Electron Devices*, Vol. 36, No. 6, pp. 1110-1116 (1989).	
2024	Shigyo, N.; Wada, T.; Fukuda, S.; Hieda, K., Hamamoto, T.; Watanabe, H.; Sunouchi, K.; and Tango, H. "Steep Subthreshold Characteristic and Enhanced Transconductance of Fully-Recessed Oxide (Trench) Isolated 1/4 μm Width MOSFETs." *1987 International Electron Devices Meeting*, pp. 636-639 (1987).	
2025	Furukawa, T., and Mandelman, J.A. "Process and Device Simulation of Trench Isolation Corner Parasitic Device." *Journal Of The Electrochemical Society*, Vol. 135, No. 8, p. 358C, Item 236 (1988).	
2026	"Structural Analysis Sample Report" downloaded from https://www.chipworks.com/TOC/Structural_Analysis_Sample_Report.pdf (2013).[2]	
2027	U.S. Patent No. 4,776,922 to Bhattacharyya et al.	

[2] Date corrected from 2008 to 2013.

Exhibit No.	Description	Newly Submitted
2028	Subbanna, S.; Ganin, E.; Crabbé, E.; Comfort, J.; Wu, S.; Agnello, P.; Martin, B.; McCord, M.; Newman, H. Ng. T.; McFarland, P.; Sun, J.; Snare, J.; Acovic, A.; Ray, A.; Gehres, R.; Schulz, R.; Greco, S.; Beyer, K.; Liebmann, L.; DellaGuardia, R.; Lamberti, A. "200 mm Process Integration for a 0.15 µm Channel-Length CMOS Technology Using Mixed X-Ray / Optical Lithography." *Proceedings of 1994 IEEE International Electron Devices Meeting*, pp. 695-698 (1994).	
2029	Chung, J.; Jeng, M.-C.; Moon, J.E.; Wu, A.T.; Chan, T.Y.; Ko, P.K.; Hu, Chenming. "Deep-Submicrometer MOS Device Fabrication Using a Photoresist-Ashing Technique." *IEEE Electron Device Letters*, Vol. 9. No. 4, pp. 186-188 (1988).	
2030	Tanaka, Tetsu; Suzuki, Kunihiro; Horie, Hiroshi; Sugii, Toshihiro. "Ultrafast Low-Power Operation of p^+-n^+ Double-Gate SOI MOSFETS." *1994 Symposium on VLSI Technology Digest of Technical Papers*, pp. 11-12 (1994).	
2031	WIPO Publication No. WO 90/05377 to Lowrey.	
2032	Kaufman, F. B.; Thompson, D. B.; Broadie, R. E.; Jaso, M. A.; Guthrie, W. L.; Pearson, D. J.; and Small, M. B. "Chemical-Mechanical Polishing for Fabricating Patterned W Metal Features as Chip Interconnects." *Journal of The Electrochemical Society*, Vol. 138, No. 11, pp. 3460-3465 (1991).	

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