VERIFICATION OF TRANSLATION

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declare that I am well acquainted with both the Japanese and English languages, and that the attached is an accurate partial translation, to the best of my knowledge and ability, of Japanese Patent Application Publication No. H9-97838 (translation of first and last pages only), published April 8, 1997.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-captioned application or any patent issued thereon.

Signature _____ Date 6-28-2017

Yukiko Toyoda Buntin

Exhibit 2065

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To be continued on the last page

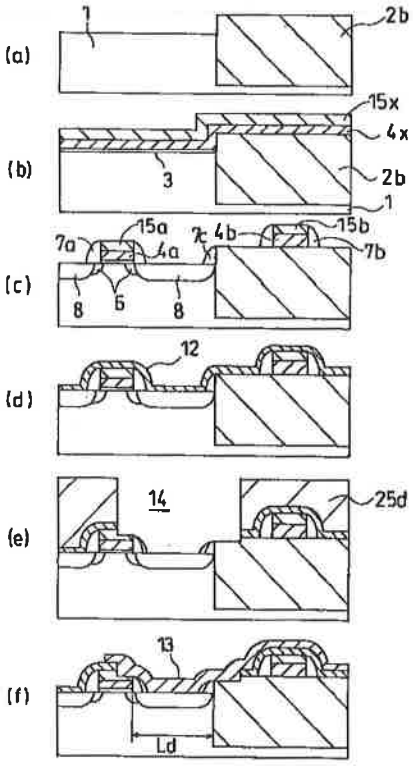
(54) Title of Invention

SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

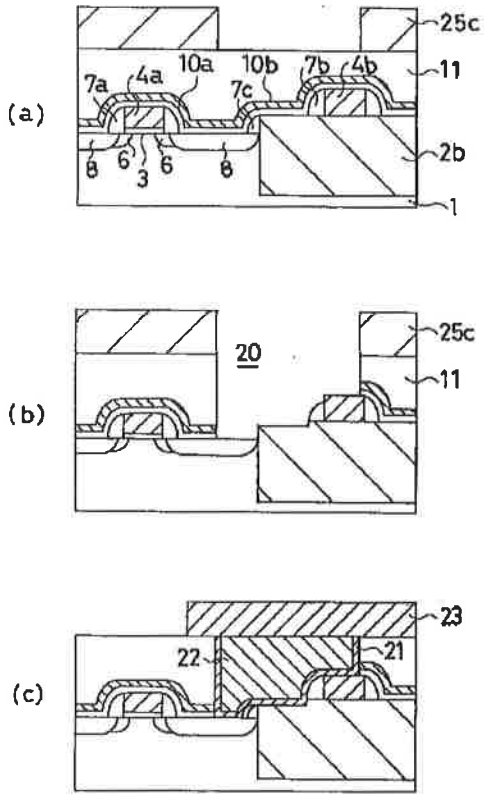
(57)【要約】

【課題】　半導体装置における接合耐圧の低下や接合リーク電流の増大を招くことなく、半導体装置の集積度を向上させ、占有面積を低減する。

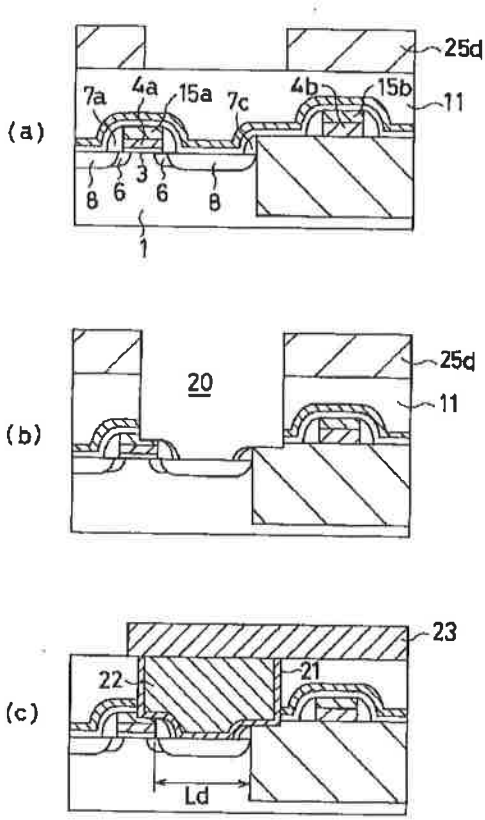
【解決手段】　シリコン基板１の活性領域よりも階段状に高い素子分離２ｂを形成し、活性領域上にゲート酸化膜３，ゲート電極４ａ，ゲート上保護膜１５ａ，サイドウォール７ａ等からなるＦＥＴを形成する。基板の全面上に絶縁膜１２を堆積し、絶縁膜１２の上に、活性領域から素子分離２ｂの一部及びゲート上保護膜１５ａに亘る領域の上を開口したレジスト膜２５ｄを形成する。接続孔１４の形成領域に素子分離２ｂ等と干渉しないための合わせマージンが不要となる。素子分離２ｂが活性領域よりも階段状に高いので、接続孔１４形成時のオーバーエッチングによって、活性領域内の不純物濃度の低い部分に接するほど素子分離２ｂが深く除去されるのが防止される。



【図１０】



【図１１】



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