

[54] SPLIT-POLYSILICON CMOS PROCESS INCORPORATING SELF-ALIGNED SILICIDATION OF CONDUCTIVE REGIONS

[75] Inventors: Tyler A. Lowrey; Dermot M. Durcan; Trung T. Doan; Gordon A. Haller; Mark E. Tuttle, all of Boise, Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

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[51] Int. Cl.<sup>5</sup> ..... H01L 21/265; H01L 21/336

[52] U.S. Cl. .... 437/34; 437/44; 437/57; 357/42; 357/44

[58] Field of Search ..... 437/27, 28, 29, 30, 437/34, 56, 57, 200, 192, 40, 41, 44, 233; 357/23.3, 23.4, 40, 41, 42, 44

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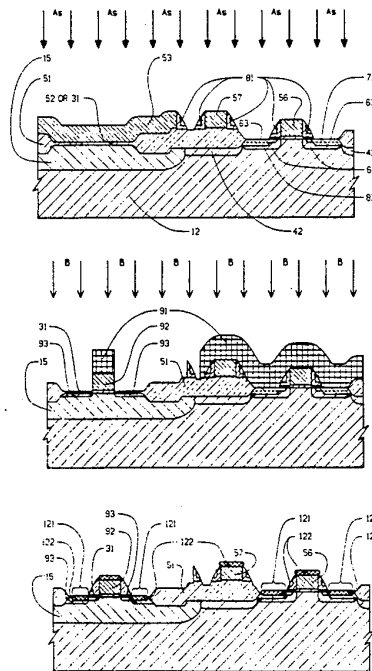
Primary Examiner—Olik Chaudhuri  
Assistant Examiner—M. Wilczewski

Attorney, Agent, or Firm—Angus C. Fox, III; Stanley N. Protigal; Albert Crowder

[57] ABSTRACT

An improved CMOS fabrication process which uses separate masking steps to pattern N-channel and P-channel transistor gates from a single layer of conductively-doped polycrystalline silicon (poly) and incorporates self-aligned silicidation of conductive regions. The object of the improved process is to reduce the cost and improve the reliability, performance and manufacturability of CMOS devices by a process which features a dramatically reduced number of photomasking steps and which further allows self-aligned silicidation of transistor conductive regions. By processing N-channel and P-channel devices separately, the number of photomasking steps required to fabricate complete CMOS circuitry in a single-polysilicon-layer or single-metal layer process can be reduced from eleven to eight. Starting with a substrate of P-type material, N-channel devices are formed first, with unetched poly left in the future P-channel regions until N-channel processing is complete. The improved CMOS process provides the following advantages over conventional process technology: Use of a masked high-energy punch-through implant for N-channel devices is not required; individual optimization of N-channel and P-channel transistors is made possible; a lightly-doped drain (LDD) design for both N-channel and P-channel transistors is readily implemented; source/drain-to-gate offset may be changed independently for N-channel and P-channel devices; and N-channel and P-channel transistors can be independently controlled and optimized for best LDD performance and reliability.

5 Claims, 13 Drawing Sheets



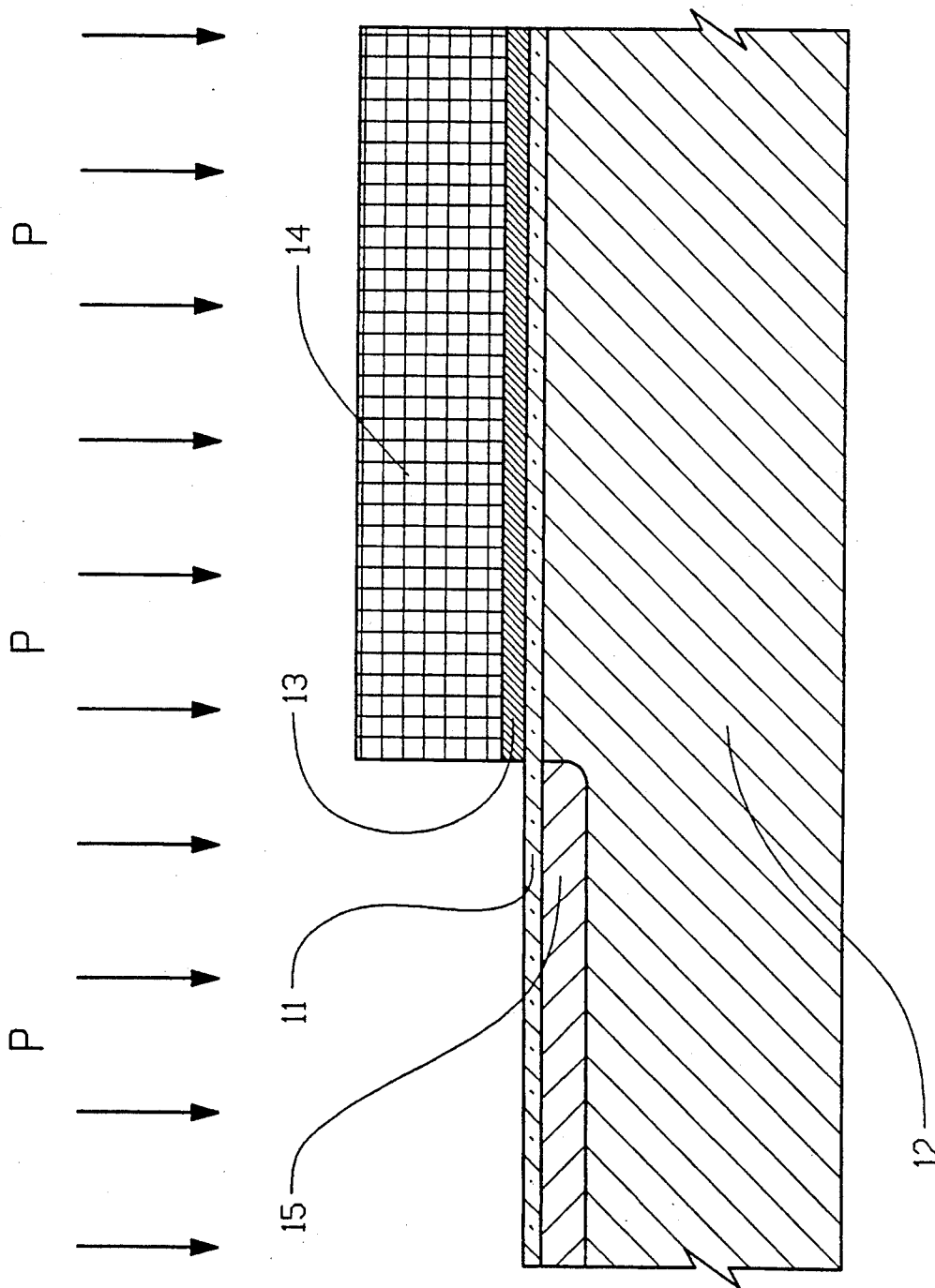


FIG. 1

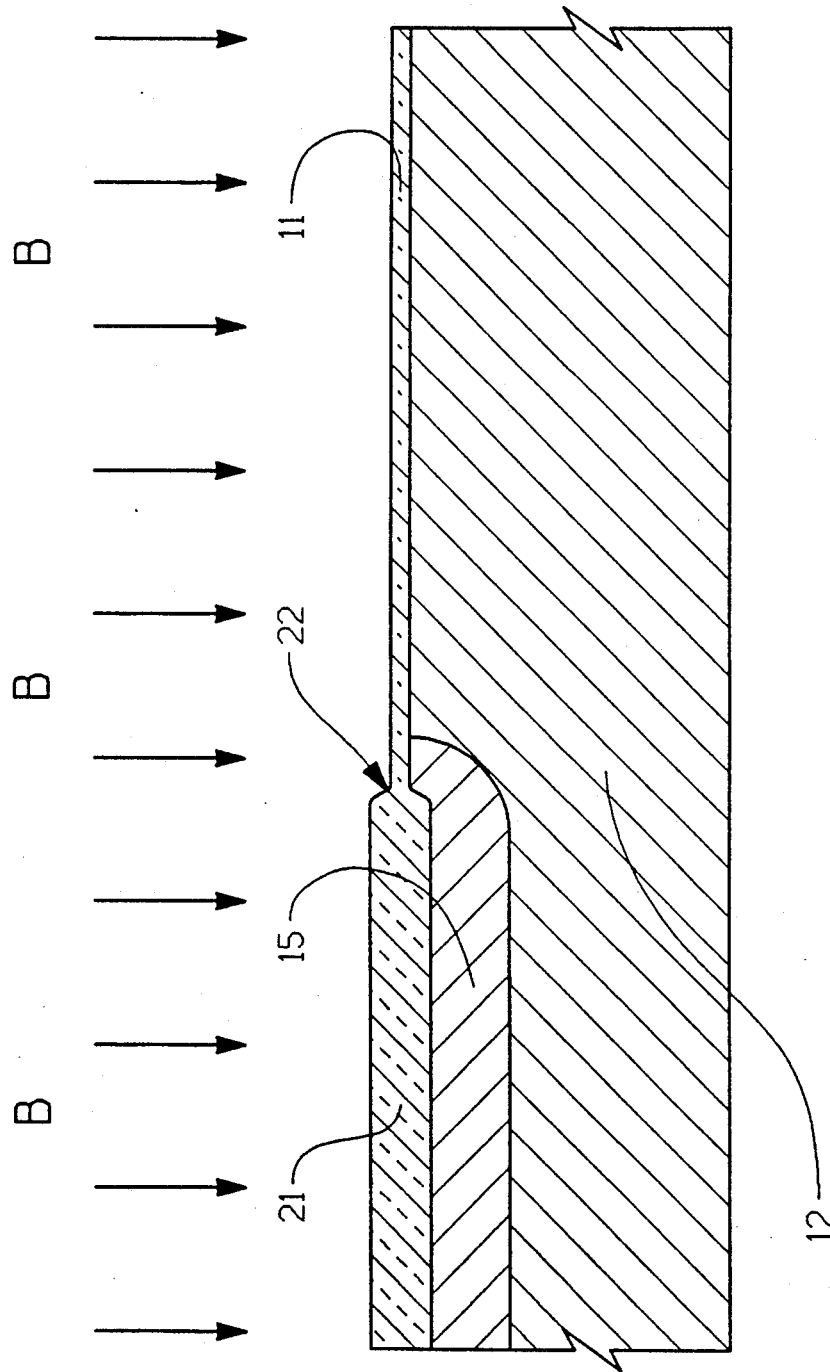


FIG. 2

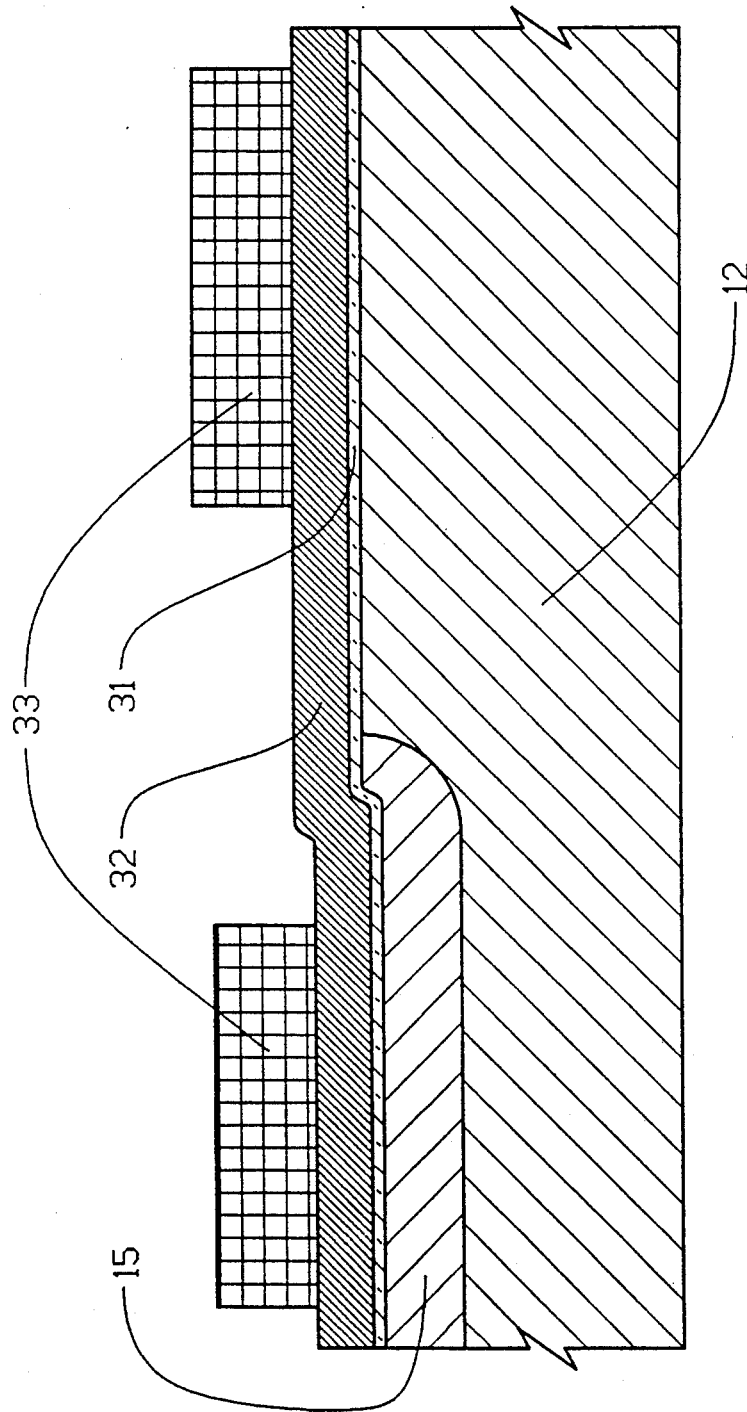


FIG. 3

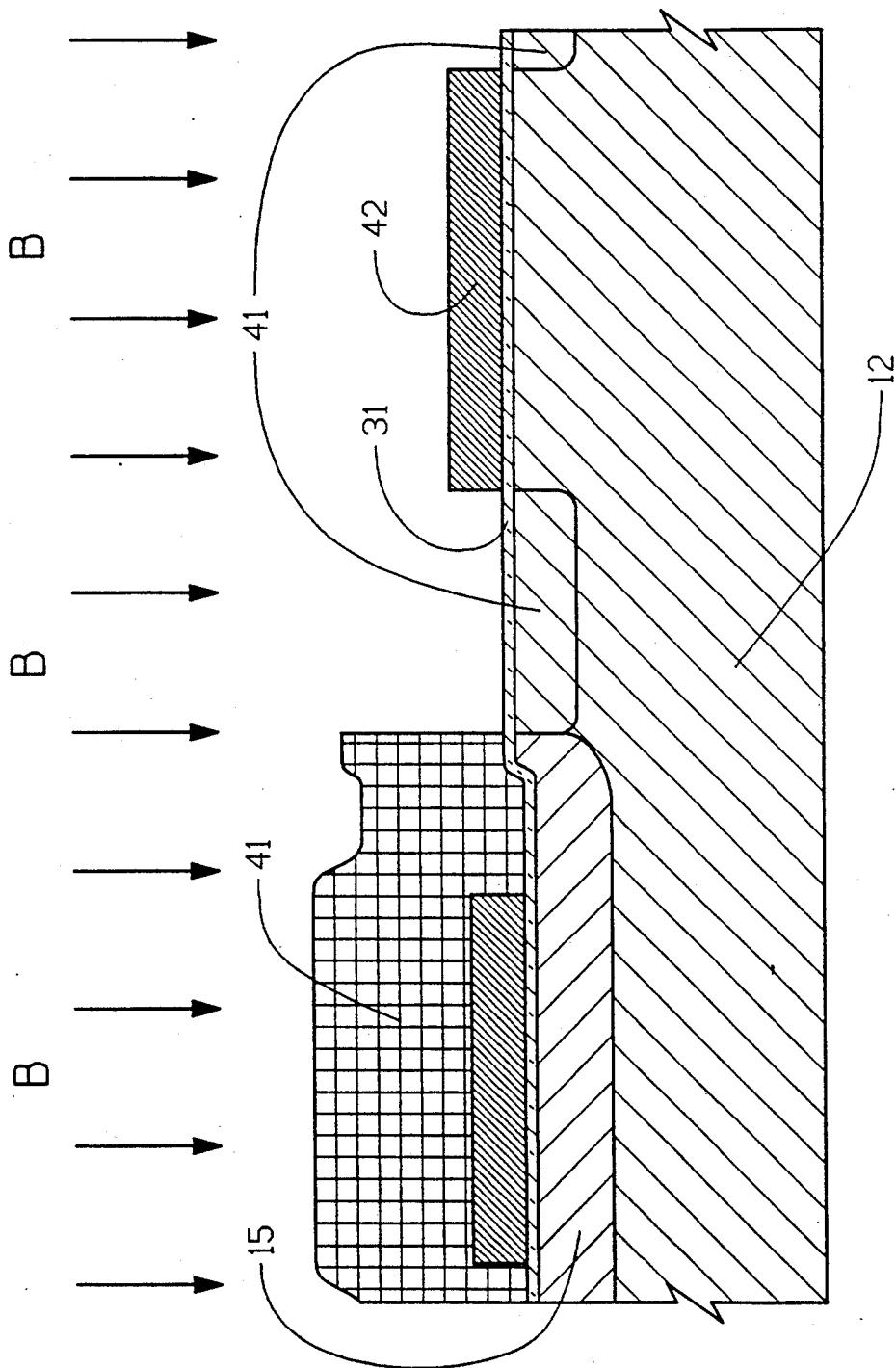


FIG. 4

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