

United States Patent [19]

Noble, Jr et al.

[54] MOSFET WITH RAISED STI ISOLATION SELF-ALIGNED TO THE GATE STACK

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- [21] Appl. No.: 365,729
- [22] Filed: Dec. 28, 1994
- [51] Int. Cl.⁶ H01L 27/08; H01L 29/76;
- H01L 29/00 [52] **U.S. Cl.** **257/301**; 257/305; 257/397;

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US005539229A

[11] **Patent Number:** 5,539,229

[45] Date of Patent: Jul. 23, 1996

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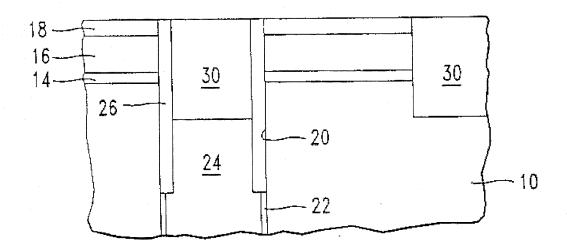
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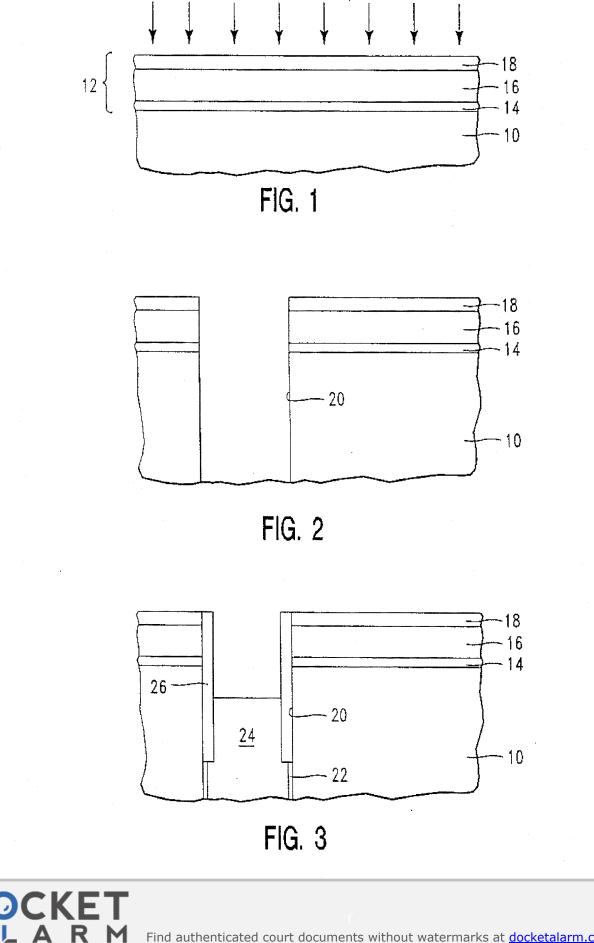
Primary Examiner-Donald L. Monin, Jr. Attorney, Agent, or Firm-James M. Leas

[57] ABSTRACT

A semiconductor structure comprising a transistor having a gate conductor that has first and second edges bounded by raised isolation structures (e.g. STI). A source diffusion is self-aligned to the third edge and a drain diffusion is self-aligned to the fourth edge of the gate electrode.

19 Claims, 5 Drawing Sheets





Jul. 23, 1996

VT CHANNEL IMPLANT

Sheet 1 of 5

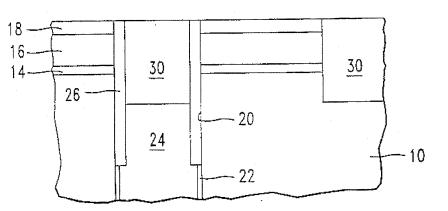
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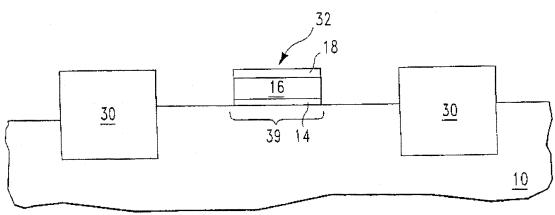


FIG. 5

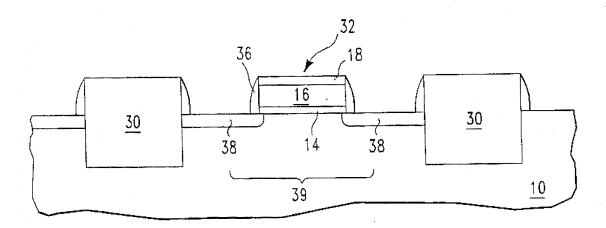
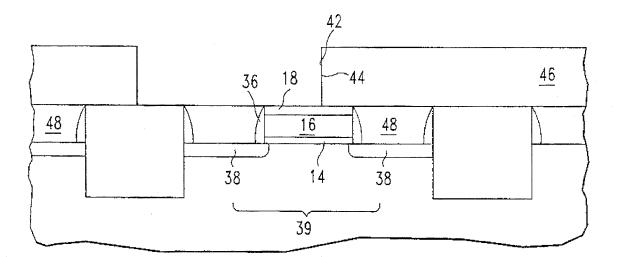


FIG. 6

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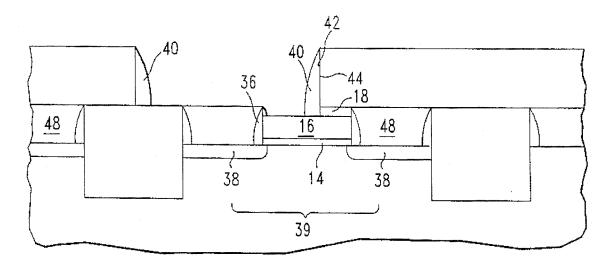
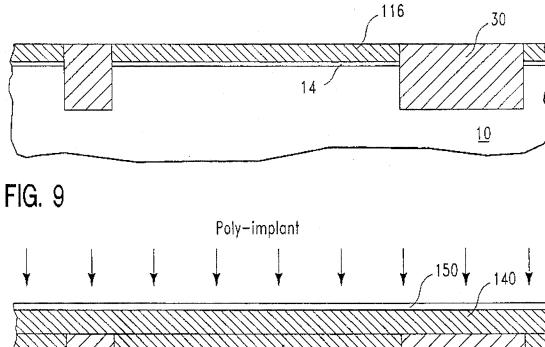


FIG. 8

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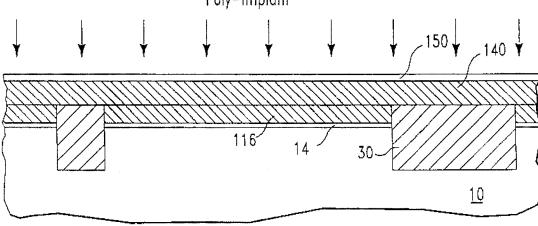


FIG. 10

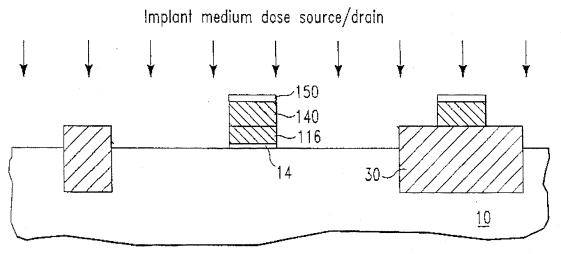


FIG. 11

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