



US006165826A

United States Patent [19]

[11] Patent Number: **6,165,826**

Chau et al.

[45] Date of Patent: ***Dec. 26, 2000**

[54] **TRANSISTOR WITH LOW RESISTANCE TIP AND METHOD OF FABRICATION IN A CMOS PROCESS**

[75] Inventors: **Robert S. Chau**, Beaverton; **Chia-Hong Jan**, Portland; **Chan-Hong Chern**, Portland; **Leopoldo D. Yau**, Portland, all of Oreg.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

5,162,263	11/1992	Kunishima et al.	437/200
5,168,072	12/1992	Moslehi	437/41
5,231,042	7/1993	Ilderem et al.	437/44
5,285,088	2/1994	Sato et al.	257/192
5,336,903	8/1994	Ozturk et al.	257/19
5,341,014	8/1994	Fujii et al.	257/377
5,352,631	10/1994	Sitaram et al.	437/200
5,393,685	2/1995	Yoo et al.	437/44
5,397,909	3/1995	Moslehi	257/383
5,405,795	4/1995	Beyer et al.	437/89

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

8448061	5/1998	European Pat. Off.	
361051959	3/1986	Japan	438/FOR 168

[21] Appl. No.: **08/581,243**

[22] Filed: **Dec. 29, 1995**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/363,749, Dec. 23, 1994, Pat. No. 5,710,450.

[51] Int. Cl.⁷ **H01L 21/8238**

[52] U.S. Cl. **438/231**; 438/226; 438/233; 438/232; 438/305; 438/306; 438/586; 438/589; 438/576; 438/558; 438/561; 438/664

[58] **Field of Search** 438/589-663, 438/664, 191, 226-223, 229, 230, 231, 232, 259, 270, 330, 301, 303, 305, 306, 586, 576, 558, 565, 581, 583, FOR 168, FOR 180, FOR 197, FOR 216, FOR 217, FOR 218, FOR 251, FOR 250, FOR 219; 148/DIG. 147, DIG. 19, DIG. 59; 257/288, 900

[56] References Cited

U.S. PATENT DOCUMENTS

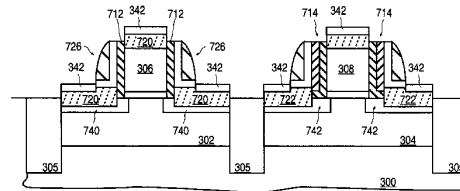
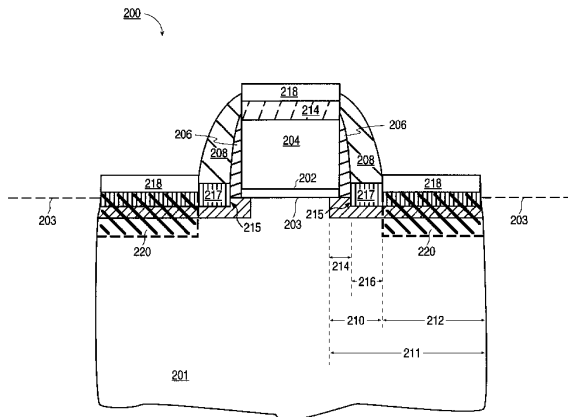
4,133,704	1/1979	MacIver et al.	148/1.5
4,683,645	8/1987	Naguib et al.	437/41
4,876,213	10/1989	Pfiester	437/34
4,998,150	3/1991	Rodder et al.	357/23.1
5,006,476	4/1991	De Jong et al.	437/31

Primary Examiner—Long Pham
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman LLP

[57] ABSTRACT

A novel transistor with a low resistance ultra shallow tip region and its method of fabrication in a complementary metal oxide semiconductor (CMOS) process. According to the preferred method of the present invention, a first gate dielectric and a first gate electrode are formed on a first portion of a semiconductor substrate having a first conductivity type, and a second gate dielectric and a said gate electrode are formed on a second portion of semiconductor substrate having a second conductivity type. A silicon nitride layer is formed over the first portion of the semiconductor substrate including the first gate electrode and over the second portion of the semiconductor substrate including the second gate electrode. The silicon nitride layer is removed from the second portion of the silicon substrate and from the top of the second gate electrode to thereby form a first pair of silicon nitride spacers adjacent to opposite sides of the second gate electrode. A pair of recesses are then formed in the second portion of the semiconductor substrate in alignment with the first pair of sidewall spacers. A selectively deposited semiconductor material is then formed in the recesses.

52 Claims, 13 Drawing Sheets



U.S. PATENT DOCUMENTS		5,620,912	4/1997	Hwang et al.	438/301		
5,478,776	12/1995	Luftman et al.	437/163	5,710,450	1/1998	Chau et al.	257/344
5,538,909	7/1996	Hsu	437/35	5,726,071	3/1998	Segawa et al.	437/57
5,569,624	10/1996	Weiner	437/200	5,770,507	6/1998	Chen et al.	438/305

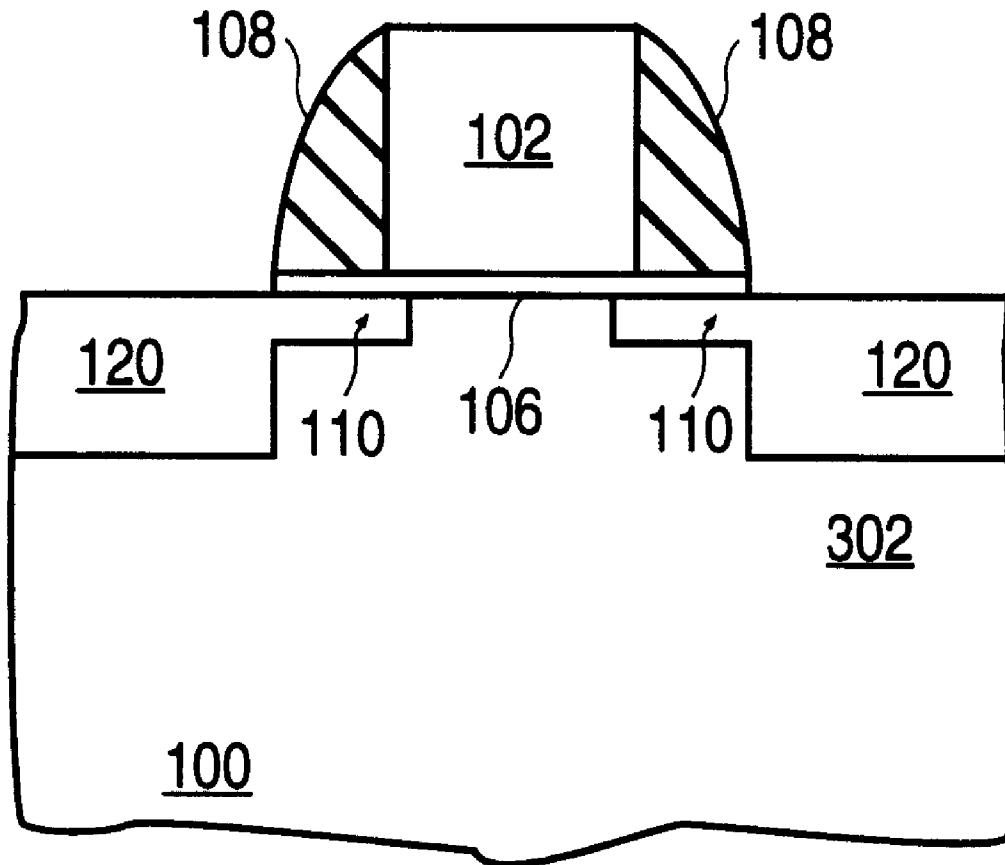


FIG. 1 (PRIOR ART)

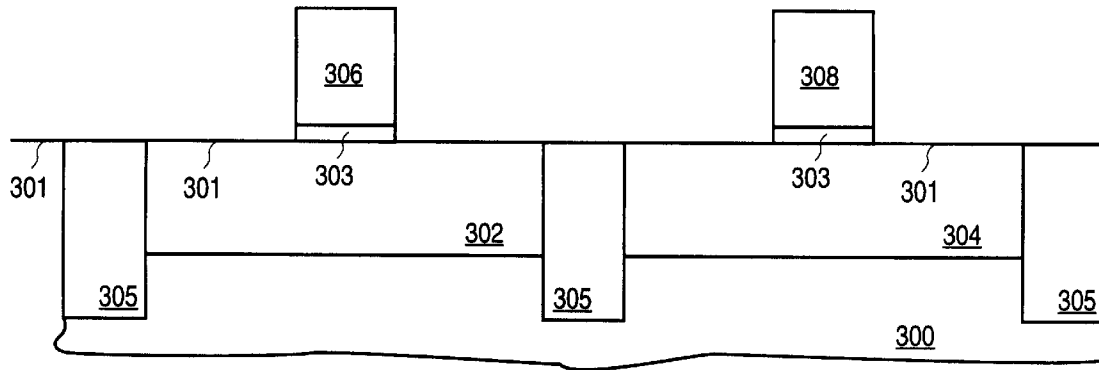


FIG. 3A

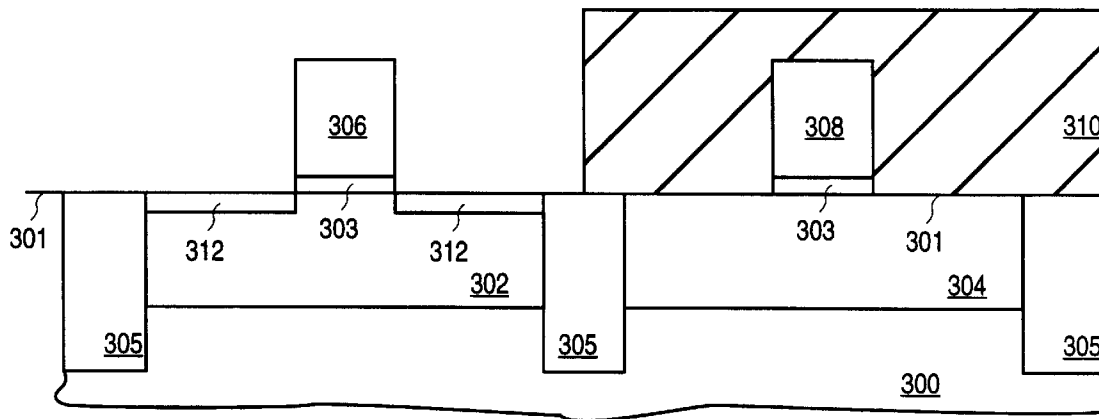


FIG. 3B

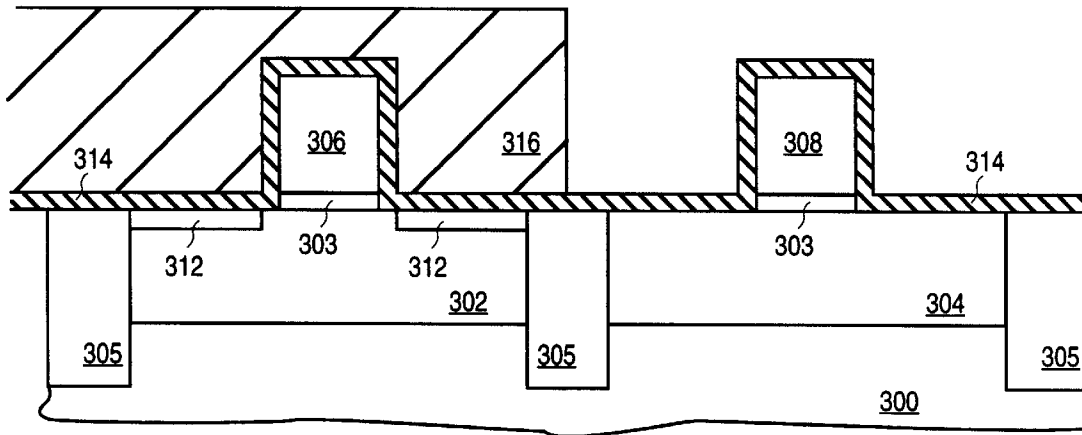


FIG. 3C

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.