A Trench Isolation Process for BiCMOS Circuits

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ABSTRACT

A new isolation process using 1 μm deep trench is developed for BiCMOS circuits. Well behaved MOSFETs and NPN devices with excellent parasitic performance were achieved. Low leakage diodes with butted junctions were demonstrated by inclusion of an oxidation barrier in the trench liner and utilizing a GeO_2 doped oxide with matched thermal coefficient of expansion to the silicon substrate for trench fill. Planarity for arbitrary width isolation was obtained by using oxide RIE followed by chemical-mechanical polishing.

INTRODUCTION

Trench isolation has been reported since the early 1980's as a replacement for LOCOS isolation for VLSI. However, process complexity associated with trench technology has restricted its appeal to a limited number of circuit applications while continuous modifications and improvements to LOCOS has enabled its implementation in a proposed 16 Mbit fast SRAM cell with 1 μm active pitch [1]. Nevertheless, LOCOS is not expected to scale significantly beyond 1 μm pitch due to its intrinsic limitations such as field oxide thinning, bird's beak encroachment, lack of planarity, and punchthrough. As a result, trench isolation is required to meet the demands of ULSI. However, a relatively simple process with sufficient benefits must be developed to gain wide acceptance.

In this paper, a single isolation process utilizing a 1 μm deep trench with arbitrary width is proposed for BiCMOS circuits to avoid the complexity of shallow and deep trench isolation typically employed in high performance BiCMOS technology [2]. A schematic representation of the structure is shown in Figure 1. Latchup immunity, intrawell and interwell isolations, reduced parameter capacitance, as well as bipolar parasitic reduction are simultaneously satisfied with the proposed structure. The processing technique used to fabricate this structure and the electrical results achieved are described.

FABRICATION

The process platform was adopted from a 0.5 μm BiCMOS technology developed for 4 Mbit fast SRAMs [3]. Epi thickness is optimized to ensure up-diffusion from the buried layers to merge with the trench bottom to obtain the desired isolation and parasitic characteristics. A hard mask is used to protect the active regions for etching of a 1 μm depth trench into the substrate. Both thermal oxide and composite thermal oxide/deposited nitride trench liners were evaluated along with several chemical vapor deposited oxides to determine the most suitable combination of processes to minimize defect generation in the substrate and to minimize seam or void formation in narrow width trenches.

A combination of oxide RIE and chemical mechanical polishing process [4,5] is used for the planarization of arbitrary width trench. A schematic cross section of the planarization process sequence is shown in Figure 2. Compared to [4], this planarization sequence has a reduced number of process steps and has replaced the more complex planarization etchback process with an oxide RIE process. At this point, MOS and bipolar devices were fabricated using previously reported processes [3] to evaluate the merit of the proposed structure.

RESULTS AND DISCUSSION

Transistor characteristics were measured on both CMOS and non-self-aligned NPN devices. Typical 0.5 μm Wdrawn subthreshold characteristics are shown in Figure 3. Both n- and p- channel devices exhibit ideal behavior with no degradation of the subthreshold slope. A Gummel plot for 0.8 μm emitter NPN is shown in Figure 4. Functional BiCMOS and ECL ring oscillators were also achieved.

Field punchthrough voltage on intrawell and interwell isolation structures are shown in Figure 5. Results measured on trench isolated structures were independent of field width and are well above 10 volts. Holding voltage for latchup and parasitic bipolar gain are improved compared to a PBL isolation control because current path in the substrate is interrupted by the trench bottom reaching into up-diffusion from the buried layer. These results are shown in Figures 6 and 7, respectively. A SEM micrograph which illustrates this is shown in Figure 8.

Deposited oxides are typically known to create voids and weak seams in narrow width and high aspect ratio trenches after wet strips/cleans due to poor step coverage. However, this problem is improved with ozone enhanced depositions [6,7] and ECR deposited films. Leakage current measured between gate poly combs in an on-pitch array for two different oxide trench fill is shown in Figure 9. A TEM cross section micrograph showing planar and defect-free isolation trench is shown in Figure 10.

In order to alleviate stress induced leakage caused by substrate defects due to oxidation and other thermal processes in 1 μm deep oxide filled trench, composite thermal oxide/CVD nitride trench liner [8,9] and trench fill with matched thermal coefficient expansion to the substrate [6] were evaluated. Stress

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measurement obtained on oxide trench fill film doped with GeO_2 is shown in Figure 11. Leakage measured on butted diodes with and without nitride liner are compared in Figure 12.

Gate oxide thinning at the trench corner which can degrade intrinsic dielectric breakdown was avoided by careful optimization of the process module. The results are shown in Figure 14.

SUMMARY

A simple trench isolation process that can simultaneously satisfy several requirements for submicron BiCMOS circuits is proposed and described. Well-behaved devices with excellent isolation and parasitic characteristics are demonstrated.

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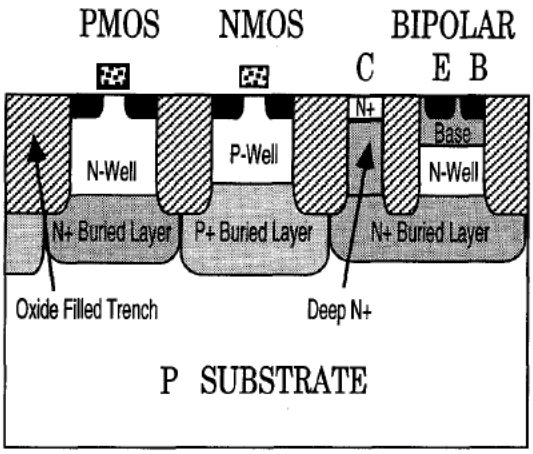


Fig. 1 Trench Isolated BiCMOS Architecture

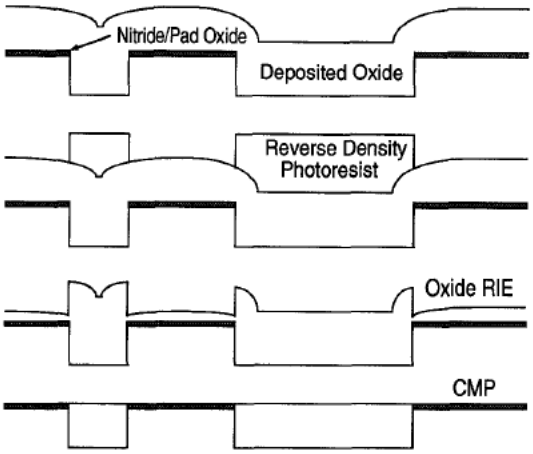


Fig. 2 Planarization Process Sequence

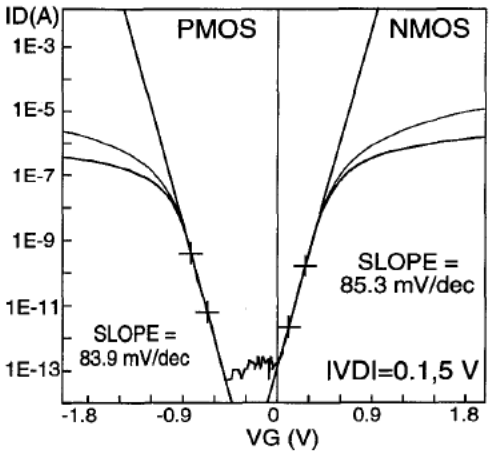


Fig. 3 MOS Subthreshold Characteristics

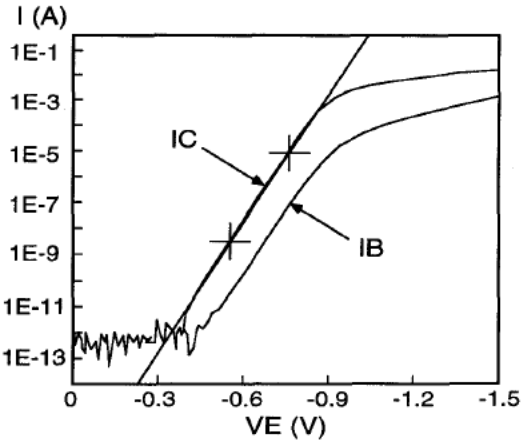


Fig. 4 Bipolar Characteristics

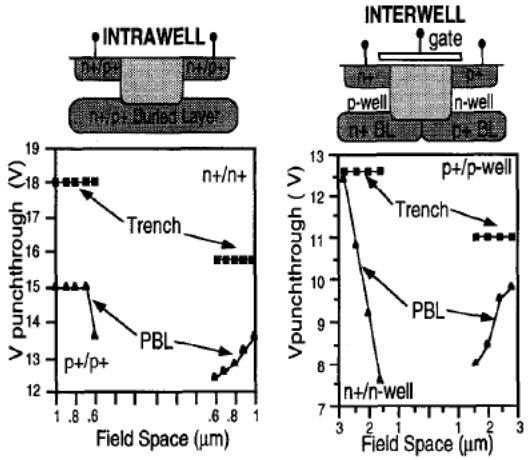


Fig. 5 Field Punchthrough Voltage

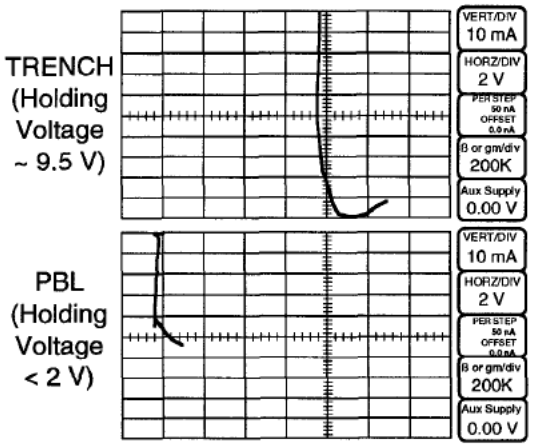


Fig. 6 Latch-Up Characteristics

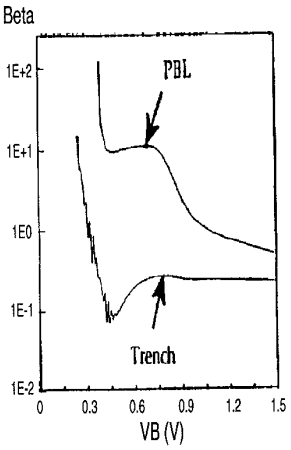
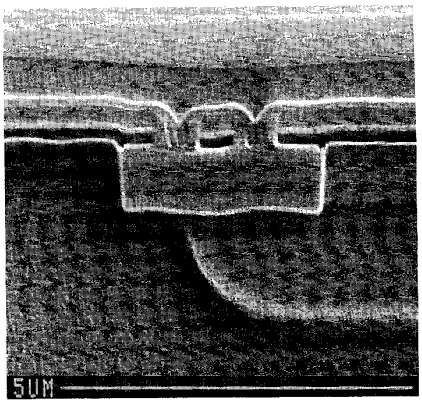


Fig. 7 Parasitic PNP Bipolar Gain



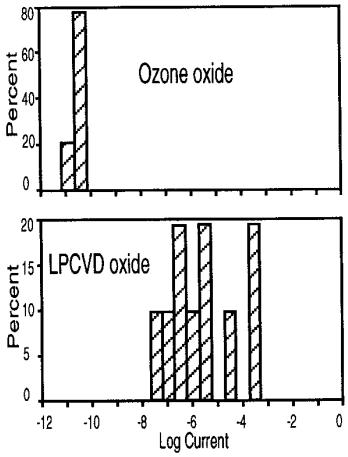


Fig. 9 Leakage between Gate Poly Combs

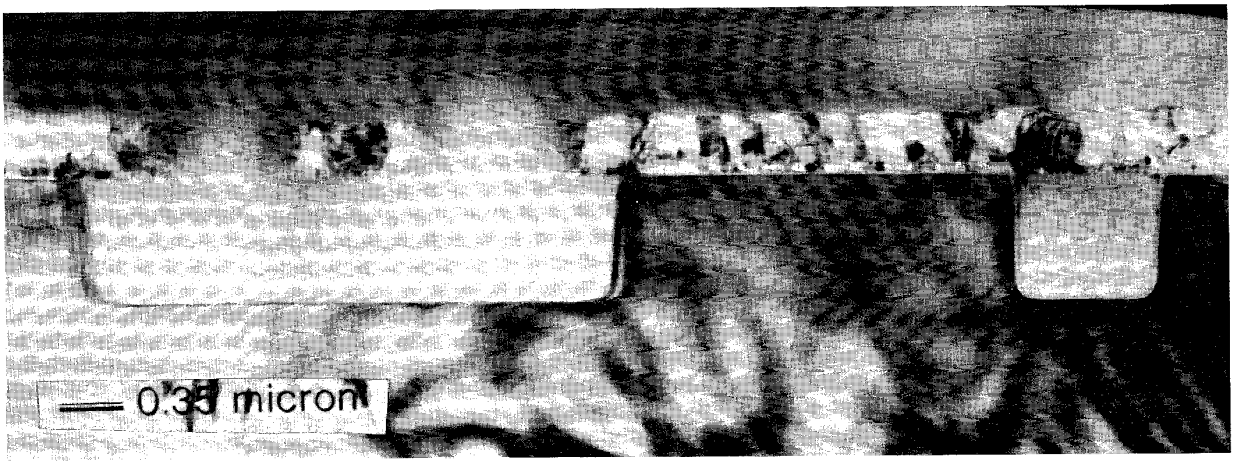


Fig. 10 TEM micrograph showing planar and defect free trench

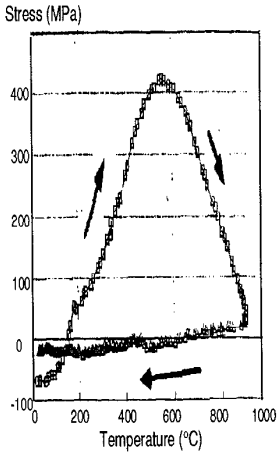


Fig. 11 In-situ Stress vs. Temp

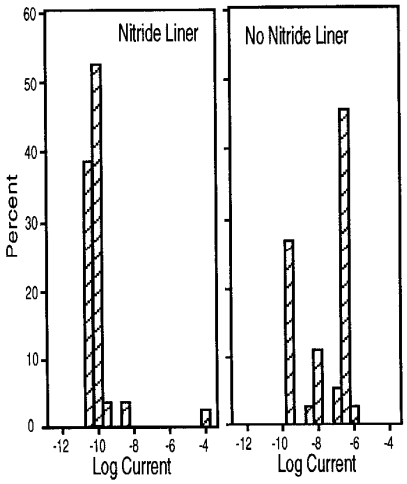


Fig. 12 N+ Junction Leakage (Perim.= 40 cm)

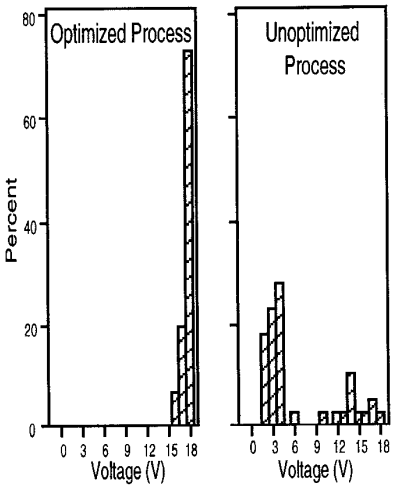


Fig. 13 Gate Oxide Breakdown (Perim. = 78 cm)