# United States Patent [19]

**Ma et al.**

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[54] **PROCESS FOR FABRICATING SELF-ALIGNED SILICIDE LIGHTLY DOPED DRAIN MOS DEVICES**


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[21] Appl. No.: **291,541**

[22] Filed: **Dec. 29, 1988**

**Related U.S. Application Data**

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[51] **Int. Cl.**[4] ..... **H01L 21/265**; H01L 21/44; H01L 21/48

[52] **U.S. Cl.** ..... **437/44**; 437/200; 437/202; 437/41; 437/931; 156/643; 156/653; 357/23.3; 148/DIG. 147; 148/DIG. 105

[58] **Field of Search** ..... 437/40, 41, 43, 44, 437/200, 196, 202, 931, 34, 56, 57; 357/23.3, 23.4, 23.9, 23.11; 156/643, 650, 651, 652, 653; 148/DIG. 131, DIG. 147, DIG. 105



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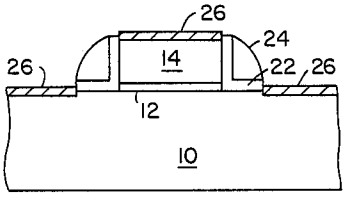
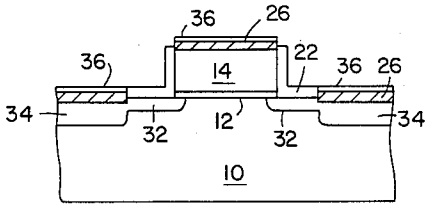
[57] **ABSTRACT**

In a method for fabricating an MOS structure, in accordance with one embodiment, a layer of material that serves as an etching stop during the side wall spacer etch, is inserted between the silicon substrate and the side wall spacer. In another embodiment of the invention, after establishing differential layer thicknesses on the source/drain surface, the side wall spacer is completely removed and light and heavy ion implantation steps are performed sequentially with one single lithographic step. In a further embodiment of the invention, after the self-aligned silicide is formed, the side wall spacer is removed, and light and heavy ion implantation steps are sequentially performed.


**12 Claims, 2 Drawing Sheets**



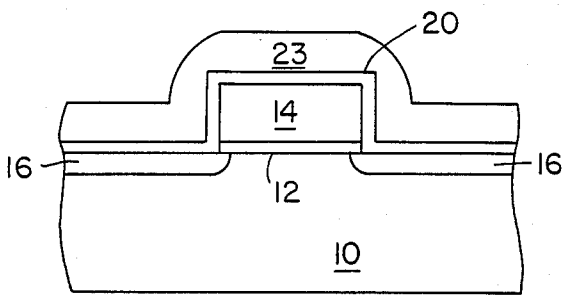



FIG. 1(a)

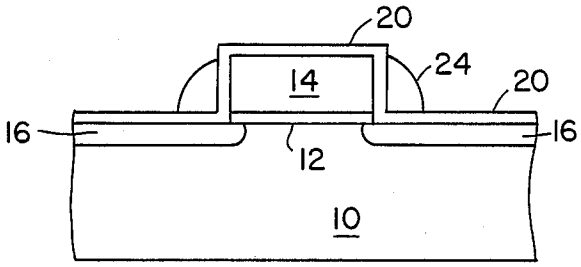



FIG. 1(b)

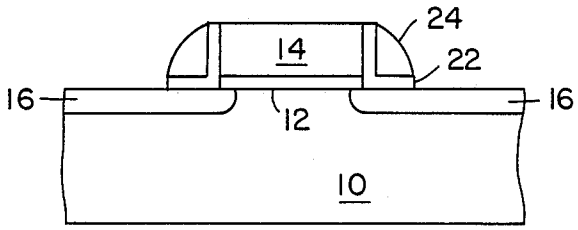



FIG. 1(c)

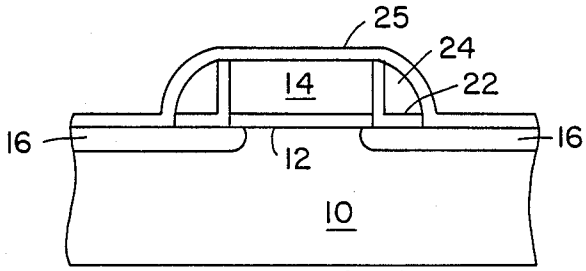



FIG. 1(d)

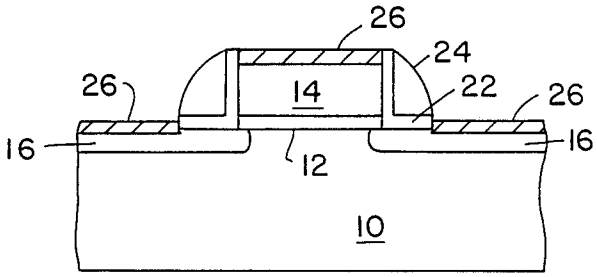



FIG. 1(e)

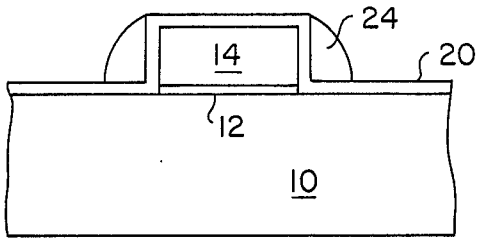



FIG. 2(a)

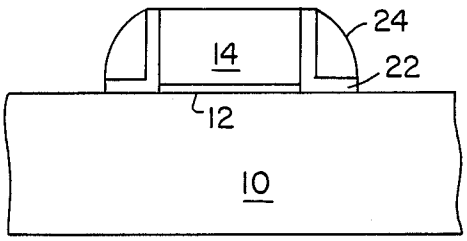



FIG. 3(a)

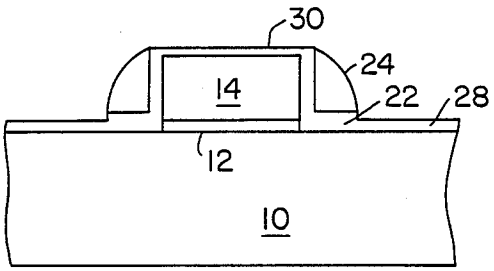



FIG. 2(b)

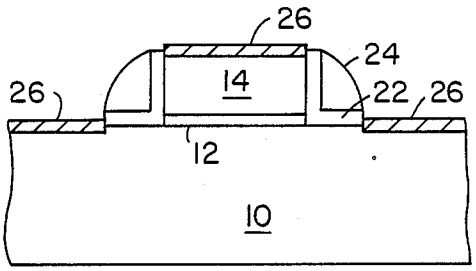



FIG. 3(b)

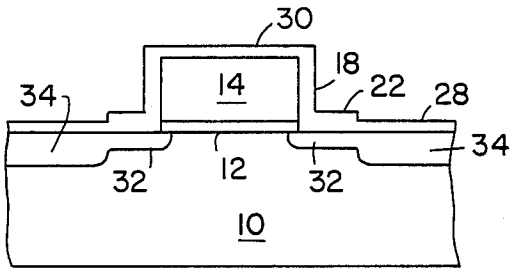



FIG. 2(c)

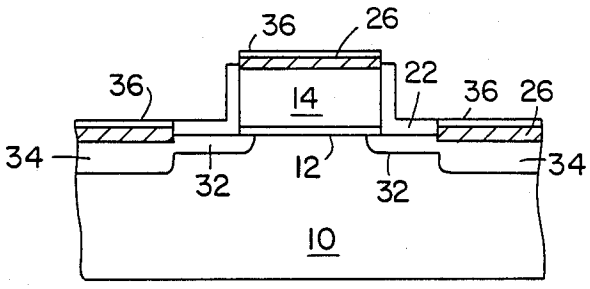



FIG. 3(c)

# PROCESS FOR FABRICATING SELF-ALIGNED SILICIDE LIGHTLY DOPED DRAIN MOS DEVICES

This is a divisional of Ser. No. 145,390, filed Jan. 19, 1988.

## BACKGROUND OF THE INVENTION

1. Field Of The Invention

This invention relates generally to the fabrication of metal-silicon dioxide semiconductor (MOS) devices, and more particularly to the fabrication of self-aligned silicide and lightly doped drain MOS device structures.

2. Description Of The Related Art

Recent developments in MOS fabrication techniques have produced MOS devices in which ever-decreasing device dimensions are realized in order to achieve greater device density and increased operating speeds. This decrease in MOS device dimensions has, however, created a concern over the high sheet resistance in the source/drain regions and hot carrier injection.

That is, as device dimensions continue to decrease, the junction depths of the source/drain regions are reduced so as to minimize parasitic effects. One direct result of this reduction in the source/drain junction depth is an increase of the sheet resistance of the source/drain regions. Another result of decreasing device dimensions bears on the junction integrity when a metal layer is applied to make a contact to the source/drain regions. The shallower the junction, the more difficult it is to reduce the leakage current of the source/drain regions to the substrate.

In order to reduce the sheet resistance of the source/-drain regions, a device structure has been developed, known as a self-aligned silicide structure, in which a metal silicide film is formed at the source/drain regions as well as at the polysilicon gate. In a conventional method for fabricating a self-aligned silicide structure, a silicon dioxide side wall spacer is formed before the source/drain and polysilicon regions are silicided. In this conventional process the side wall spacer etch has to clear the source/drain regions that are not intended to be covered by the side wall spacer so that these regions can be silicided. However, since the junctions are already formed, any significant etch into the silicon of the source/drain regions will reduce the junction depth. This is compounded by the fact that during the silicide formation, the top silicon layer of the source/drain regions is consumed by the silicide, thus further reducing the junction depth. As a result, in order to successfully fabricate a self-aligned silicide MOS device by the conventional fabrication process, all the silicon dioxide in the desired silicon region must be cleared without etching significantly into the junctions.

The performance of MOS integrated circuits is also enhanced by decreasing the separation between the source and drain of an MOS transistor, also known as the effective channel length. However, the applied drain-to-source voltage is kept at a constant level irrespective of reductions in channel length which results in a higher electric field being established across the channel region. This elevated electric field has the ability to inject the carriers (electrons or holes) in the channel region across the silicon and silicon dioxide interface and to trap the carriers in the oxide. Since the silicon dioxide layer forms the gate insulator of the MOS device, the trapped charges in the gate oxide have an effect on the electrical characteristics of the device. This is a particular concern from the reliability standpoint since the longer the drain-to-source voltage is applied, the more charges are trapped.

This phenomenon can be alleviated by using a lightly doped drain (LDD) structure in which a lightly doped region is inserted between the channel and the heavily doped source/drain regions. The lightly doped region has the effect of reducing the peak electric field in the channel region, thereby alleviating the hot carrier injection problem. One common way of implementing an LDD structure requires the formation of a side wall spacer, and hence is called a SWS-LDD (side wall spacer lightly doped drain) structure.

The construction of the SWS-LDD device requires the formation of a side wall spacer that is adjacent to the polysilicon gate. This side wall spacer is formed between two ion implantation steps; the first is a light implant, the second is a heavy implant to define the lightly and heavily doped regions, respectively. When the SWS-LDD structure is implemented in CMOS (complementary MOS) technology, two lithographic steps are required for each dopant polarity, one for each of the implants. For the non-LDD structure, only one such lithographic step is required since only one implant is needed.

As a result of the junction integrity problem described above, it has been proposed that the junctions be formed after silicidation, so that the impurities are implanted into or through the silicide. During the subsequent heat treatment, impurities in the silicide diffuse into the silicon to form the junctions. In addition, it is desirable to combine the self-aligned silicide feature with the LDD structure for advanced MOS device applications. When a self-aligned silicide is implemented with an SWS-LDD structure on a CMOS device, one additional lithographic step is required for each dopant polarity to fabricate the device.

In summary, the following three problems or disadvantages are recognized with regard to the fabrication of self-aligned silicide and lightly doped drain MOS structures:

(1) in the implementation of a self-aligned silicide structure, the side wall spacer etching has to be critically controlled;

(2) in the implementation of an SWS-LDD structure in CMOS, an additional lithographic step is required; and

(3) in the implementation of a self-aligned silicide LDD structure in which the junctions are formed after metal deposition or silicide formation, an additional lithographic step is required.

## SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved process for fabricating MOS devices having reduced dimensions in which one or more of the aforesaid problems are alleviated or eliminated.

It is also an object of the invention to provide a process for fabricating a self-aligned silicide MOS structure in which far greater processing latitude in side wall spacer etching is allowed.

It is another object of the invention to provide a process for fabricating a CMOS structure with a side wall spacer and lightly doped drain (SWS-LDD) features, which requires only one lithographic step for each source/drain dopant polarity.

It is a further object of the invention to provide a process for fabricating a CMOS self-aligned silicide lightly doped drain structure in which the silicide is formed or the metal is deposited which eventually forms silicide before the junction formation with one lithographic step for each source/drain dopant polarity.

In one embodiment of the invention, a layer of material is grown or deposited before the deposition of the side wall spacer material. The material of this layer has a different etching characteristic than that of the side wall spacer material and the silicon substrate. During the subsequent side wall spacer etch, this material serves as an etching stop. A second and different etch that has a substantially lower etch rate of the silicon substrate and side wall spacer material is then applied to remove the material in areas not covered by the side wall spacer.

In a second embodiment of the invention, a polysilicon gate is defined and a first layer is grown before the deposition of the side wall spacer material. The material of the first layer has a different etching characteristic than that of the silicon substrate and side wall spacer material. During the subsequent side wall spacer etch, this material serves as an etching stop. A second and different etch that has a substantially lower etch rate of the silicon substrate and side wall spacer material is then applied to remove the first layer of material in areas not covered by the side wall spacer. A second layer of material is grown over the exposed silicon substrate to a thickness whose ion implantation stopping power is less than that of the first layer. The side wall spacer is then removed, and two sequential ion implantations of the same polarity are performed after a lithographic step to define the regions that are to receive such implants. These two implants define, respectively, the lightly and heavily doped regions.

In a third embodiment of the invention, after a polysilicon gate is defined, a first layer of material is deposited before the deposition of the side wall spacer material. This first layer of material has a different etching characteristic than that of the silicon substrate and side wall spacer material. During the subsequent side wall spacer etch, this material serves as an etching stop. A second and different etch that has a substantially lower etch rate of the silicon substrate and side wall spacer material is applied to remove this material in the area not covered by the side wall spacer. Silicide is formed selectively over the silicon and polysilicon regions and the side wall spacer is etched away. For certain silicides that cannot withstand this etching environment, a layer of a second material may be selectively grown or deposited over the silicide but not on the side wall spacer. In addition, this second material has a different etching characteristic than that of the side wall spacer material. During the etching to remove the side wall spacer, this second material serves as an etching stop to protect the formed silicide layer. A lithographic step is performed to define the proper regions, and two sequential ion implants of the same dopant polarity are applied to form the lightly and heavily doped regions, respectively.

To the accomplishment of the above and such further objects as may hereinafter appear, the present invention relates to an improved process for fabricating MOS devices substantially as defined in the appended claims and as described in the following specification as considered with the accompanying drawings in which:

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(*a*)–1(*e*) are cross sections of a self-aligned silicide MOS device at various stages in its fabrication in accordance with a first embodiment of the invention;

FIGS. 2(*a*)–2(*c*) are cross sections of an SWS-LDD MOS device at various stages of its fabrication in accordance with a second embodiment of the invention; and

FIGS. 3(*a*)–3(*c*) are cross sections of a self-aligned silicide LDD MOS device at various stages of its fabrication in accordance with a third embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the figures, there is shown in FIG. 1(*a*) a self-aligned silicide MOS integrated circuit in an early stage of its fabrication in accordance with one embodiment of the invention. As therein shown, a silicon dioxide film **12** is grown over the upper surface of a silicon substrate **10**. As is per se conventional, a polysilicon gate **14** is defined over the film **12** and source/drain regions **16** are formed in the substrate **10** such as by diffusion or ion implantation. The silicon dioxide film **12** sandwiched between the substrate **10** and polysilicon gate **14** is to serve, in a known manner, as the gate insulation of the completed MOS device.

A layer of silicon dioxide **20** is then grown over the exposed surface of the substrate **10** and over the polysilicon gate **14**. Although in FIG. 1(*a*) only a conventional singly implanted/diffused junction is shown, the method of the invention can be applied as well to other types of junctions. The silicon dioxide layer **20** may be either thermally grown or deposited by a chemical vapor deposition (CVD) method. The thickness of the silicon dioxide layer **20** is such that it does not consume too much polysilicon and the silicon substrate if it is thermally grown, but thick enough to be a good etch stop for the subsequent side wall spacer etch. If the silicon dioxide layer **20** is deposited by a CVD method, there is no concern for polysilicon and silicon consumption. A thickness of the silicon dioxide layer **20** between 150 A and 2000 A is sufficient for this purpose.

A layer of silicon nitride **23** is subsequently deposited by a CVD method, which later in the process forms the side wall spacer. The thickness of the silicon nitride layer **23** is determined by the desired width of the side wall spacer, which also depends on other factors such as the angle of the polysilicon side wall profile and the thickness of polysilicon. A thickness of silicon nitride layer **23** of 1000A or greater is needed for practical applications.

Subsequent to the silicon nitride deposition, as shown in FIG. 1(*b*), a directional silicon nitride etch is performed to form the silicon nitride side wall spacer **24**. This is done preferably in a plasma etcher or in a reactive ion etcher. The etching process should have a sufficiently high silicon nitride etch rate and a sufficiently low oxide etch rate (good silicon nitride-to-silicon dioxide selectivity). The etch should stop when the silicon nitride in the planar surface is completely removed.

Such an etch could be accomplished in a planar plasma etcher with a two-step etch technique. The first step has the following conditions: pressure: 325 mtorr; power: 175 watt; with a gas flow of 10 sccm of argon and 60 sccm of sulfur hexafluoride ($SF_6$) The second step consists of: pressure: 325 mtorr; power: 100 watt;

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