Trials@uspto.gov
571-272-7822

Paper 52
Entered: April 19, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
and GLOBALFOUNDRIES U.S. INC.,
Petitioners,

v.

GODO KAISHA IP BRIDGE 1,
Patent Owner.

Case IPR2016-01246[1]
Patent 7,126,174 B2

Before JUSTIN T. ARBES, MICHAEL J. FITZPATRICK, and JENNIFER MEYER CHAGNON, *Administrative Patent Judges*.

ARBES, *Administrative Patent Judge*.

DECISION
Patent Owner's Request for Rehearing
37 C.F.R. § 42.71

[1] Case IPR2016-01247 has been consolidated with this proceeding.

Patent Owner filed a Request for Rehearing (Paper 50, "Req. Reh'g") of our Final Decision (Paper 49, "Dec." or "Decision") determining that Petitioner[2] had shown, by a preponderance of the evidence, that claims 1–12 and 14–18 of U.S. Patent No. 7,126,174 B2 (Ex. 1001, "the '174 patent") are unpatentable. For the reasons stated below, Patent Owner's Request for Rehearing is *denied*.

"A party dissatisfied with a decision may file a single request for rehearing without prior authorization from the Board." 37 C.F.R. § 42.71(d). "The burden of showing a decision should be modified lies with the party challenging the decision." *Id.* "The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply." *Id.*

After reviewing the arguments and evidence submitted by both parties in this proceeding, we determined that Petitioner had met its burden to show unpatentability of the challenged claims under 35 U.S.C. § 103(a) by a preponderance of the evidence. Patent Owner argues that, in doing so, we "misapplied the law of obviousness in the field of semiconductor fabrication and relied extensively upon the unreliable testimony" of Petitioner's declarant, Sanjay Kumar Banerjee, Ph.D. Req. Reh'g 1.

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[2] On June 9, 2017, we granted motions for joinder filed by GlobalFoundries U.S. Inc. ("GlobalFoundries") in Cases IPR2017-00925 and IPR2017-00926, and authorized GlobalFoundries to participate in this proceeding only on a limited basis. *See* Paper 20; IPR2017-00925, Paper 13; IPR2017-00926, Paper 12. Although the papers referenced herein were filed by Taiwan Semiconductor Manufacturing Company, Ltd., we refer to both entities as "Petitioner" throughout this Decision.

First, with respect to our application of the law of obviousness, Patent Owner argues that we "mistakenly overlook[ed] that neither the Petition nor Dr. Banerjee ever said 'how' the reference processes were to be combined to arrive at a workable claimed invention." *Id.* at 2, 9–10 (similarly arguing that Petitioner failed to "explain what the final combined structure would look like"), 14 (similarly arguing that Petitioner failed to "evaluate the workability of the proposed processes"). According to Patent Owner, such an explanation was necessary due to the complexity of semiconductor fabrication technology, and we overlooked evidence in the record of such complexity, "misapprehended the law of obviousness by failing to take technological complexity into account," and incorrectly found that a person of ordinary skill in the art would have been able to combine the references' teachings in the manner asserted by Petitioner. *Id.* at 2–6 (citing Exs. 2012–19, 1025 (shown in Ex. 1060, cited by Patent Owner)). Patent Owner also points to another Board decision, cited after the oral hearing in this proceeding, *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, Case IPR2016-00394 (PTAB June 23, 2017) (Paper 64) ("*Samsung*"), in support of its position. Req. Reh'g 3–4 & n.2; *see* Ex. 2080.

We are not persuaded that we misapprehended or overlooked any of the parties' arguments or supporting evidence regarding the asserted combinations of references.[3] As explained in the Decision, Petitioner relied

[3] Petitioner asserted four obviousness combinations in this proceeding: (1) Lee and Noble, (2) Lee and Ogawa, (3) Lowrey and Noble, and (4) Lowrey and Ogawa. Dec. 6–7. Many of Patent Owner's arguments in the Request for Rehearing assert error in our Decision generally, rather than referring to a particular combination. For those arguments, we refer to the

on Lee for all of the limitations of claim 1 except a "trench isolation," and relied on Noble for that limitation. Dec. 13–16, 28, 37. Specifically, Petitioner argued that an ordinarily skilled artisan would have been motivated to substitute Noble's isolation structure (shallow trench isolation (STI) 30) in place of Lee's isolation structure (field oxide 113, formed using Local Oxidation of Silicon (LOCOS)). *Id.* Thus, contrary to Patent Owner's arguments, Petitioner explained "how" (and why) a person of ordinary skill in the art would have combined the teachings of the references to achieve the semiconductor device recited in claim 1. *See id.* at 13–16, 21–26, 28.

What allegedly was missing from Petitioner's analysis in the Petition, according to Patent Owner, was a recitation of the particular sequence of steps by which a device based on the combined teachings of Lee and Noble would have been made. *See* Req. Reh'g 2; Paper 14, 1–5, 14. Upon review of the parties' arguments, we were not persuaded that such an explanation was necessary in the Petition, given the particular factual circumstances of this case. Dec. 21–29. Among other things, claim 1 is an apparatus claim; it is not a method claim for fabricating a semiconductor device and does not require any particular process for forming the recited components, including the "trench isolation." *Id.* at 28–29. Petitioner also provided considerable evidence showing that (1) LOCOS and trench isolation were well-known isolation structures and recognized in the industry as interchangeable, functionally equivalent substitutes for each other, (2) trench isolation had various advantages such that it would have been considered an improvement over LOCOS, and (3) it would have been well within the skill level of a

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Lee-Noble combination for convenience, but our analysis applies equally to the other grounds.

person of ordinary skill in the art to make a semiconductor device using either isolation technique. *Id.* at 21–28; *see* Ex. 1001, col. 1, l. 29–col. 2, l. 6, col. 3, l. 53–col. 4, l. 19, Figs. 17, 20(e) (the '174 patent describing "conventional" semiconductor devices of the time with a trench isolation and stating that manufacturers had begun moving from LOCOS to trench isolation); *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) ("For the technique's use to be obvious, the skilled artisan need only be able to recognize, based on her background knowledge, its potential to improve the device and be able to apply the technique."); *In re Mouttet*, 686 F.3d 1322, 1333 (Fed. Cir. 2012) ("[T]he test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art.").

Regardless, though, we evaluated Patent Owner's arguments regarding the fabrication processes of the cited references to determine whether the processes are "so different or incompatible that they would have discouraged a person of ordinary skill in the art from making the asserted combination or would not have produced a reasonable expectation of success in achieving the claimed device." Dec. 29–38. We were persuaded that an ordinarily skilled artisan would have been able to form an STI instead of a LOCOS isolation in Lee, using Lee's order of steps (i.e., forming an isolation structure before forming the gate stack components), for the reasons explained in the Decision.[4] *Id.*

[4] Many of Patent Owner's arguments were premised on bodily incorporating Noble's STI and surrounding components into Lee's device, which is not required to demonstrate obviousness. *See* Dec. 29–33, 35 n.13. Patent Owner does not address this aspect of the Decision in its Request for Rehearing.

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