

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2016-01246<sup>1</sup>  
Patent 7,126,174 B2

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**PETITIONER'S OBJECTIONS TO PATENT OWNER'S EVIDENCE  
SUBMITTED IN THE PATENT OWNER'S RESPONSE**

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<sup>1</sup> Case IPR2016-01247 has been consolidated with this proceeding.

In accordance with 37 C.F.R. § 42.64(b)(1), Petitioner Taiwan Semiconductor Manufacturing Company, Ltd. submits the following list of objections to Patent Owner IP Bridge's Exhibits 2004, 2012 through 2019, 2021, 2026 through 2030, 2032, and 2033 to the Patent Owner's Response:

<b>Exhibit Number</b>	<b>Description</b>
2004	Photograph of a Chemical Mechanical Polishing Tool from the Applied Materials Company. BusinessWire.com. Accessed October 5, 2016. <a href="http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion">http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion</a>
2012	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Response filed in IPR2016-01246 on March 24, 2017.
2013	Thompson, L. F. "An Introduction to Lithography." <i>Introduction to Microlithography</i> , ACS Symposium Ser., American Chemical Society, pp. 1–13 (1983).
2014	CA1275846 C to Roland et al.
2015	U.S. Patent No. 5,314,843 to Yu et al.
2016	U.S. Patent No. 5,231,306 to Meikle et al.
2017	U.S. Patent No. 4,529,621 to Ballard.
2018	U.S. Patent No. 5,310,624 to Ehrlich.
2019	U.S. Patent No. 5,097,422 to Corbin, II et al.
2021	U.S. Patent No. 4,952,524 to Lee et al.

Exhibit Number	Description
2026	“Structural Analysis Sample Report” downloaded from <a href="https://www.chipworks.com/TOC/Structural_Analysis_Sample_Report.pdf">https://www.chipworks.com/TOC/Structural_Analysis_Sample_Report.pdf</a> (2008).
2027	U.S. Patent No. 4,776,922 to Bhattacharyya et al.
2028	Subbanna, S.; Ganin, E.; Crabbé, E.; Comfort, J.; Wu, S.; Agnello, P.; Martin, B.; McCord, M.; Newman, H. Ng. T.; McFarland, P.; Sun, J.; Snare, J.; Acovic, A.; Ray, A.; Gehres, R.; Schulz, R.; Greco, S.; Beyer, K.; Liebmann, L.; DellaGuardia, R.; Lamberti, A. “200 mm Process Integration for a 0.15 $\mu\text{m}$ Channel-Length CMOS Technology Using Mixed X-Ray / Optical Lithography.” <i>Proceedings of 1994 IEEE International Electron Devices Meeting</i> , pp. 695–698 (1994).
2029	Chung, J.; Jeng, M.-C.; Moon, J.E.; Wu, A.T.; Chan, T.Y.; Ko, P.K.; Hu, Chenming. “Deep-Submicrometer MOS Device Fabrication Using a Photoresist-Ashing Technique.” <i>IEEE Electron Device Letters</i> , Vol. 9, No. 4, pp. 186–188 (1988).
2030	Tanaka, Tetsu; Suzuki, Kunihiro; Horie, Hiroshi; Sugii, Toshihiro. “Ultrafast Low-Power Operation of p <sup>+</sup> -n <sup>+</sup> Double-Gate SOI MOSFETS.” 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 11–12 (1994).
2032	Kaufman, F. B.; Thompson, D. B.; Broadie, R. E.; Jaso, M. A.; Guthrie, W. L.; Pearson, D. J.; and Small, M. B. “Chemical-Mechanical Polishing for Fabricating Patterned W Metal Features as Chip Interconnects.” <i>Journal of The Electrochemical Society</i> , Vol. 138, No. 11, pp. 3460–3465 (1991).
2033	Landis, H.; Burke, P.; Cote, W.; Hill, W.; Hoffman, C.; Kaanta, C.; Koburger, C.; Lange, W.; Leach, M.; and Luce, S. “Integration of chemical-mechanical polishing into CMOS integrated circuit manufacturing.” <i>Thin Solid Films</i> , Vol. 220, No. 1–2, pp. 1–7 (1992).

**I. Objection to Paragraphs 4–10 and 35–458 of Patent Owner’s Exhibit 2012—Unreliable “Expert” Testimony**

Petitioner objects to Exhibit 2012 because it contains unreliable testimony under Fed. R. Evid. 702 and *Daubert v. Merrell Dow Pharm., Inc.*, 509 U.S. 579 (1993). Dr. Schubert’s declaration includes numerous opinions on matters for which Dr. Schubert has failed to establish himself as an expert. Dr. Schubert has not established himself as someone possessing sufficient knowledge, skill, experience, training, and/or education regarding LDD (lightly doped drain) MOSFETs. *See* Ex. 2012, ¶¶ 13–23, App’x A. Although Dr. Schubert may have experience with III-V compound semiconductors and light-emitting devices,<sup>2</sup> such devices are vastly different from the LDD Si MOSFET devices at issue in these proceedings.

Dr. Schubert does not claim to have significant experience designing or making LDD Si MOSFET devices.<sup>3</sup> Nevertheless, Dr. Schubert repeatedly opines

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<sup>2</sup> *See, e.g.*, Ex. 2012 at ¶¶ 14–17; <https://www.rpi.edu/dept/cfes/researchers/Fred%20Schubert.html> (last visited Mar. 29, 2017).

<sup>3</sup> Although MOSFETS may be included in some of the subject matter of courses taught by Dr. Schubert, he provides no evidence regarding the type of information taught relative to MOSFETs, the depth of its treatment, or why mere

about the understanding of a person of ordinary skill in the art during the relevant period with respect to LDD Si MOSFET devices.

**II. Objection to Patent Owner’s Exhibits 2004, 2026, 2029, 2030, 2032, and 2033—Failure to Authenticate**

Patent Owner fails to provide evidence to authenticate Exhibits 2004, 2026, 2029, 2030, 2032, and 2033, making them inadmissible under Fed. R. Evid. 901.

**III. Objection to Patent Owner’s Exhibit 2021—Incomplete Document**

Patent Owner’s Exhibit 2021 appears to be an incomplete document, missing at least three pages, in violation of Fed. R. Evid. 106.

**IV. Objection to Patent Owner’s Exhibits 2004, 2013–2019, 2026–2030, 2032, and 2033—Irrelevant and Non-Probative Evidence**

Patent Owner’s Exhibits 2004, 2013–2019, 2026–2030, 2032, and 2033 are irrelevant to any material facts at issue in these proceedings, and any probative value Patent Owner may try to assign them is substantially outweighed by their tendency to confuse the issues, mislead the Board, waste time, and needlessly present cumulative evidence. These exhibits are therefore inadmissible under Fed. R. Evid. 401, 402, and 403.

Citations to Exhibits 2004, 2032, and 2033 appear only in footnotes to paragraph 68 of Dr. Schubert’s declaration (Exhibit 2012 ) and page 102 of Patent

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inclusion of MOSFETs in a course establishes him as an expert relative to the design and fabrication of LDD MOSFETs (or even one of ordinary skill in the art).

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