Ultrafast Low-Power Operation of p^+-n^+ Double-Gate SOI MOSFETs

Tetsu Tanaka, Kunihiro Suzuki, Hiroshi Horie, and Toshihiro Sugii
Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

1. Introduction

Double-gate SOI MOSFETs don't suffer from the short-channel effects that limit the scaling of bulk MOSFETs because two gate electrodes jointly control the carriers. The excellent short-channel behavior and high transconductance has been studied theoretically and experimentally [1-4].

As the MOSFET technology is extended into the sub-quarter-micron range and the supply voltage is scaled to 1-2 V, it needs to lower the threshold voltage (Vth) less than 0.3 V to obtain enough drain current. However, the Vth of conventional double-gate SOI nMOSFETs is -0.1 V with n^+-n^+ poly Si gate electrodes, and 1 V with p^+-p^+ poly Si gate electrodes. The values are not appropriate for such short gate lengths. In this paper, we proposed p^+ poly Si for the front-gate electrode and n^+ poly Si for the back-gate electrode in order to optimize the Vth, resulting in small subthreshold current and large drain current. A record ring oscillator gate delay of 27 ps at 2 V for Lg = 0.19 μm was obtained.

2. Vth Control

Figure 1 shows the cross-sectional view of this device. Assuming full-depletion of the Si layer and charge conservation at Si-SiO2 interfaces, we found that the nMOS threshold voltage, Vth_{pn}, with these gate electrodes is :

$$Vth_{pn} = Vth_{pp} - \frac{3T_{ox} + T_{Si}}{6T_{ox} + T_{Si}} (Vth_{pp} - Vth_{nn}),$$

where T_{si} is the silicon thickness, T_{ox} is the gate oxide thickness, Vth_{pp} is the Vth of p^+-p^+ poly Si gate devices, and Vth_{nn} is the Vth of n^+-n^+ poly Si gate devices. Vth_{pp} and Vth_{nn} are 0.98 V and -0.12 V, respectively [5]. The pMOS Vth is the same magnitude as the nMOS Vth but the opposite polarity because of the symmetrical structure. We plotted the dependence of Vth_{pn} on the aspect ratio of silicon thickness to gate oxide (Fig. 2). The Vth_{pn} is less than 0.3 V for the aspect ratio more than 2. The experimental Vth with the aspect ratio of 5 were 0.17 V for nMOS and -0.24 V for pMOS, which were almost the same as those expected from our theory.

3. Process Technology

Figure 3 shows a SEM cross section of nMOS device. A detailed process integration is given in [3]. The key process were as follows ; we used direct bonded SOI wafers thinned to 40 nm by chemical-mechanical polishing (CMP). The n- and pMOS gate conductivity types were the same, so the poly Si gate doping didn't require a mask process. To minimize the series resistance, we used W silicide for the back-gate and Co salicide for the front-gate, source and drain [6]. The resultant sheet resistance of 6-9 Ω/sq. was achieved.

4. Results and Discussion

Figure 4 shows the threshold rolloff. The Vth is less than 0.3 V. Both the thin silicon films and the use of two gate electrodes suppress short-channel effects for gate length below 0.2 μm. Figure 5 shows the I-V characteristics of 0.19-μm Lg MOSFETs. We used the front-gate poly Si length as the gate length for all the devices. We obtained very large drain currents and steep subthreshold slope for n- and pMOS with front-gate oxide 8.2 nm thick and back-gate oxide 9.9 nm thick. The subthreshold slope was about 69 mV/decade for nMOS and 70 mV/decade for pMOS because of two gate electrodes. We extracted capacitance values of equivalent circuit parameters for the nMOS device from S-parameter measurements (Table 1). The reference bulk MOSFET had a gate 0.15 μm long and a gate oxide 4 nm thick [6]. The drain-source capacitance, Cds, is remarkably small, which is about 10% of the reference value, because of thick buried oxide under the drain. The gate-drain capacitance, Cgd, is larger than the reference value due to the overlap capacitance between back-gate and drain. Using these devices, we fabricated an unload inverter ring oscillator. We examined the dependence of the delay time on the supply voltage and the power dissipation normalized to 1 GHz clock-frequency (Figs. 6,7). For Lg = 0.19 μm, we obtained an inverter delay time of 43 ps at 1 V, and 27 ps at 2 V. These are, to our knowledge, the fastest reported values for this gate length despite the thick gate oxides. The p^+-n^+ double-gate SOI MOSFETs operate with a faster switching speed especially at low supply voltage and lower power consumption at the same switching speed. This is because low Vth and steep subthreshold slope lead large drain currents at low supply voltage and because the Cds doesn't increase at low supply voltage unlike the bulk MOSFET.

5. Summary

Using direct bonded SOI wafers just 40 nm thick, we fabricated p^+-n^+ double-gate SOI MOSFETs. These devices, with an appropriate Vth, have good short-channel behavior and a large drive current. For Lg = 0.19 μm, we obtained an inverter delay time of 43 ps at 1 V, and 27 ps at 2 V. These are the fastest reported values for this gate length. The high performance is attributed to the large drain current, the low series resistance, and the reduction of the parasitic drain junction capacitance.

Acknowledgments

The authors are thankful to members of device fabrication group in our laboratory. The authors are also thankful to Drs. Arimoto, Hijiya, and Ito for their encouragement.

References

1. T. Sekigawa, et al., Solid-St. Electron. 27, p. 827 (1984).
2. H. Horie, et al., SSDM Tech. Dig., p. 165 (1991).
3. T. Tanaka, et al., IEDM Tech. Dig., p.683 (1991).
4. J. P. Colinge, et al., IEDM Tech. Dig., p595 (1990).
5. K. Suzuki, et al., Solid-St. Electron. (in print).
6. T. Yamazaki, et al., IEDM Tech. Dig., p906 (1993).

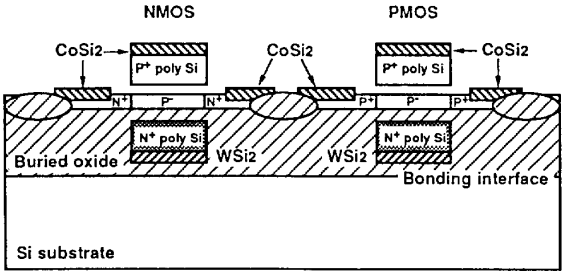

Figure 1 Cross section of CMOS devices

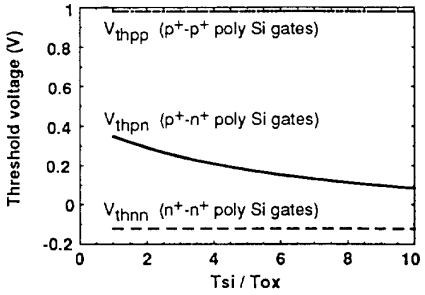

Figure 2 Dependence of Vth on aspect ratio

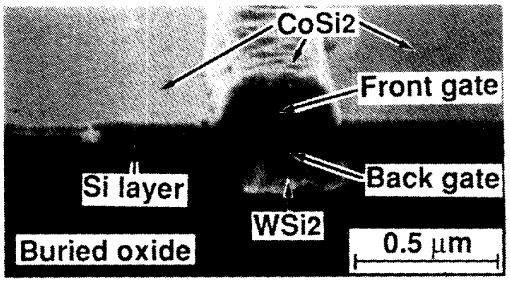

Figure 3 SEM image

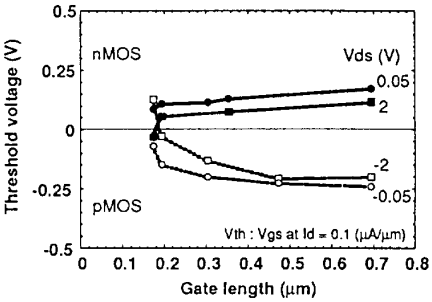

Figure 4 Vth rolloff

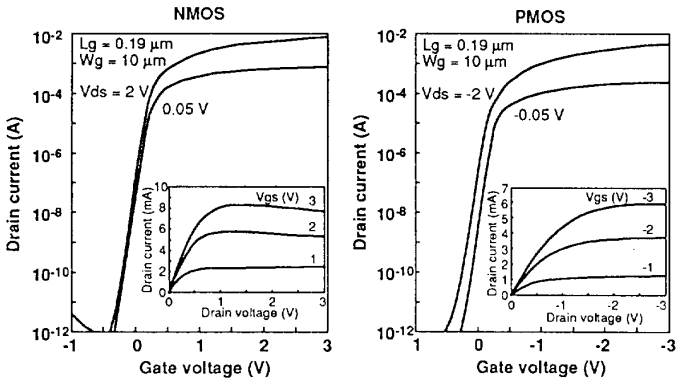

Figure 5 I-V characteristics of devices with T_{si} = 40 nm, T_{ox} (front) = 8.2 nm, and T_{ox} (back) = 9.9 nm.

Table 1

	DG-SOI	Bulk MOS*
Cds	0.40 fF	3.75 fF
Cgd	1.98 fF	1.40 fF
Cgs	4.59 fF	6.11 fF

Device width is 5 µm. * Reference [6]

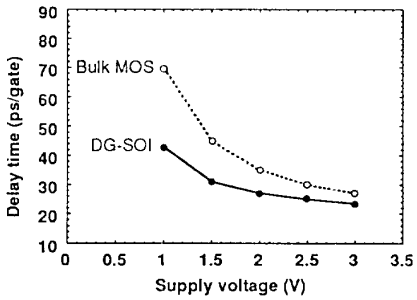

Figure 6 Dependence of delay time on supply voltage

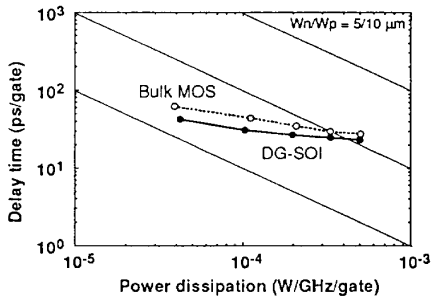

Figure 7 Dependence of delay time on power dissipation