Deep-Submicrometer MOS Device Fabrication Using a Photoresist-Ashing Technique

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Abstract—**A photoresist-ashing process has been developed which, when used in conjunction with conventional g-line optical lithography, permits the controlled definition of deep-submicrometer features. The ultra-fine lines were obtained by calibrated ashing of the lithographically defined features in oxygen plasma. The technique has been successfully employed to fabricate MOSFET's with effective channel length as small as 0.15 μm that show excellent characteristics. An NMOS ring oscillator with 0.2-μm devices has been fabricated with a room-temperature propagation delay of 22 ps/stage which is believed to be the fastest value obtained for a MOS technology. Studies indicate that the thinning is both reproducible and uniform so that it should be usable in circuit as well as device fabrication. Since most polymer-based resist materials are etchable with an oxygen plasma, the basic technique could be extended to supplement other lithographic processes, including e-beam and X-ray processes, for fabricating both silicon and nonsilicon devices and circuits.**

I. Introduction

BECAUSE of the resolution limit of optical lithography, e-beam and X-ray lithography have been the principal means used to fabricate deep-submicrometer devices including MOSFET's [1]–[3]. However, both techniques are complicated and expensive. In addition, both techniques require exposing the device to varying doses of high-energy radiation creating potential reliability problems.

In this paper, a photoresist-ashing process is presented which, when used in conjunction with conventional g-line ($\lambda = 436$ nm) optical lithography, permits the controlled definition of deep-submicrometer features. The technique has been successfully employed to fabricate MOSFET's with effective channel length as small as 0.15 μm that show excellent overall characteristics. Results of evaluation studies indicate that the ashing is both reproducible and uniform so that it should be usable in circuit as well as device fabrication.

II. Fabrication Process

Polysilicon-gate NMOS transistors were fabricated as a demonstration of this technique. The starting substrates were 4-in-diameter, 15–30 Ω·cm, p-type silicon wafers. Each wafer was given a boron field implant of 2.25×10^{12} cm^{-2} at 70 keV. The active regions were then defined using local oxidation of silicon (LOCOS). A field oxide of 0.25 μm was grown in steam at 950°C. Depending upon the gate oxide thickness, a boron threshold/punchthrough implant at 30 keV with varying dose from 1.0×10^{12} to 1.6×10^{13} cm^{-2} was performed. Gate oxides of 3.6, 5.6, 7.5, and 8.6 nm were then grown at 800°C in dry oxygen. Gate oxide of 15.6 nm was grown at 900°C in dry oxygen. All gate oxides were annealed in nitrogen at their oxidation temperature for 20 min. *In-situ* doped n^+-polysilicon (0.25 μm) was then immediately deposited by LPCVD. Up to this point, the process was similar to a standard NMOS process.

Gates with drawn lengths from 0.7 to 1.5 μm were initially defined using conventional lithographic methods. Kodak Micro Positive Resist 820, a positive photoresist, was spun on to a thickness of 1.0 μm and soft-baked for 1 min at 100°C. All exposures were performed using a g-line 10× wafer stepper. In order to obtain optimal after-ashing line shape and step coverage for the submicrometer gates, it was necessary to reduce the exposure 10–20 percent from the exposure required for defining gates longer than 1 μm. After exposure, the wafers were developed and given a final hard bake of 15 min at 120°C before ashing.

A low-frequency (30 kHz) plasma etching system was then used to ash the patterned photoresist. Optimal controllability and uniformity of the ashing process was observed for an oxygen pressure of 300 mtorr and an RF power of 50 W. To define the gates, the polysilicon was then anisotropically etched in CCl_4 plasma.

Self-aligned arsenic source/drain implants of 3.0×10^{15} cm^{-2} at 50 keV were then performed. Subsequent thermal cycles were less than 60 min at 900°C in order to reduce implant diffusion and the junction depth.

III. Experimental Results

The ashing process was observed to be controllable and reproducible. Fig. 1 displays a plot of the SEM-measured gate length versus ashing time for four different drawn MOSFET gate lengths. A lateral ashing rate of about 0.068 μm/min is observed. This rate appears to be relatively independent of the ashing time, the initial drawn length, and the original photoresist shape. The linear ash rate appears constant down to at least 0.2 μm. Narrower lines can be created, but only with a lesser degree of control. The difference between the drawn lengths and the measured lengths before ashing is due to the reduced exposure mentioned above. The polysilicon gate width was also determined from the changing resistances of

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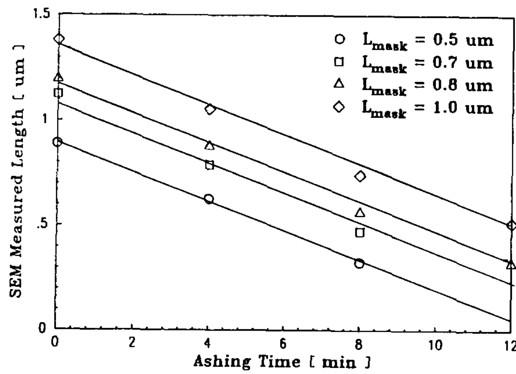

Fig. 1. SEM measured channel length versus ashing time for four different initial mask channel lengths. The net lateral ashing rate is approximately 680 Å/min.

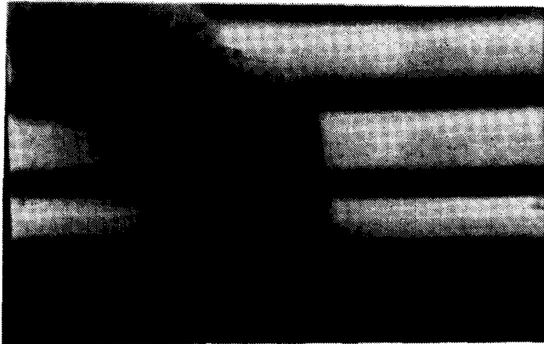

Fig. 2. SEM photograph of the step coverage of a photoresist-covered polysilicon gate after 8 min of ashing. The polysilicon line is 0.5 μm wide. The profile of the photoresist is preserved after ashing.

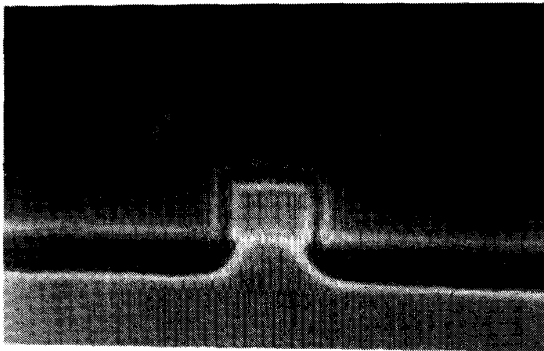

Fig. 3. SEM photograph of a transistor cross section with $L_{\rm eff}$ = 0.22 μm. The junction depth is 0.2 μm. Ashing time is 8 min, and ΔL due to the ashing is approximately 0.5 μm.

polysilicon resistors with varying amounts of ashing time. Good agreement between electrical and SEM results was observed. Fig. 2 presents an SEM picture of a photoresist-covered polysilicon line after 8 min of ashing. Excellent line shape and step coverage is observed. No change in the photoresist profile was observed during the ashing procedure.

This ashing procedure was incorporated into a deep-submicrometer process. Fig. 3 displays an SEM picture of transistor cross sections with an $L_{\rm eff}$ of 0.22 μm. The ashing time was 8 min with a corresponding length reduction of

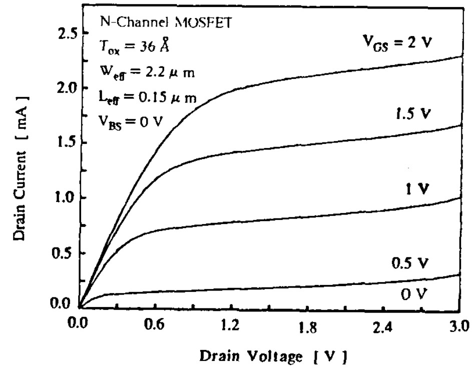

Fig. 4. Characteristic of a deep-submicrometer MOSFET fabricated with the photoresist-thinning technique.

Fig. 5. Waveform of a 101-stage enhancement/depletion ring oscillator consisting of 0.2-μm MOSFET's with 75-nm gate oxide at a power supply voltage of 3 V. The output signal is 75 mV peak to peak (20 mV/div).

approximately 0.5 μm. The estimated junction depth is 0.2 μm. The difference between the measured junction depth and the lateral diffusion distance under the gate edge reflects a nonequality between the vertical and lateral arsenic diffusion rates. From C–V profiling measurements and computer simulations, the channel doping was estimated to be 2–8 $\times$ 10^{17} cm^{-3} depending upon the threshold/punchthrough implant.

No process controllability problems were introduced by the ashing procedure. Using data obtained from the capacitance technique [4], the effective channel length $L_{\rm eff}$ was compared with the drawn gate length $L_{\rm mask}$. The amount of length reduction ($\Delta L = L_{\rm mask} - L_{\rm eff}$) was found to be independent of $L_{\rm mask}$. Statistical measurements were performed on wafer lots with varying amounts of ashing time. No significant variability in channel length was introduced by the ashing process within a particular lot. Any channel length variations observed were found to be within the tolerances of the lithographic system used.

Fig. 4 shows the characteristics for a transistor with an oxide thickness of 3.6 nm and an effective channel length of 0.15 μm. The measured transconductance of this device is over 630 mS/mm at room temperature. Excellent performance and punchthrough control are observed, and no gate-diffusion nonoverlap problems were found [5].

Fig. 5 displays the waveform of a 101-stage enhancement/

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depletion ring oscillator with an L_{eff} of 0.2 μm and a 7.5-nm gate oxide. A room-temperature gate delay of 22 ps is observed at a power supply voltage of 3 V. This delay is believed to be the fastest value reported for a silicon MOS technology.

IV. Conclusions

A photoresist-ashing process has been developed which allows the relatively simple fabrication of deep-submicrometer MOSFET's using only g-line lithography. This process appears to be controllable and easily adaptable to most existing technologies. Although this technique does not inherently improve circuit density, by increasing the gain and driving capability of the MOSFET, the potential of improving digital and analog circuit speed is significant. Since most polymer-based resist materials are ashable with an oxygen plasma, the basic technique could be extendible to supplement other lithographic processes, including e-beam and X-ray processes, for fabricating both silicon and nonsilicon devices and circuits.

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