Structural Analysis

Sample Report

Overview and Layout Analysis – Excerpt from 45 nm Process Technology
Process Analysis – Excerpt from 45 nm Process Technology
SRAM Analysis – Excerpt from SOI 45 nm Process Technology
Materials Analysis – Excerpt from SOI 45 nm Process Technology
Critical Dimensions – Excerpt from 90 nm Process Technology

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Table of Contents

1 Overview
- 1.1 List of Figures
- 1.2 List of Tables
- 1.3 Introduction
- 1.4 Device Summary
- 1.5 Process Summary

2 Device Overview
- 2.1 Package and Die
- 2.2 Die Features
- 2.3 Die Utilization
- 2.4 Selected Layout Features

3 Process Analysis
- 3.1 General Structure
- 3.2 Dielectrics
- 3.3 Metallization
- 3.4 Vias and Contacts
- 3.5 Logic MOS Transistors
- 3.6 Isolation
- 3.7 Wells and Substrate

4 High Density (HD) 6T SRAM Analysis
- 4.1 HD 6T SRAM Schematic and Layout Analysis
- 4.2 HD 6T SRAM Cross-Section Analysis

5 Materials Analysis
- 5.1 TEM-EDS Analysis of BEOL Dielectrics
- 5.2 TEM-EDS Analysis of MIM Capacitor
- 5.3 TEM-EDS Analysis of BEOL Metallization and Contacts
- 5.4 TEM-EDS Analysis of Transistors, SOI, and BOX

6 Critical Dimensions
- 6.1 Horizontal Dimensions
- 6.2 Vertical Dimensions

7 Statement of Measurement Uncertainty and Scope Variation

About Chipworks

1 Overview

1.1 List of Figures

2 Device Overview
2.1.1 Package on PCB
2.1.2 Package Top
2.1.3 Package Bottom
2.1.4 Package X-Ray
2.1.5 Die Photograph
2.1.6 Die Markings
2.1.7 Analysis Sites
2.2.1 Die Corner A
2.2.2 Die Corner B
2.2.3 Die Corner C
2.2.4 Die Corner D
2.2.5 Detail of Die Corner A
2.2.6 Detail of Die Corner B
2.2.7 Detail of Die Corner C
2.2.8 Detail of Die Corner D
2.2.9 Bond Pads
2.3.1 Die Functional Blocks
2.3.2 Area 1
2.3.3 Area 2
2.3.4 Area 3
2.3.5 Area 4
2.4.1 Standard Logic at Metal 1
2.4.2 Detail of Standard Logic Cells at Metal 1
2.4.3 Overview of Standard Logic at Poly
2.4.4 Standard Logic at Poly – Wide Gates
2.4.5 Standard Logic – Standard Cell Size and Dummy Poly

3 Process Analysis
3.1.1 General Structure
3.1.2 Die Thickness
3.1.3 Die Edge Seal
3.2.1 Dielectric Stack Overview
3.2.2 Passivation and ILD 8
3.2.3 ILD 6 and ILD 7
3.2.4 ILD 7 – TEM
3.2.5 ILD 3, ILD 4, and ILD 5
3.2.6 TEM of ILD 5 – TEM
3.2.7 ILD 4 – TEM
3.2.8 ILD 3 – TEM
3.2.9 ILD 2 – TEM
3.2.10 ILD 1 – TEM

3.2.11 PMD Overview
3.2.12 PMD – TEM
3.2.13 TEM-EDS Spectrum of Passivation
3.2.14 TEM-EDS Spectra of ILD 7-4 and ILD 7-5
3.2.15 TEM-EDS Spectra of ILD 7-1 through ILD 7-3
3.2.16 TEM-EDS Spectra of ILD 5
3.2.17 TEM-EDS Spectra of ILD 1
3.2.18 TEM-EDS Spectra of PMD
3.3.1 Minimum Pitch Metal 9
3.3.2 Metal 9
3.3.3 Metal 9 Barrier – TEM
3.3.4 Minimum Pitch Metal 8
3.3.5 Metal 8 Liner – TEM
3.3.6 Minimum Pitch Metal 6
3.3.7 Metal 6 Liner – TEM
3.3.8 Minimum Pitch Metal 3 and 5
3.3.9 Metal 3 Liner – TEM
3.3.10 Minimum Pitch Metal 2 and 4
3.3.11 Metal 2 Liner – TEM
3.3.12 Minimum Pitch Metal 1
3.3.13 Metal 1 Liner
3.3.14 TEM-EDS Spectrum of Metal 9 Body
3.3.15 TEM-EDS Spectra of Metal 9 Barrier Layers
3.3.16 TEM-EDS Spectrum of Metal 1 Barrier
3.4.1 Minimum Pitch Via 8s
3.4.2 Minimum Pitch Via 7s
3.4.3 Minimum Pitch Via 6s
3.4.4 Minimum Pitch Via 5s
3.4.5 Via 5 – TEM
3.4.6 Minimum Pitch Via 3s and 4s
3.4.7 Via 4 – TEM
3.4.8 Minimum Pitch Via 1s and 2s
3.4.9 Via 2s – TEM
3.4.10 Minimum Pitch Contacts – TEM
3.4.11 Contact to Poly – TEM
3.4.12 Top of Contact – TEM
3.4.13 Bottom of Contact – TEM
3.4.14 TEM-EDS Spectrum of Contact Liner
3.4.15 TEM-EDS Spectrum of Contact Silicide
3.5.1 Minimum Contacted Gate Pitch
3.5.2 NMOS Transistors – Si Etch
3.5.3 PMOS Transistors – Si Etch
3.5.4 Minimum Gate Length MOS Transistor
3.5.5 Minimum Gate Length MOS Transistor – TEM

3.5.6 Gate Dielectric – TEM
3.5.7 Wide and Narrow Gate Length Transistors – TEM
3.5.8 Gate Dielectric Overview – TEM
3.5.9 Poly Thickness – TEM
3.5.10 Poly Gate Wrap – TEM
3.5.11 TEM-EDS Spectrum of Gate Silicide
3.6.1 Minimum Width STI – TEM
3.6.2 STI Thickness – TEM
3.6.3 STI Beneath Poly – TEM
3.7.1 SCM of Wells and Substrate
3.7.2 SCM of N-Well
3.7.3 SCM of Embedded P-Well
3.7.4 TEM Diffraction Pattern – Si Channel Region
3.7.5 TEM-EDS Spectrum of Si Substrate

4 High Density (HD) 6T SRAM Analysis
4.1.1 HD 6T SRAM Schematic
4.1.2 HD 6T SRAM at Metal 3
4.1.3 HD 6T SRAM at Via 2s
4.1.4 HD 6T SRAM at Metal 2
4.1.5 HD 6T SRAM at Via 1s
4.1.6 HD 6T SRAM at Metal 1
4.1.7 HD 6T SRAM at Poly
4.1.8 HD 6T SRAM at Active Silicon
4.2.1 TEM Overview of NMOS Access and Pull-Down Transistors
4.2.2 TEM of NMOS Transistor (T2 or T6)
4.2.3 TEM Overview of PMOS Pull-Up Transistor
4.2.4 TEM of PMOS Pull-Up Transistor
4.2.5 TEM of SRAM Transistor Gate Dielectric

5 Materials Analysis
5.1.1 TEM-EDS Spectrum of ILD 10-3
5.1.2 TEM-EDS Spectrum of ILD 9-2 (ILD 10-2)
5.1.3 TEM-EDS Spectrum of ILD 9-3
5.1.4 TEM-EDS Spectrum of ILD 8-1 (ILD 9-1, ILD 10-1)
5.1.5 TEM-EDS Spectrum of ILD 8-5
5.1.6 TEM-EDS Spectrum of ILD 8-4
5.1.7 TEM-EDS Spectrum of ILD 8-2, ILD 8-3
5.1.8 TEM-EDS Spectrum of ILD 4-2 (ILD 5-2, ILD 6-2, ILD 7-2)
5.1.9 TEM-EDS Spectrum of ILD 4-1 (ILD 5-1, ILD 6-1, ILD 7-1)
5.1.10 TEM-EDS Spectrum of ILD 1-2 (ILD 2-2, ILD 3-2)
5.1.11 TEM-EDS Spectrum of ILD 1-1 (ILD 1-2, ILD 1-3)
5.1.12 TEM-EDS Spectrum of PMD 3
5.1.13 TEM-EDS Spectrum of PMD 1/PMD 2

5.2.1 TEM-EDS Spectrum of Capacitor Hard Mask
5.2.2 TEM-EDS Spectrum of Capacitor Plates
5.2.3 TEM-EDS Spectrum of MIM Capacitor Dielectric
5.2.4 TEM-EDS Spectrum of Pre-capacitor Dielectric
5.3.1 TEM-EDS Spectrum of UBM
5.3.2 TEM-EDS Spectrum of Metal 11 Body
5.3.3 TEM-EDS Spectrum of Metal 11 Ta-based Barrier
5.3.4 TEM-EDS Spectrum of Metal 11 Ti-based Barrier
5.3.5 TEM-EDS Spectrum of Metal 10 Body
5.3.6 TEM-EDS Spectrum of Metal 1 Liner
5.3.7 TEM-EDS Spectrum of Contact Liner
5.4.1 TEM-EDS Spectrum of Gate Silicide
5.4.2 TEM-EDS Spectrum of Diffusion Silicide
5.4.3 TEM-EDS Spectrum of NMOS Stress Liner
5.4.4 TEM-EDS Spectrum of PMOS Stress Liner
5.4.5 TEM-EDS Spectrum of PMOS eSiGe
5.4.6 TEM-EDS Spectrum of SOI (Channel Region)
5.4.7 TEM-EDS Spectrum of BOX

1.2 List of Tables

1 Overview
1.3.1 Device Identification
1.4.1 Device Summary
1.5.1 Process Summary

2 Device Overview
2.1.1 Package and Die Dimensions
2.3.1 Die Utilization

3 Process Analysis
3.2.1 Measured Dielectric Thicknesses
3.3.1 Metallization – Vertical Dimensions
3.3.2 Metallization – Horizontal Dimensions
3.4.1 Via and Contact Horizontal Dimensions
3.5.1 MOS Transistor Horizontal Dimensions
3.5.2 MOS Transistor Vertical Dimensions
3.6.1 Observed Isolation Dimensions
3.7.1 Die Thickness and Well Depths

4 High Density (HD) 6T SRAM Analysis
4.2.1 6T SRAM Transistor Sizes

6 Critical Dimensions
6.1.1 Minimum Pitch Metals
6.1.2 Contacts and Vias
6.1.3 Transistors, Poly, and Isolation
6.2.1 Vertical Dimensions

1.3 Introduction

This report is a structural analysis of the 45 nm XXXX extracted from the XXXX Blu Ray DVD recorder. The part uses multi decoding technology, which is capable of simultaneously processing two screens of full-HD, and MPEG-4 AVC/H.264 encoding technology. This technology compresses a full-HD image into 1/2 to 1/3 its original size, compared with conventional technology.

XXXX developed their 45 nm process in their fab in conjunction with XXXX. The process is reported to use 193 nm immersion lithography, stress-induced, mobility-enhanced transistors, low-k dielectrics, and design-for-manufacturability (DFM) techniques.

The XXXX is fabricated using a nine metal 45 nm CMOS process, featuring 32 nm minimum gate length MOS transistors. The part features “intermediate-k” dielectrics for the upper level dielectrics, and true low-k dielectrics for the lower level dielectrics. While XXXX has reported the use of strain engineering, we do not see (through reverse engineering techniques) any mechanism for applying strain. It is possible that the thin (~0.01 µm) oxynitride contact etch stop layer (CESL) is used to apply tensile strain for NMOS. This is, however, much thinner than the silicon nitride we have seen used for applying tensile strain on other devices (at the 65 nm node). It is possible that now, with such a small gate length, XXXX is able to apply strain with such a thin film.

XXXX has migrated to using rotated wafers for the 45 nm node. The transistors on the XXXX are oriented with their channels in the <100> direction, as opposed to the more conventional <110> orientation. This technique increases the drive current of the PMOS transistors.

Five different sizes of 6T SRAM are used, the smallest having a unit cell size of 0.34 μm^2. The 6T SRAM uses a uni-directional poly layout, with butted contacts used to reduce the cell size. 8T SRAM is used with a 0.63 μm^2 unit cell size. The part also uses ROM memory.

To date (January 2008), Chipworks has analyzed just one other die fabricated using a 45 nm process, the XXXX die.

This report contains the following detailed information:

- Package photographs, package x-ray, die markings, and die features
- Die utilization analysis, including an annotated gate level die photograph and functional block measurements
- SEM and transmission electron microscopy (TEM) analysis of the dielectrics, metals, vias and contacts, transistors, isolation and major structural features, and measurement of the horizontal and vertical critical dimensions of the die
- TEM-EDS analysis of the dielectrics, metals, and transistors
- Scanning capacitance microscopy (SCM) analysis of the wells and substrate
- Embedded memory analysis, including bevel images of the 6T SRAM and block layout images of the various memory arrays

All the information was derived by Chipworks from two samples with the following markings:

Package markings	XXXX
Die markings	XXXX
Date code	XXXX

Table 1.3.1 Device Identification

1.4 Device Summary

Manufacturer	XXXX
Foundry	XXXX
Part number	XXXX
Type	System LSI
Date code	740 (week 40 of 2007)
Package markings	XXXX
Package type	BGA
Die markings	XXXX
Die size (die edge seal)	8.42 mm x 8.14 mm (65.5 mm^2)
Process type	CMOS
Number of metal layers	9
Number of poly layers	1
Minimum transistor gate length	32 nm
Process generation	45 nm
Feature measured to determine process generation	Transistor gate lengths, metal 1 pitch, SRAM cell size

Table 1.4.1 Device Summary

1.5 Process Summary

Passivation	Single layer of silicon nitride
Dielectrics	ILD 8 uses oxide and oxynitride films ILD 6 and ILD 7 use oxide/FSG line dielectrics, SiON metal etch stop, oxide via dielectric, SiON Cu sealant ILD 5 uses FSG line dielectric, oxide via dielectric, SiCNO Cu sealant ILD 1 through ILD 4 use SiOC low-k line, via dielectrics, and SiCNO Cu sealant PMD uses SiOC line dielectric, oxide contact dielectric and SiON contact etch stop layer (CESL)
Metallization	Top level Al uses TiN/Ti barrier Metal 2 through metal 8 are dual damascene Cu with Ta-based liners Metal 1 is single damascene Cu with a Ta-based liner
Vias and contacts	Via 8s are Al filled Via 1s through via 7s are Cu filled Contacts are W with TiN liner
Polysilicon	Single level of Ni silicide polysilicon
Transistor	36 nm minimum gate length Ni silicided transistor gates and diffusions (no Pt doping) Transistors oriented with their channels in the <100> direction Possible use of nitride strain for NMOS transistors
Isolation	0.10 µm minimum width shallow trench isolation (STI)
Wells	Twin-wells in a P-epi
Substrate	P-type substrate Wafer rotated to provide <100> transistor channel orientation
Embedded memory	Five different sizes of 6T SRAM used Smallest 6T SRAM has a unit cell size of 0.37 µm x 0.93 µm (0.34 μm^2) 8T SRAM used with a 0.63 μm^2 unit cell size. ROM used with a unit cell size of 0.20 µm x 0.26 µm (0.05 μm^2)
Process generation	45 nm

Table 1.5.1 Process Summary

2 Device Overview

2.1 Package and Die

The XXXX used for this analysis was removed from a XXXX Blu Ray DVD Recorder. Figure 2.1.1 shows the part as mounted on the printed circuit board (PCB).

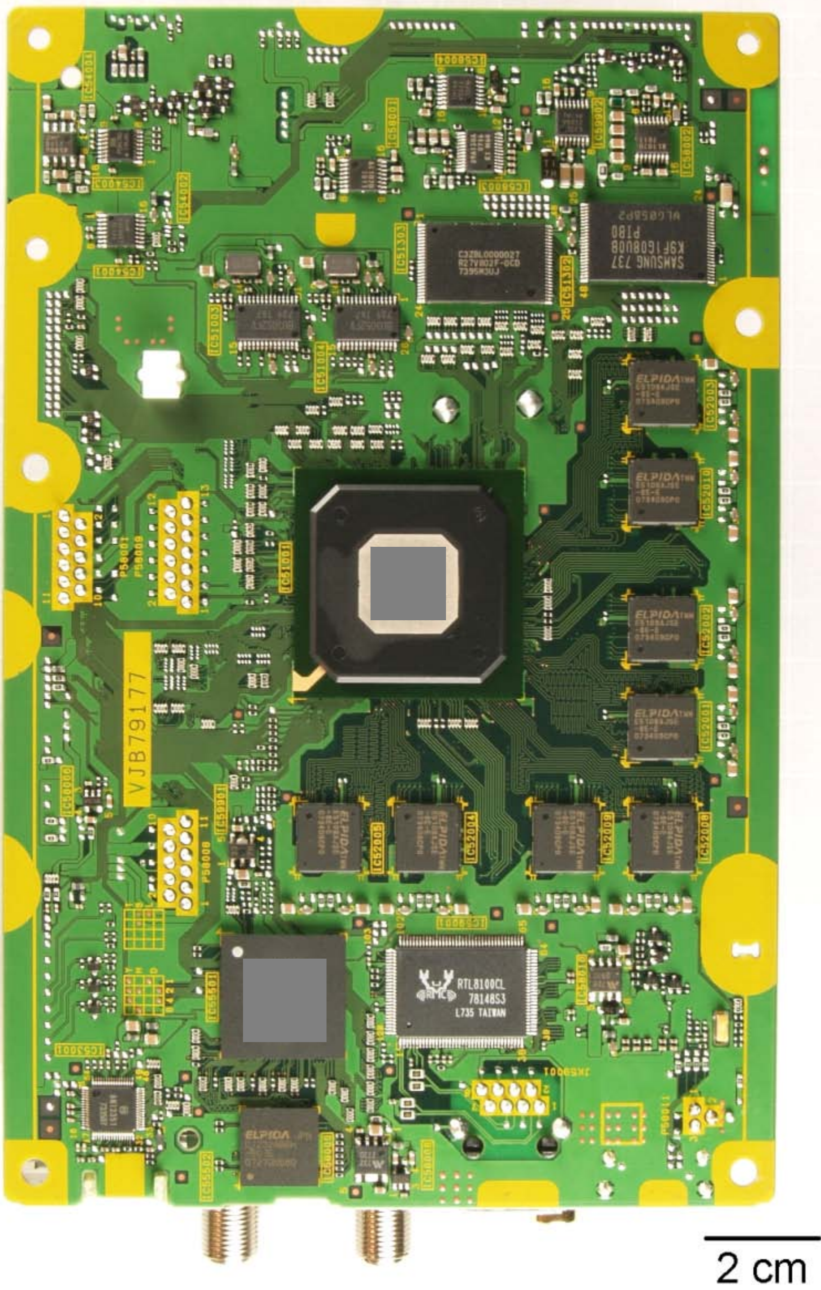

Figure 2.1.1 Package on PCB

Top and bottom photographs of the XXXX package are shown in Figure 2.1.2 and Figure 2.1.3, respectively. The package markings include:

XXXX

The XXXX was sold under XXXX consumer electronics XXXX brand.

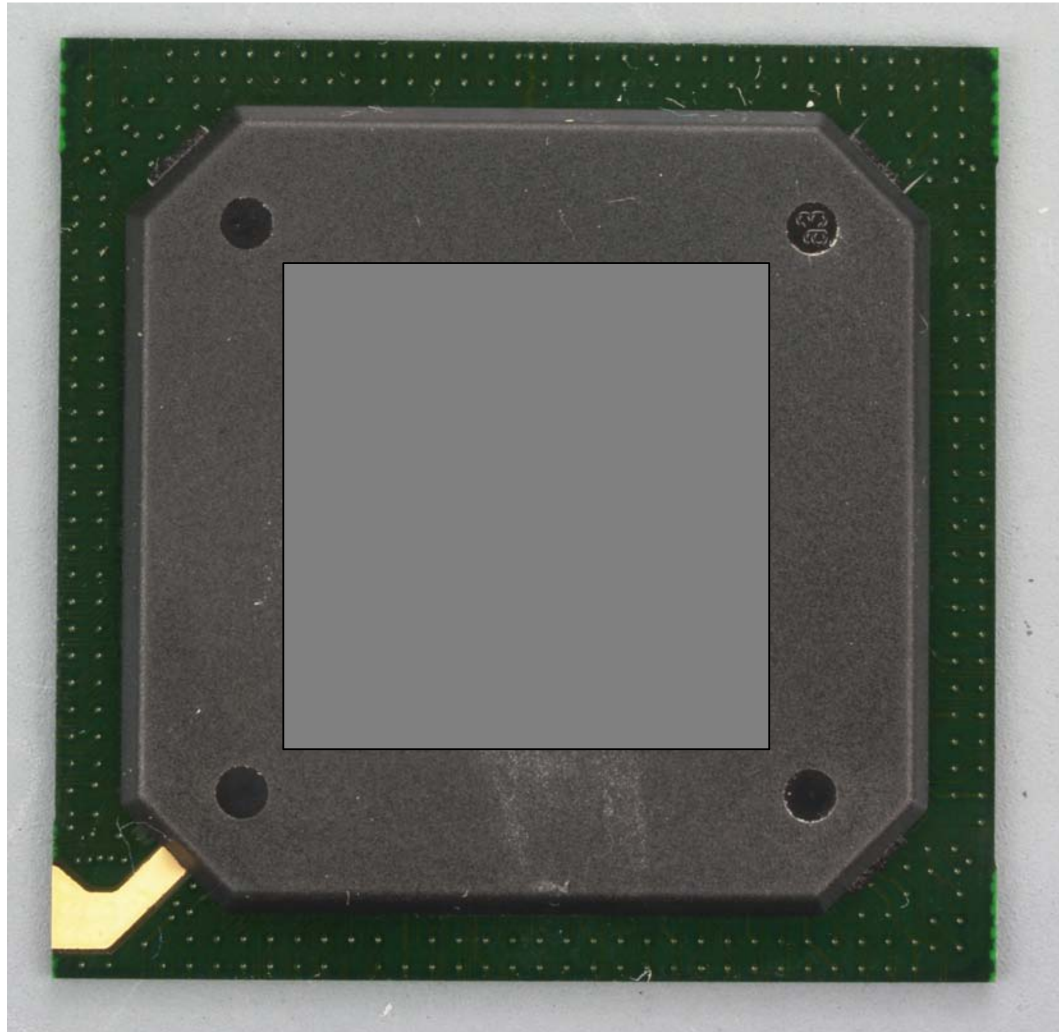

Figure 2.1.2 Package Top

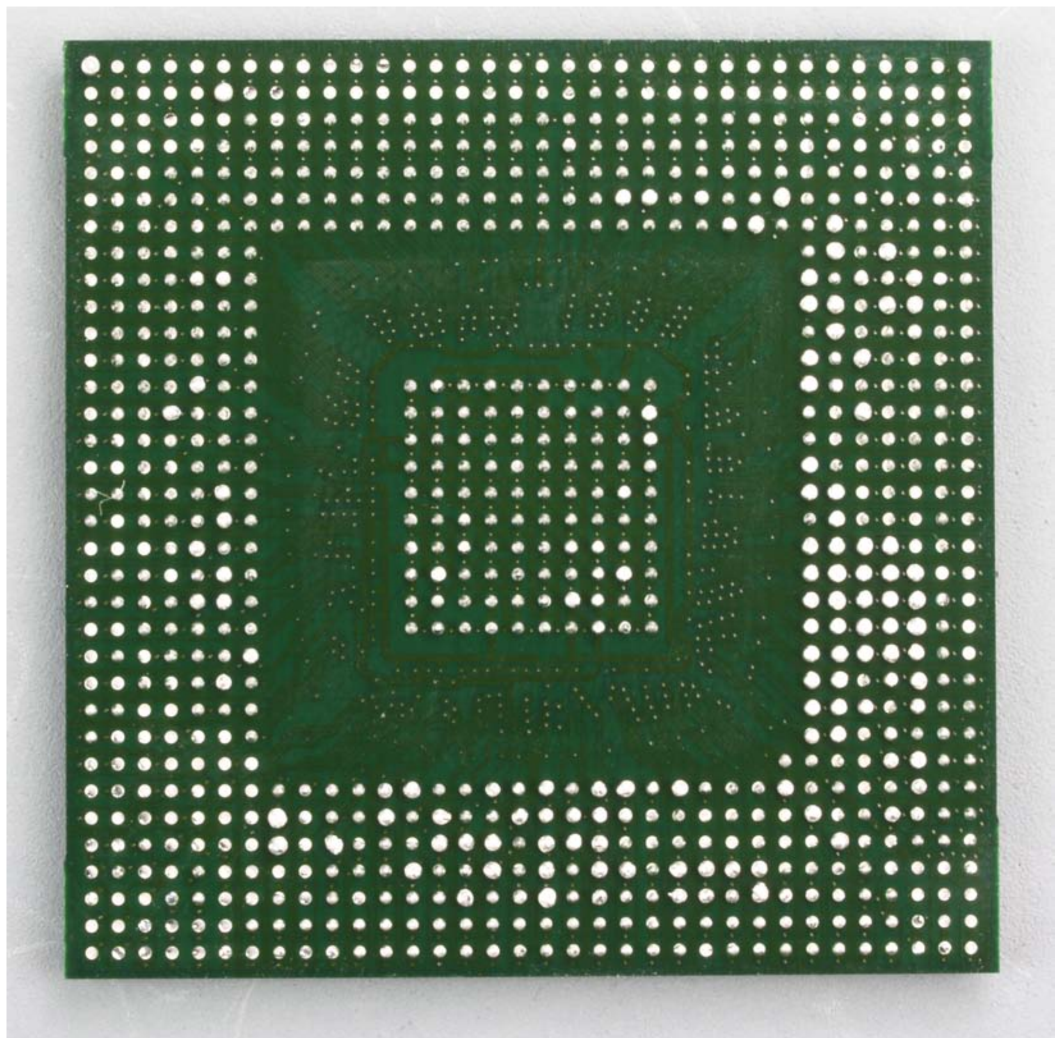

Figure 2.1.3 Package Bottom

A plan-view x-ray photograph of the XXXX is shown in Figure 2.1.4. Conventional wire bonding is used to connect the die to the package lands.

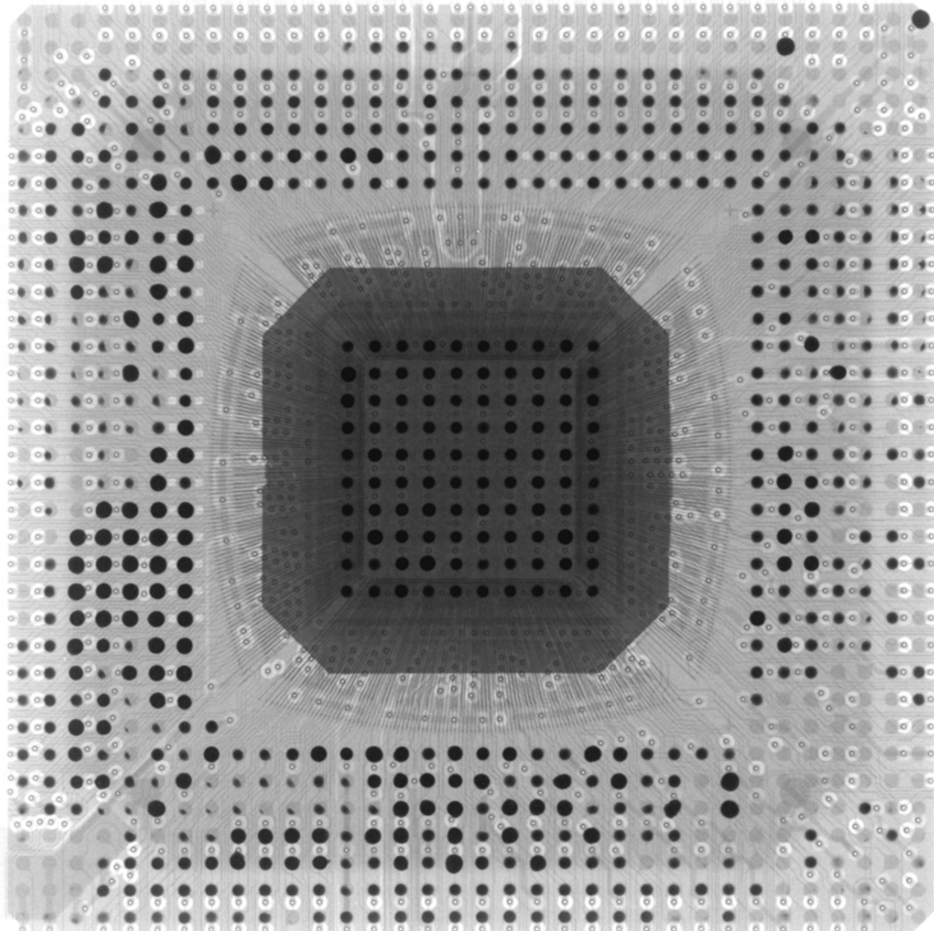

Figure 2.1.4 Package X-Ray

Figure 2.1.5 shows a photograph of the decapsulated XXXX die extracted from the XXXX. The die measures 8.42 mm x 8.14 mm from the die seals, or 8.45 mm x 8.17 mm for the whole die. The die area is 65.5 mm^2 (die seals). A double row of bond pads is visible around the periphery of the die. The die is 300 µm thick.

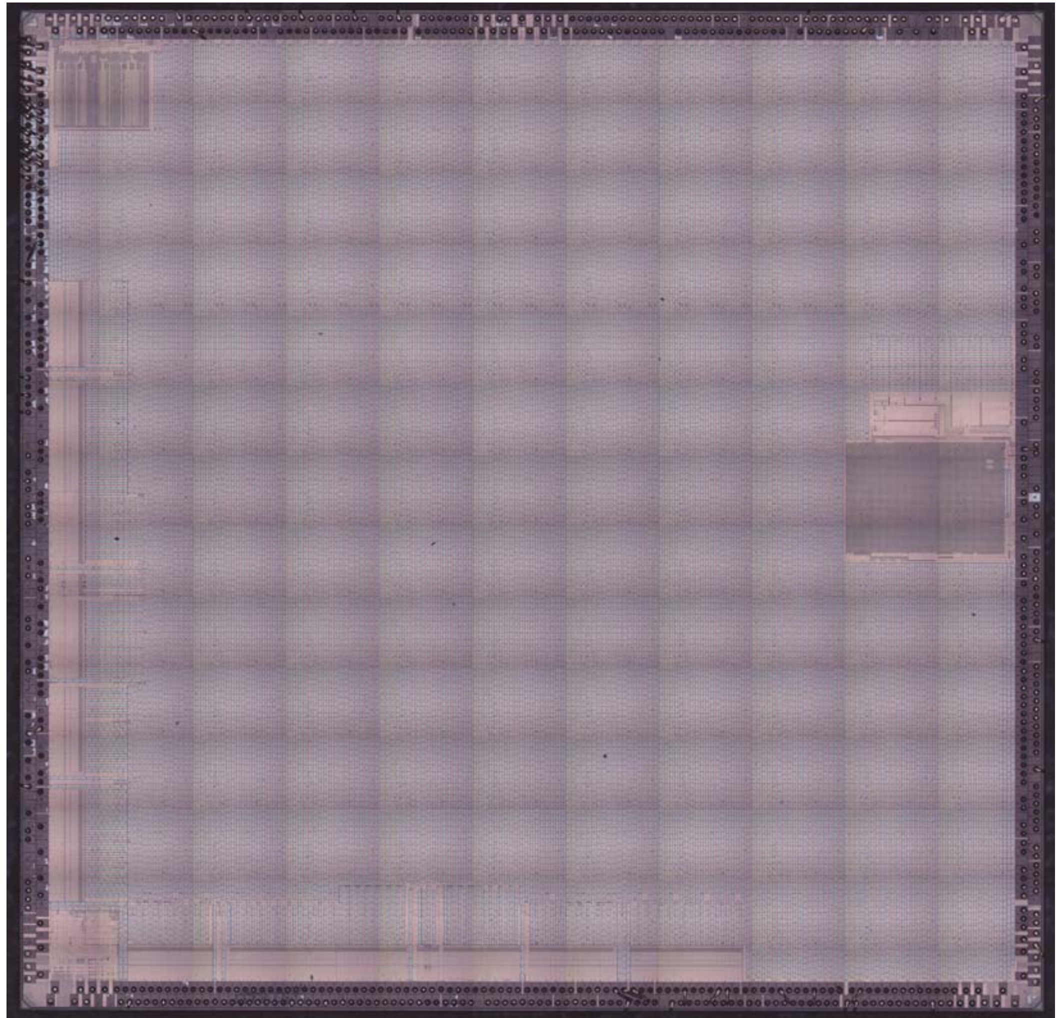

Figure 2.1.5 Die Photograph

The 2WS0038 die markings are shown in Figure 2.1.6.

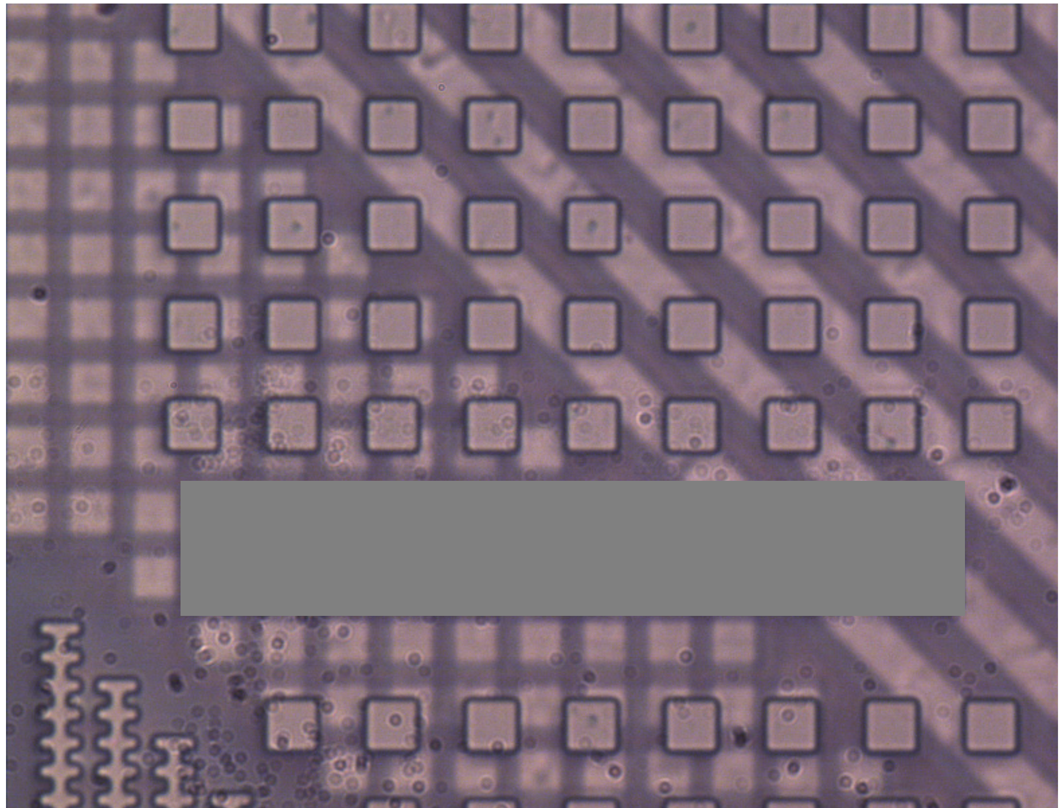

Figure 2.1.6 Die Markings

Figure 2.1.7 is a die photograph annotated to show the regions of the die analyzed by SEM, SCM, TEM, and bevel analysis.

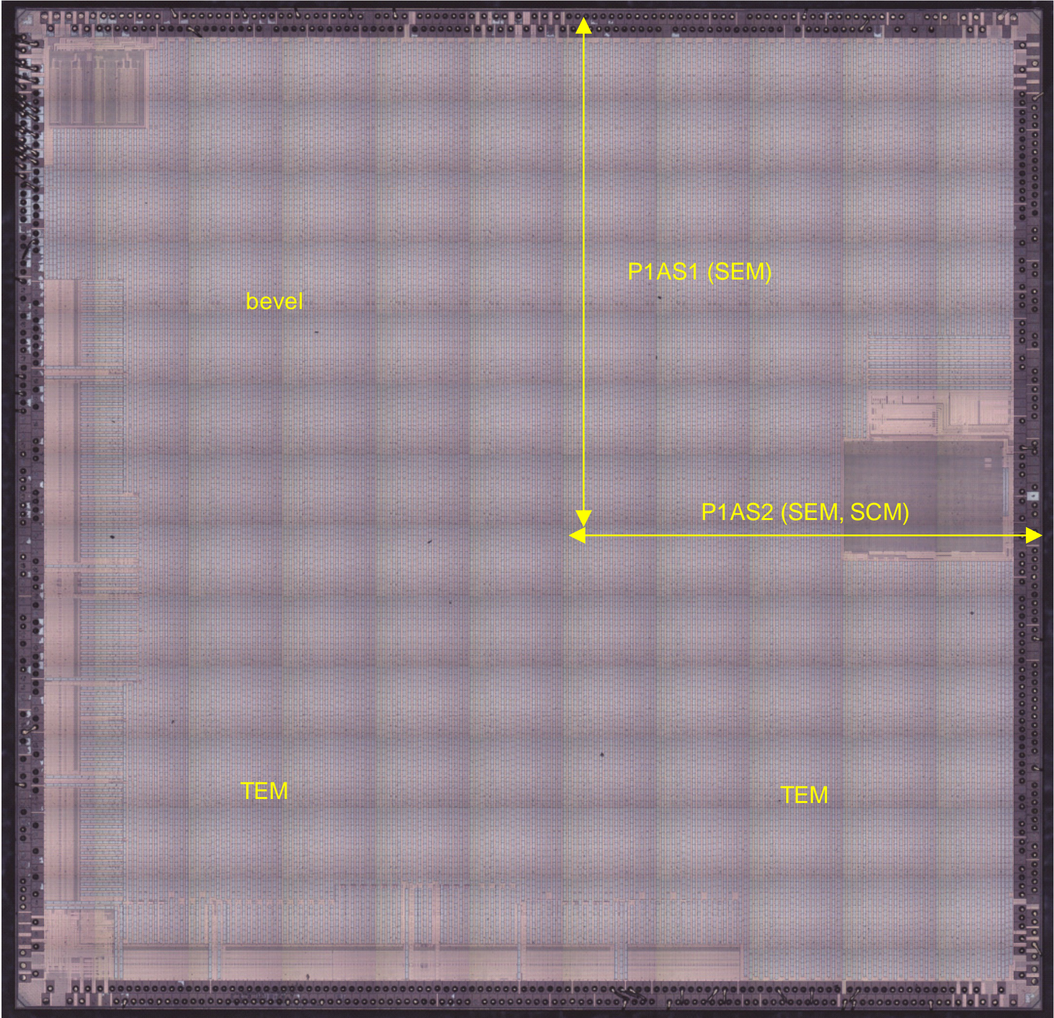

Figure 2.1.7 Analysis Sites

The dimensions of the XXXX package and die are summarized in Table 2.1.1.

Feature	**Size**
Package size	35.0 mm x 35.0 mm x 1.75 mm
Die size (edge seal)	8.42 mm x 8.14 mm
Die area (edge seal)	65.5 mm^2
Die thickness	300 µm
Bond pad size	68 µm x 101 µm
Minimum bond pad pitch	70 µm
NAND cell	0.37 µm x 1.41 µm (0.52 $µm^2$)

Table 2.1.1 Package and Die Dimensions

2.2 Die Features

Figure 2.2.1 through Figure 2.2.8 show the four corners of the XXXX die, at low and high magnification. The metal die seal structure runs along the perimeter of the die, just inside the scribe lane.

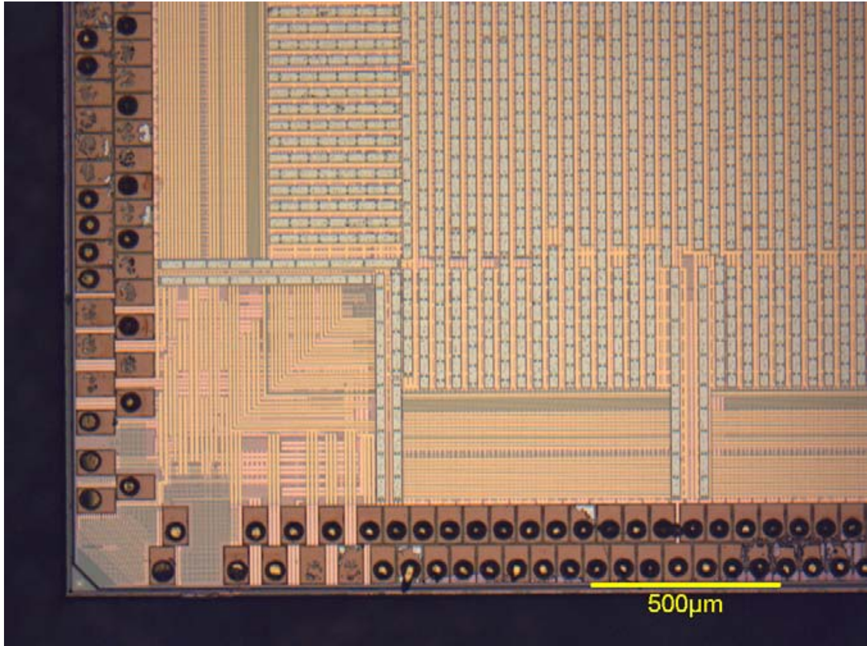

Figure 2.2.1 Die Corner A

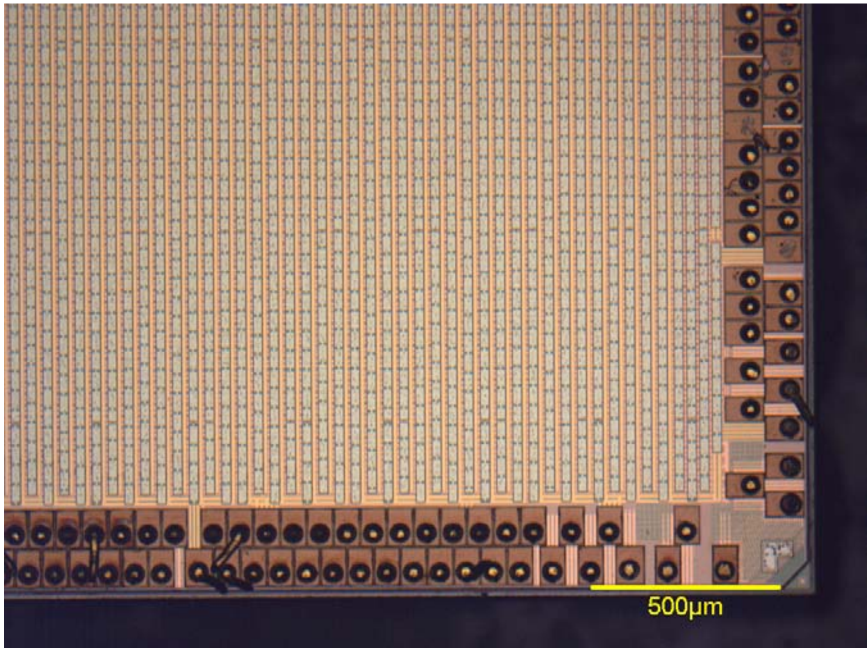

Figure 2.2.2 Die Corner B

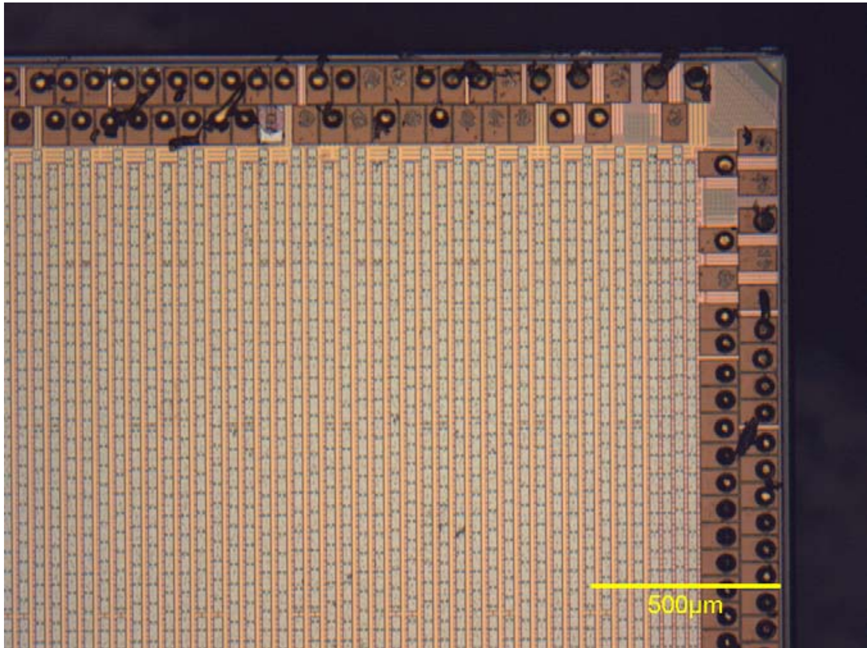

Figure 2.2.3 Die Corner C

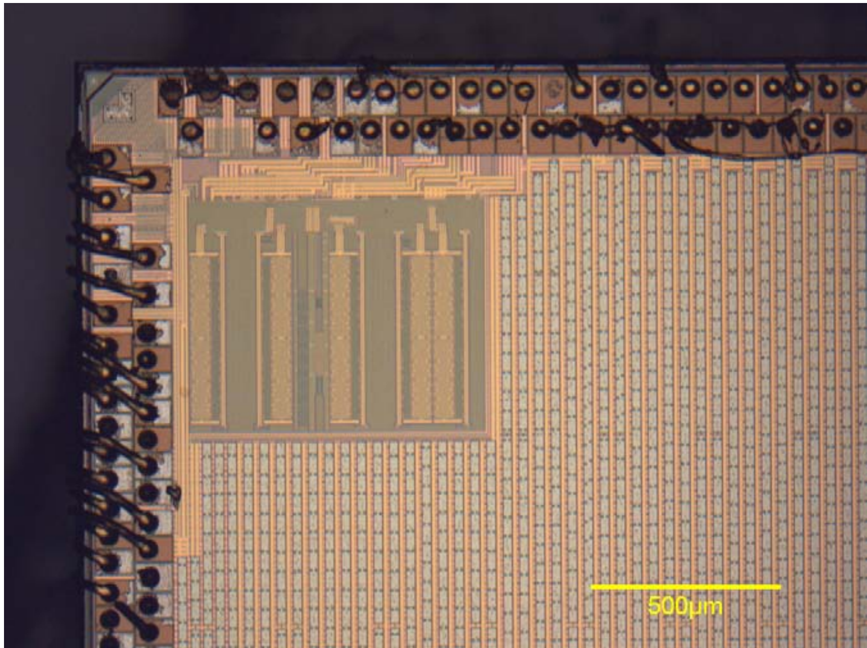

Figure 2.2.4 Die Corner D

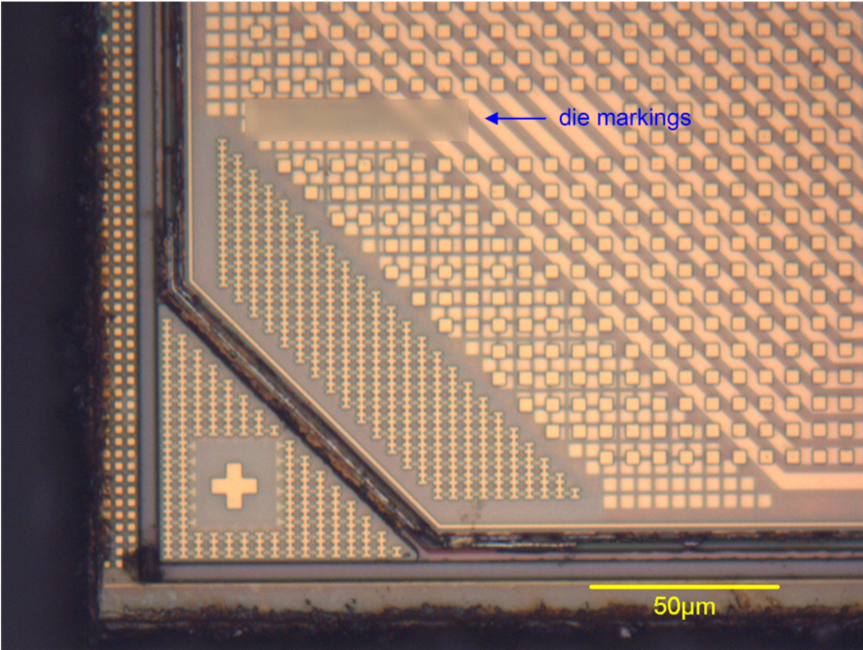

Figure 2.2.5 Detail of Die Corner A

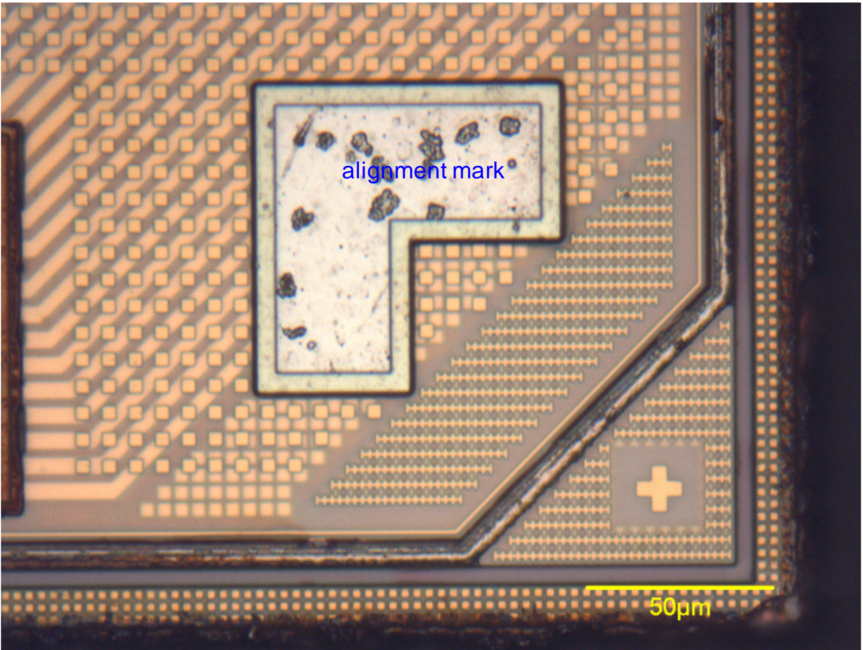

Figure 2.2.6 Detail of Die Corner B

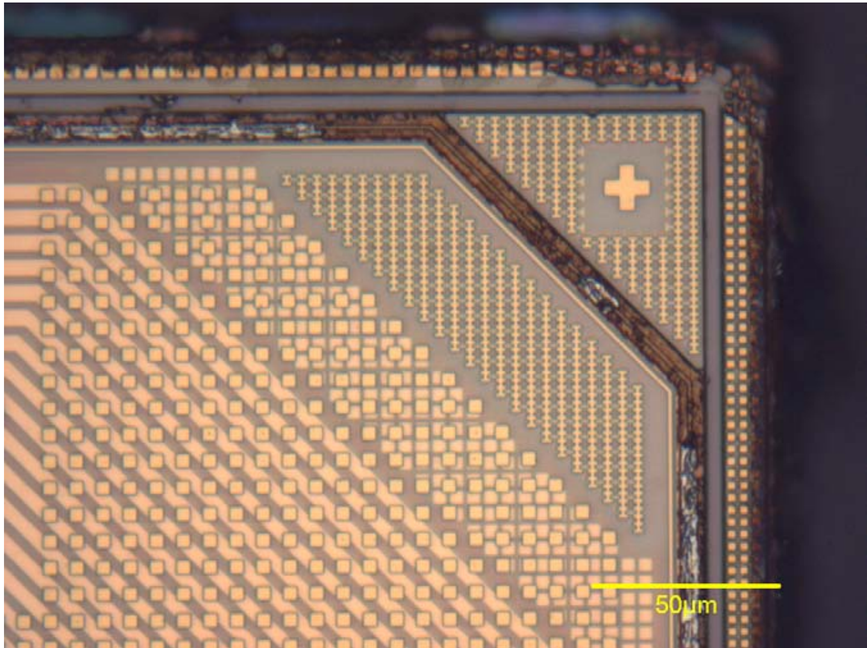

Figure 2.2.7 Detail of Die Corner C

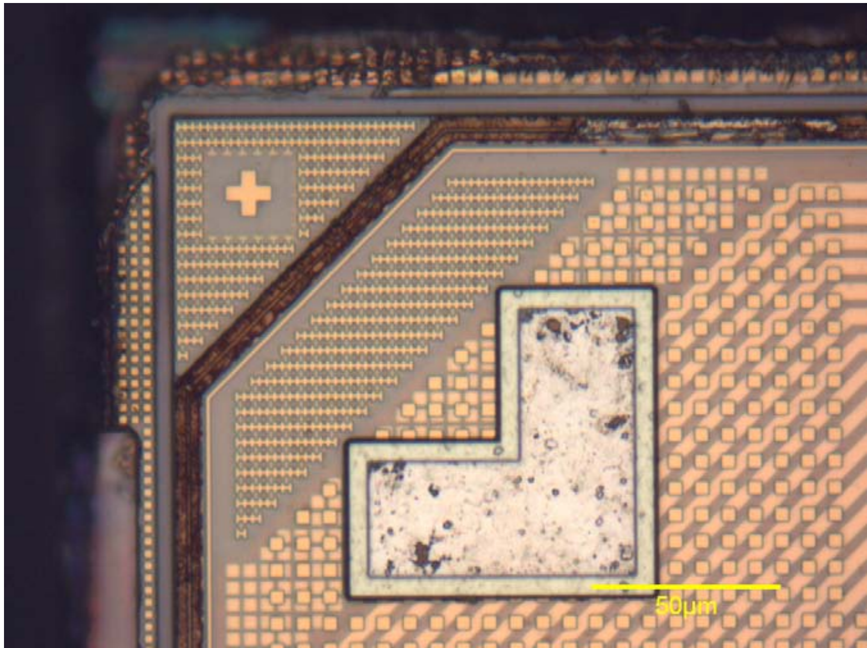

Figure 2.2.8 Detail of Die Corner D

Two rows of 70 µm pitch bond pads are present around the edge of the die, as shown in Figure 2.2.9. The bond pads are 68 µm x 101 µm large in size.

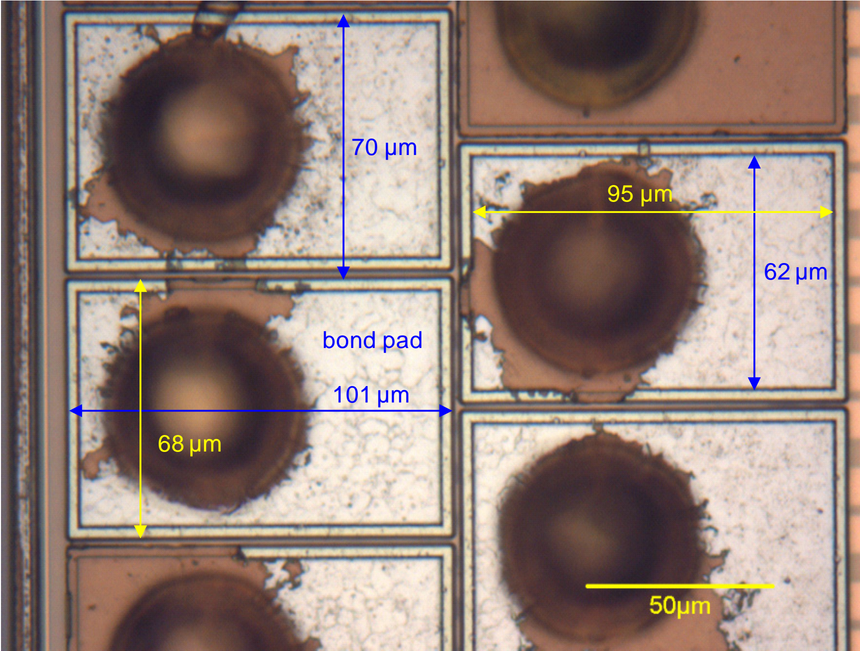

Figure 2.2.9 Bond Pads

2.3 Die Utilization

Figure 2.3.1 shows a poly die photo, annotated to show the functional blocks identified through microscopic observation. The functional block sizes are listed in Table 2.3.1. Analyses of the memory cell blocks are presented in Section X.

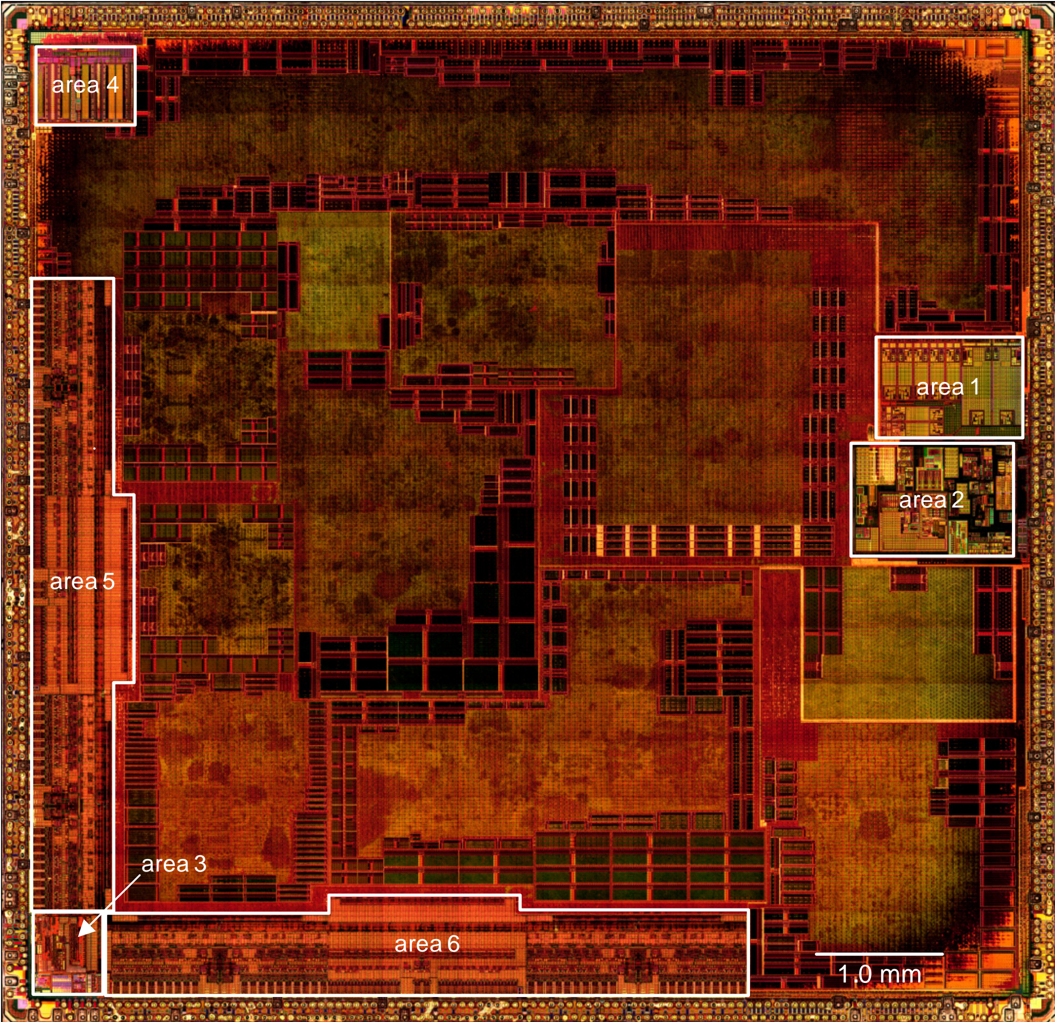

Figure 2.3.1 Die Functional Blocks

Functional Block	Length (mm)	Width (mm)	Area (mm^2)	Percentage
Area 1 (serial interface port)	1.19	0.82	1.0	2%
Area 2 (serial interface port reference)	1.31	0.92	1.2	2%
Area 3 (communications interface port)	0.57	0.67	0.4	1%
Area 4 (video/audio interface port)	0.81	0.64	0.5	1%
Area 5 (DDR2 interface ports)	0.83	5.17	4.3	7%
Area 6 (DDR2 interface ports)	5.17	0.83	4.3	7%
Die size	8.14	8.42	65.5	–

Table 2.3.1 Die Utilization

Detailed images of the area 1 through area 4 blocks are shown in Figure 2.3.1 through Figure 2.3.5. The area 5 and area 6 are two identical DDR2 interface ports, each supporting eight external DDR2 memory chips.

Figure 2.3.2 shows the area 1 block at poly. Area 1 is likely a serial interface port (Firewire) which has nine serial transceivers, including two transceivers with larger sizes.

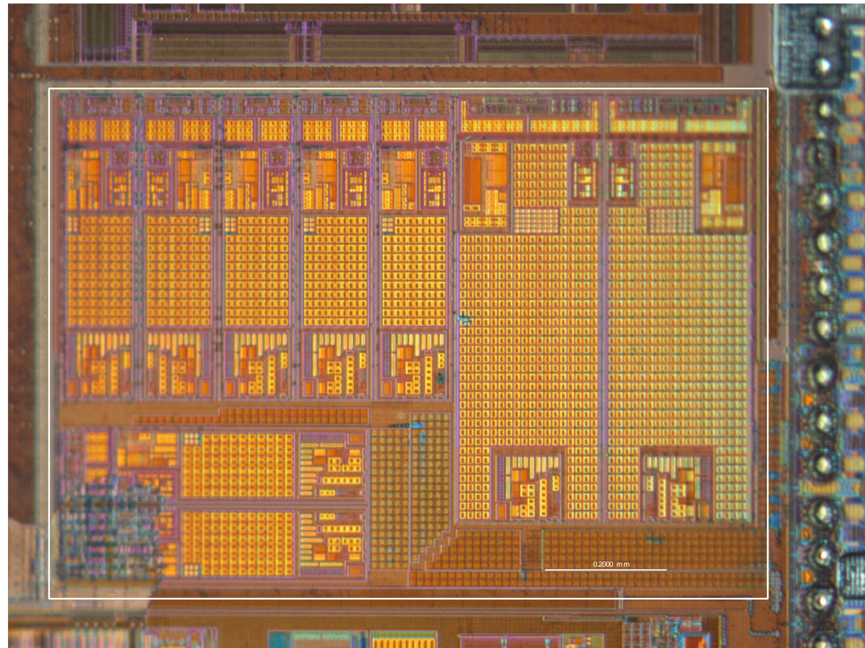

Figure 2.3.2 Area 1

Figure 2.3.3 shows the area 2 block at poly. Area 2 has analog circuits, probably providing reference for the serial interface port of area 1.

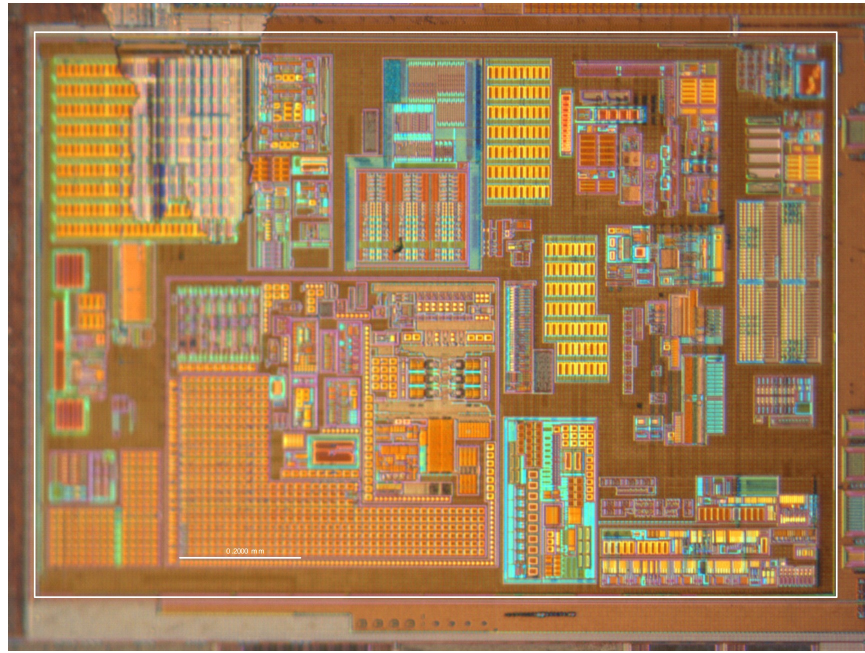

Figure 2.3.3 Area 2

Figure 2.3.4 shows the area 3 block at poly. Area 3 is likely a communication interface port such as USB.

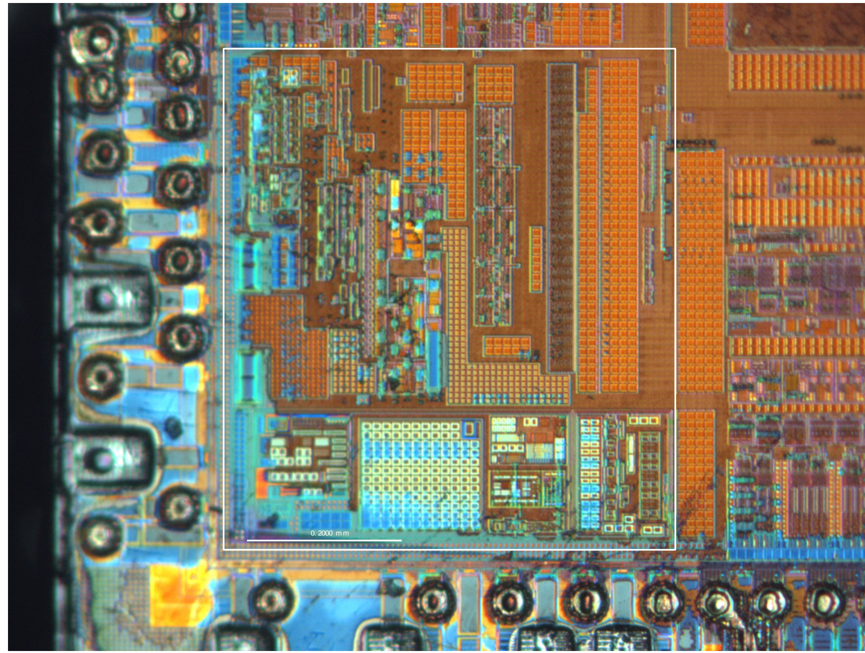

Figure 2.3.4 Area 3

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inside technology

Figure 2.3.5 shows the area 4 block at poly. Area 4 is likely a five-channel video/audio interface port, which includes five identical transmitters implemented with current-steering DAC's.

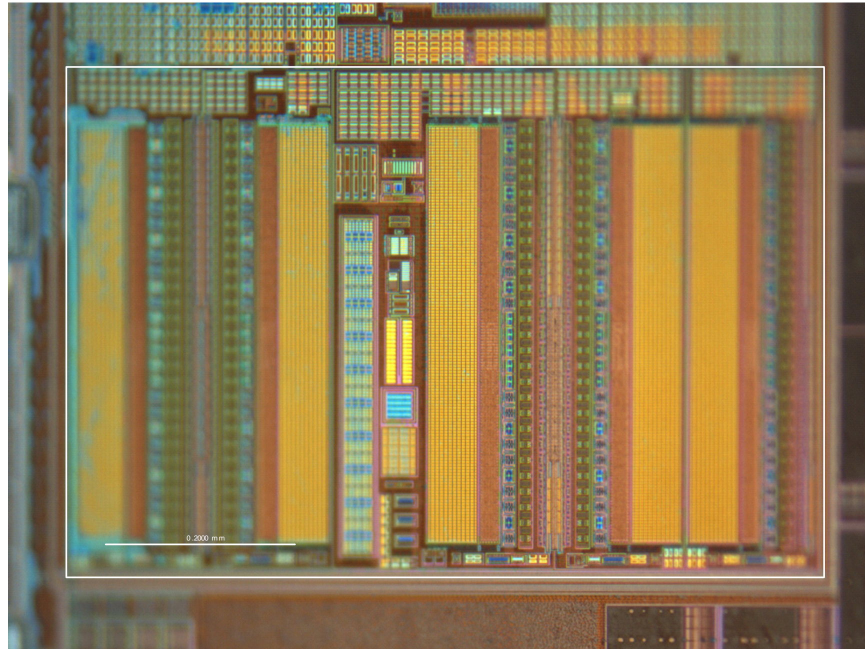

Figure 2.3.5 Area 4

2.4 Selected Layout Features

A delayered sample, prepared for the memory cell analyses presented in Section X, was inspected to determine the use of dummy metal and poly structures.

Figure 2.4.1 shows an overview of the standard logic at metal 1. The unused spaces between active interconnect lines are left unfilled (no dummy metal used).

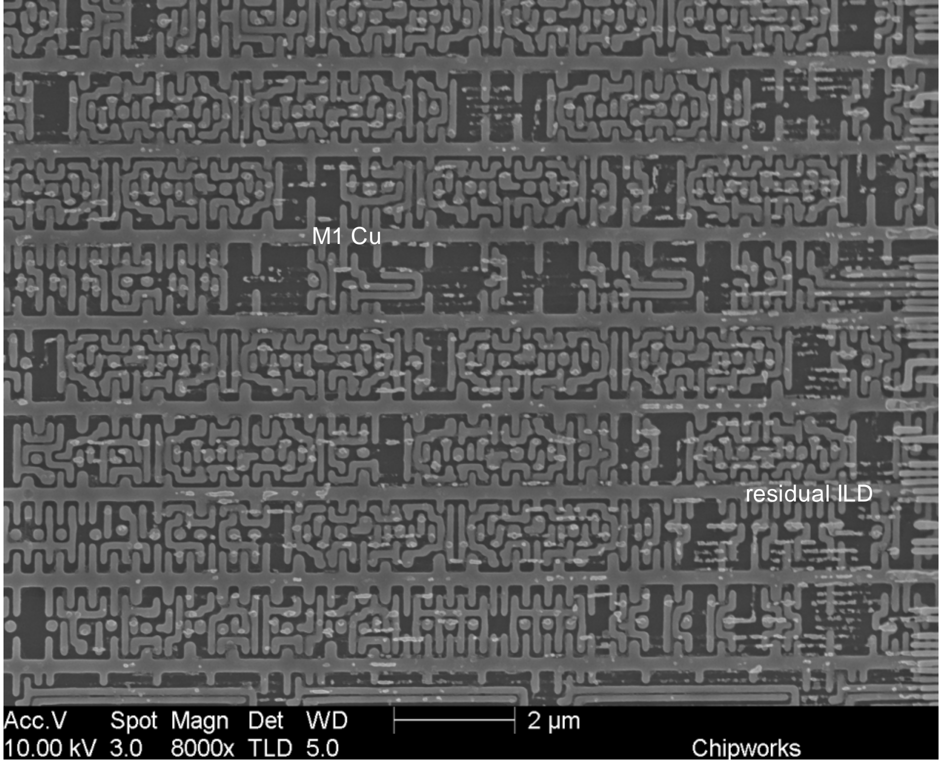

Figure 2.4.1 Standard Logic at Metal 1

Figure 2.4.2 shows a detailed view of the metal 1 patterning over the standard logic cells.

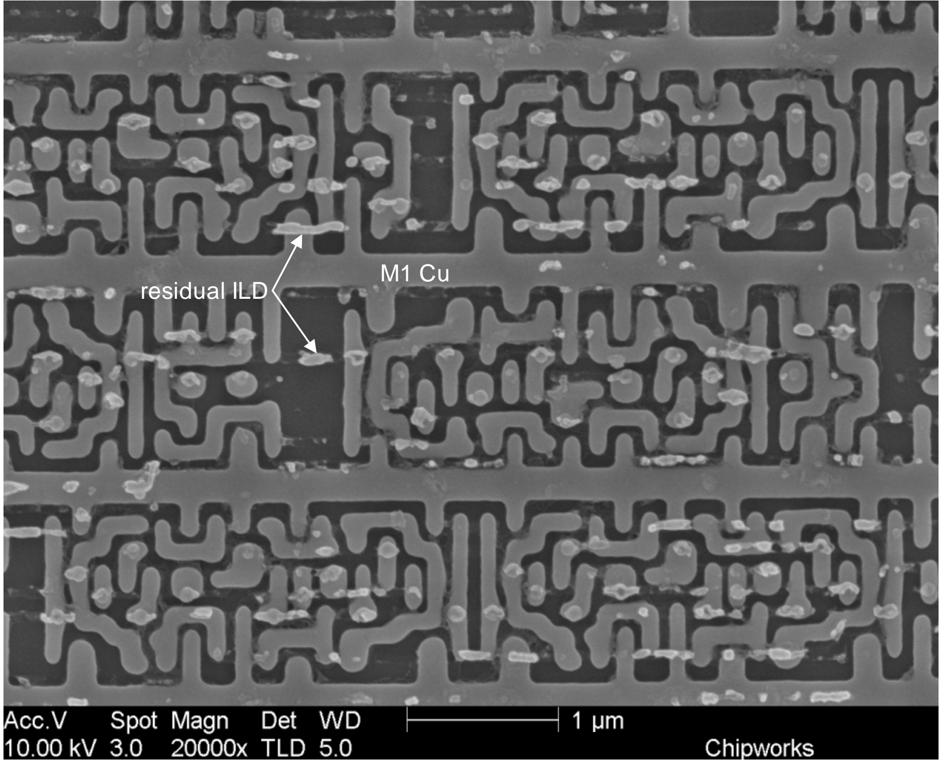

Figure 2.4.2 Detail of Standard Logic Cells at Metal 1

Figure 2.4.3 is an overview of the corner of a block of standard logic. Several rows of dummy poly surround the logic block.

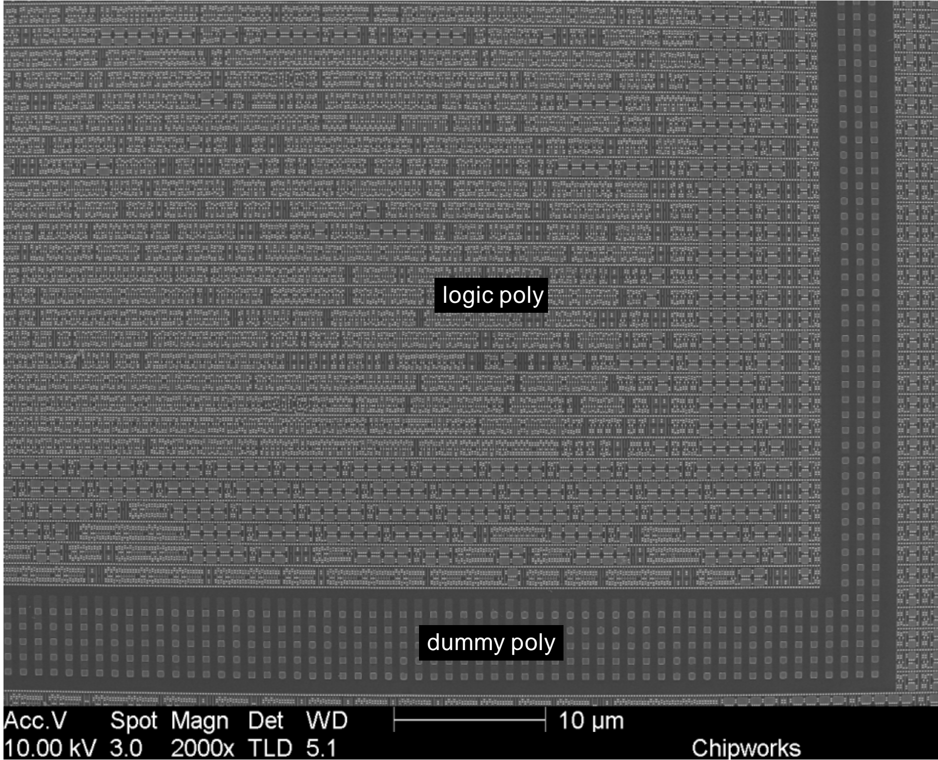

Figure 2.4.3 Overview of Standard Logic at Poly

Figure 2.4.4 shows several rows of standard logic. Both minimum gate length and wide gate transistors are used. Dummy poly lines fill the unused space between functional groupings of logic gates.

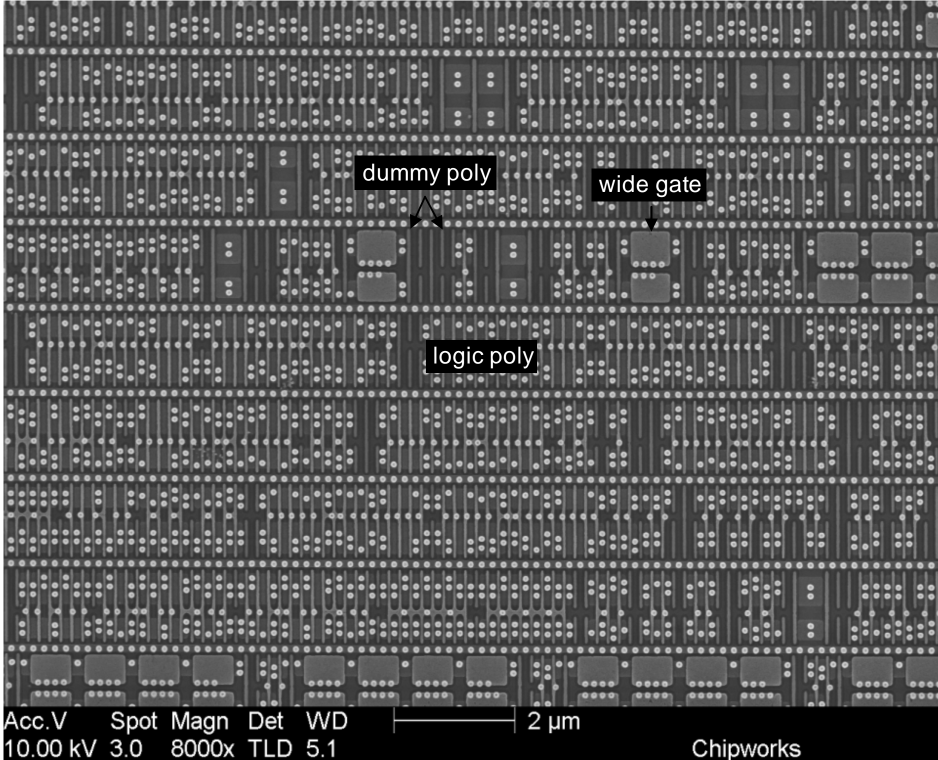

Figure 2.4.4 Standard Logic at Poly – Wide Gates

Figure 2.4.5 shows a detailed view of the equivalent area occupied by a NAND cell. A typical NAND cell would be 0.38 µm wide by 1.41 µm high, yielding a 0.54 μm^2 cell. Dummy poly is used on each end of the logic cells.

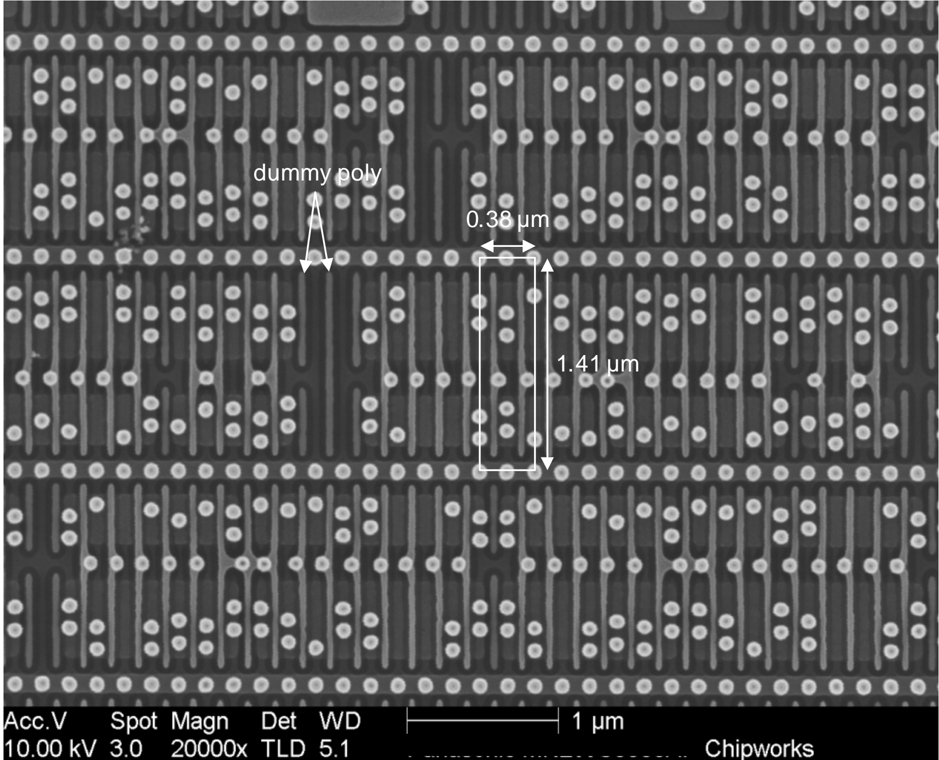

Figure 2.4.5 Standard Logic – Standard Cell Size and Dummy Poly

3 Process Analysis

3.1 General Structure

Figure 3.1.1 shows the general structure of the XXXX, which features eight levels of Cu metallization plus a top layer of Al.

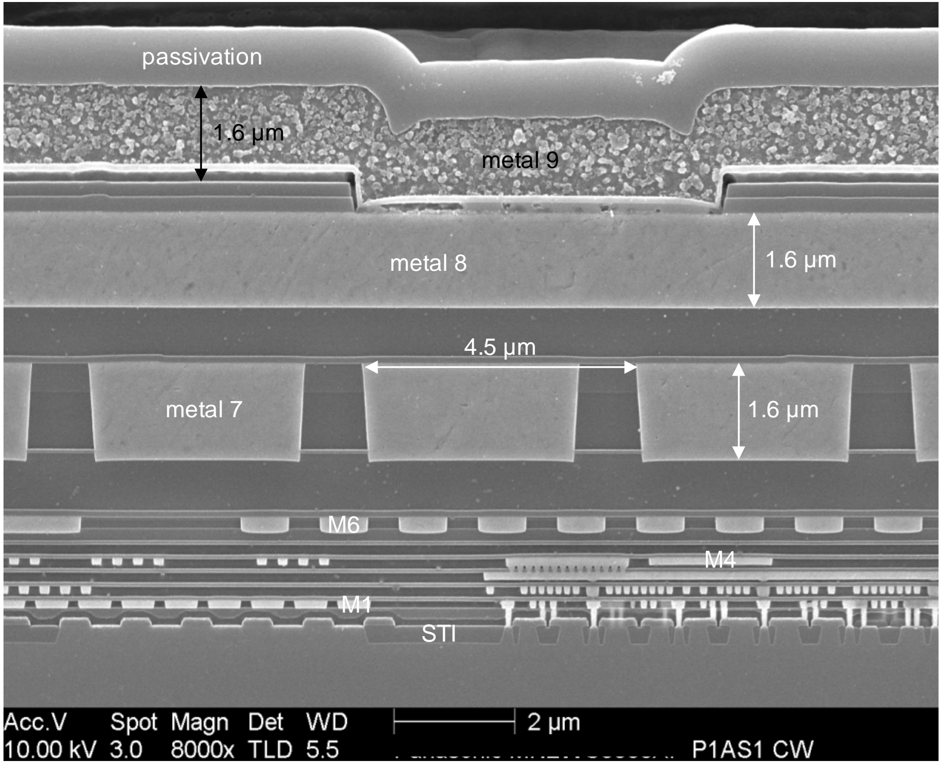

Figure 3.1.1 General Structure

Figure 3.1.2 and Figure 3.1.3 show cross-sectional views of the die. A single, full-depth saw cut was used for die singulation. No bevel has been applied to the die edge. The finished die is 300 µm thick.

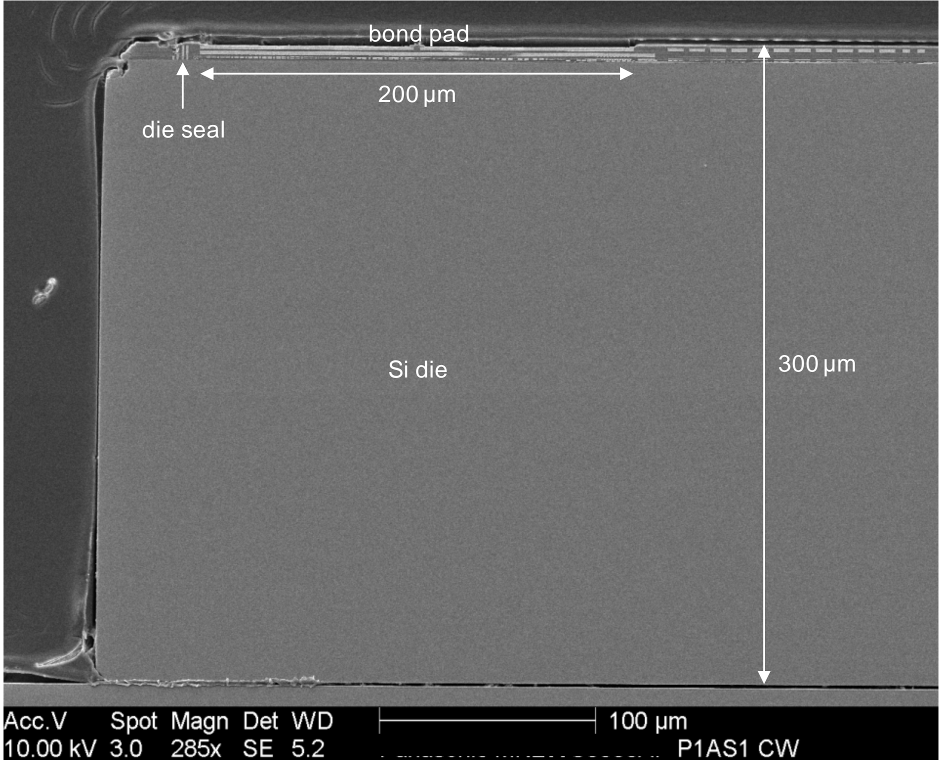

Figure 3.1.2 Die Thickness

Figure 3.1.3 shows the die seal structure. The die seal is comprised of all eight levels of Cu, plus the Al bond pad metal. The top portion of the die seal ring was etched during our sample depot process.

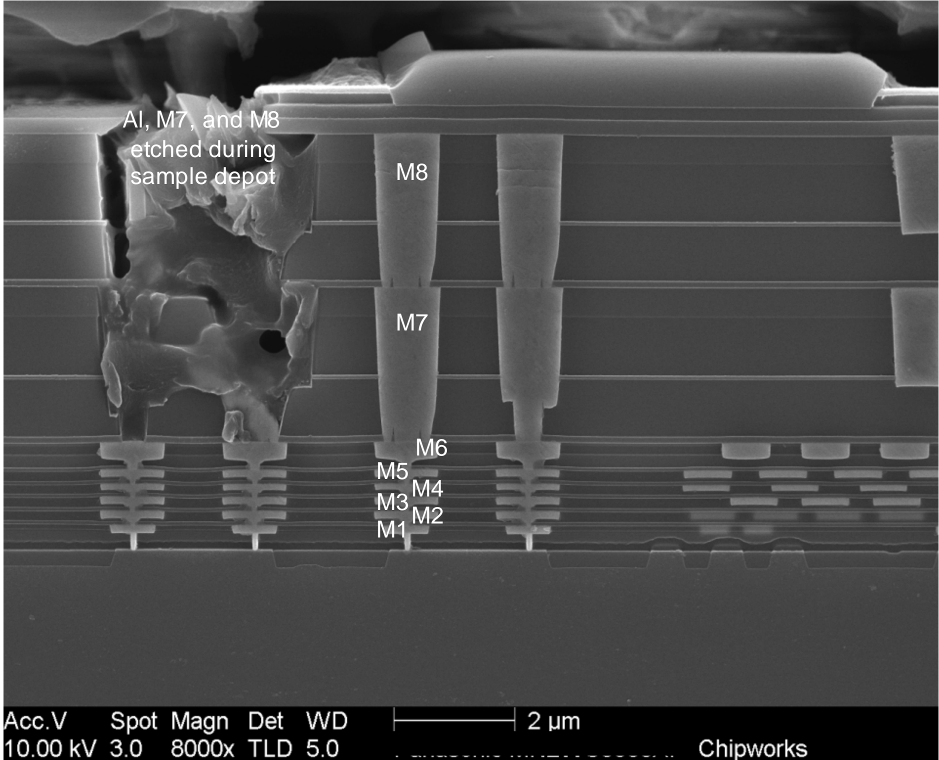

Figure 3.1.3 Die Edge Seal

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3.2 Dielectrics

The XXXX uses conventional oxide, oxynitride and silicon nitride, fluorinated silicate glass (FSG) “intermediate-k”, and carbon doped low-k films for the passivation, interlevel dielectrics (ILD), and pre-metal dielectric (PMD). A full chemical mechanical planarization (CMP) process is used as part of the damascene Cu line formation.

Table 3.2.1 lists the measured dielectric film thicknesses and material compositions, as determined by TEM-EDS. We have used the numbering convention such that the first film deposited is designated as ILD n-1, followed by ILD n-2, etc. The TEM-EDS spectra of the various dielectric films are presented in Figure 3.2.13 through Figure 3.2.18.

Layer	Composition (Top to Bottom)	Layer Thickness (µm)
Passivation	Silicon nitride	0.94
ILD 8	Oxide/oxynitride	0.46 (0.21/0.25)
ILD 7	Oxide/FSG/SiON/oxide/SiON	2.49 (0.44/0.94/0.07/0.92/0.12)
ILD 6	Oxide/FSG/SiON/oxide/SiON	2.56 (0.48/0.97/0.06/0.94/0.11)
ILD 5	FSG/oxide/SiCNO	0.45 (0.19/0.21/~0.05)
ILD 4	SiOC/SiCNO	0.20 (0.15/~0.05)
ILD 3	SiOC/SiCNO	0.23 (0.18/~0.05)
ILD 2	SiOC/SiCNO	0.21 (0.16/~0.05)
ILD 1	SiOC/SiCNO	0.21 (0.16/~0.05)
PMD	SiOC/oxide/oxide/oxide/SiON	0.44 (0.08/0.02/0.21/0.12/0.01)

Table 3.2.1 Measured Dielectric Thicknesses

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Figure 3.2.1 shows an overview of the dielectric stack. The passivation and ILD 8 films are comprised of undoped oxide, oxynitride, and silicon nitride.

The thick ILD 6 and ILD 7 layers are comprised of undoped oxide, FSG, and oxynitride.

ILD 5 is comprised of undoped oxide, FSG, and SiCNO.

The thin ILD 1 through ILD 4 films are comprised of SiOC and SiCNO low-k dielectrics.

The PMD is comprised of undoped oxide, oxynitride, and SiOC.

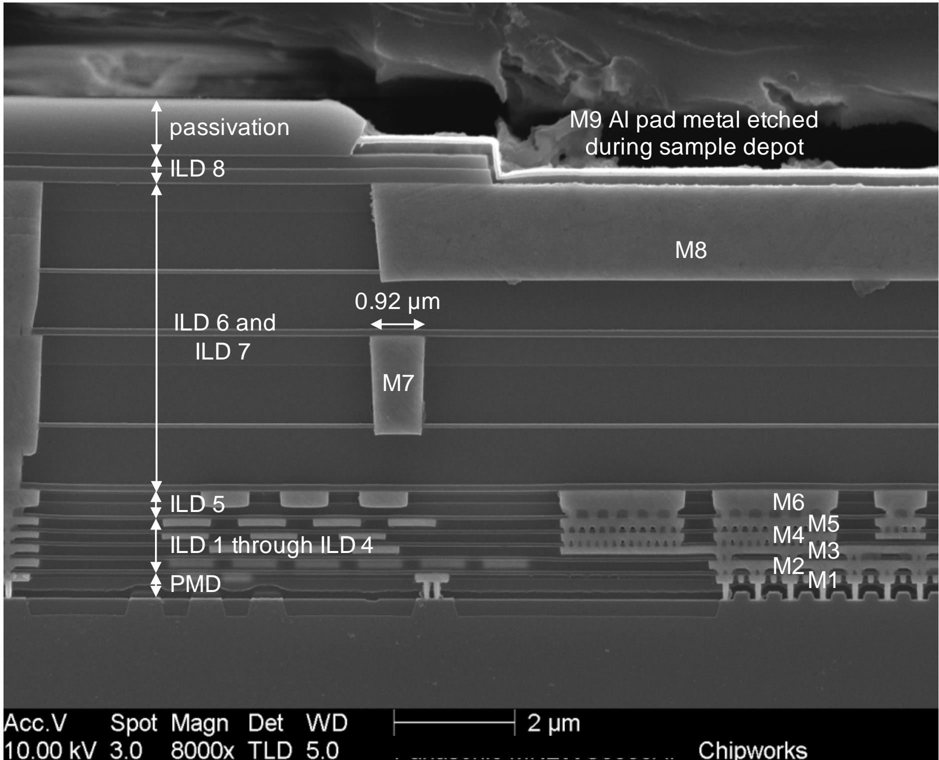

Figure 3.2.1 Dielectric Stack Overview

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Figure 3.2.2 shows the 0.94 μm thick conformal layer of silicon nitride passivation. The TEM image of Figure 3.2.4 reveals no sub layers for this film.

The figure also shows the 0.46 μm thick ILD 8. ILD 8-1 is a 0.25 μm thick oxynitride, while ILD 8-2 is a 0.21 μm thick undoped oxide.

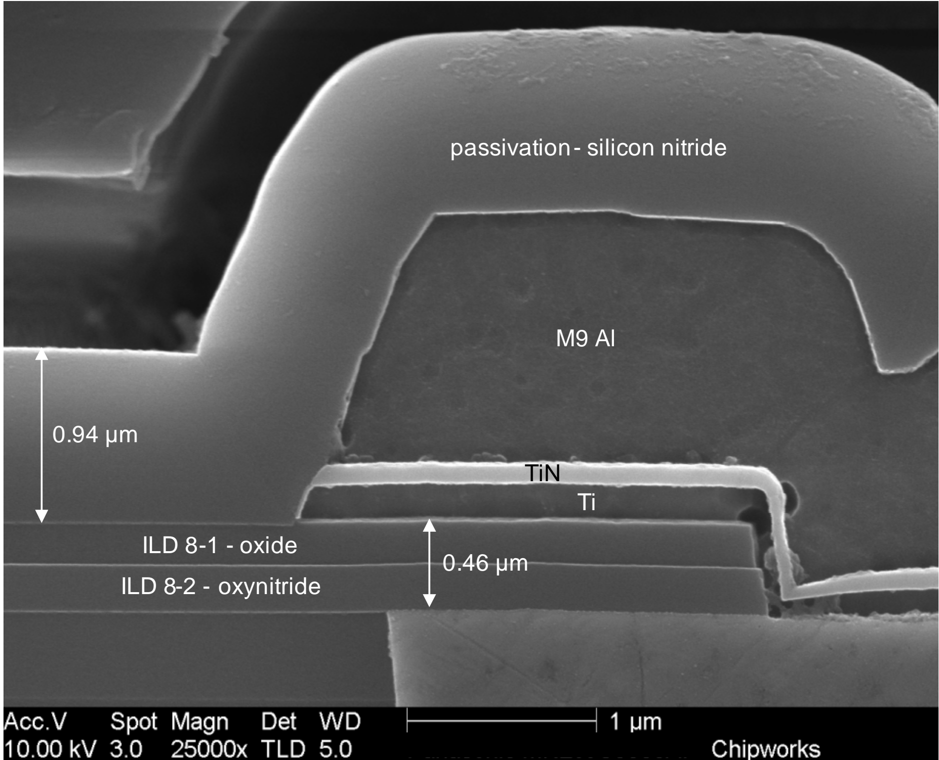

Figure 3.2.2 Passivation and ILD 8

Figure 3.2.3 shows an overview of the 2.49 µm thick ILD 7. ILD 7-1 is a 0.12 µm thick oxynitride film used to seal the metal 7 Cu. ILD 7-2 is a 0.92 µm thick undoped oxide serving as the via 7 dielectric. A 0.07 µm thick oxynitride, ILD 7-3, serves as the metal 8 trench etch stop layer. The metal 8 line dielectric is comprised of a 0.94 µm thick FSG (ILD 7-4) and a 0.44 µm thick undoped oxide (ILD 7-5).

The underlying ILD 6 has an overall thickness of 2.56 µm, and features the same composition as ILD 7.

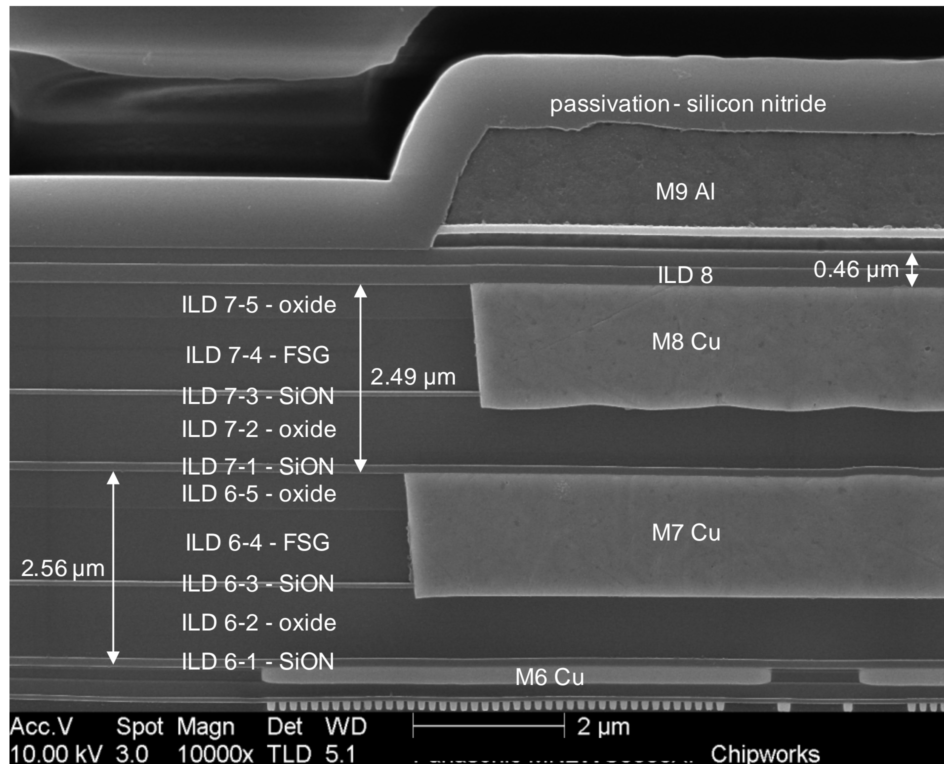

Figure 3.2.3 ILD 6 and ILD 7

Figure 3.2.4 shows a TEM image of the ILD 7, ILD 8, and passivation layers.

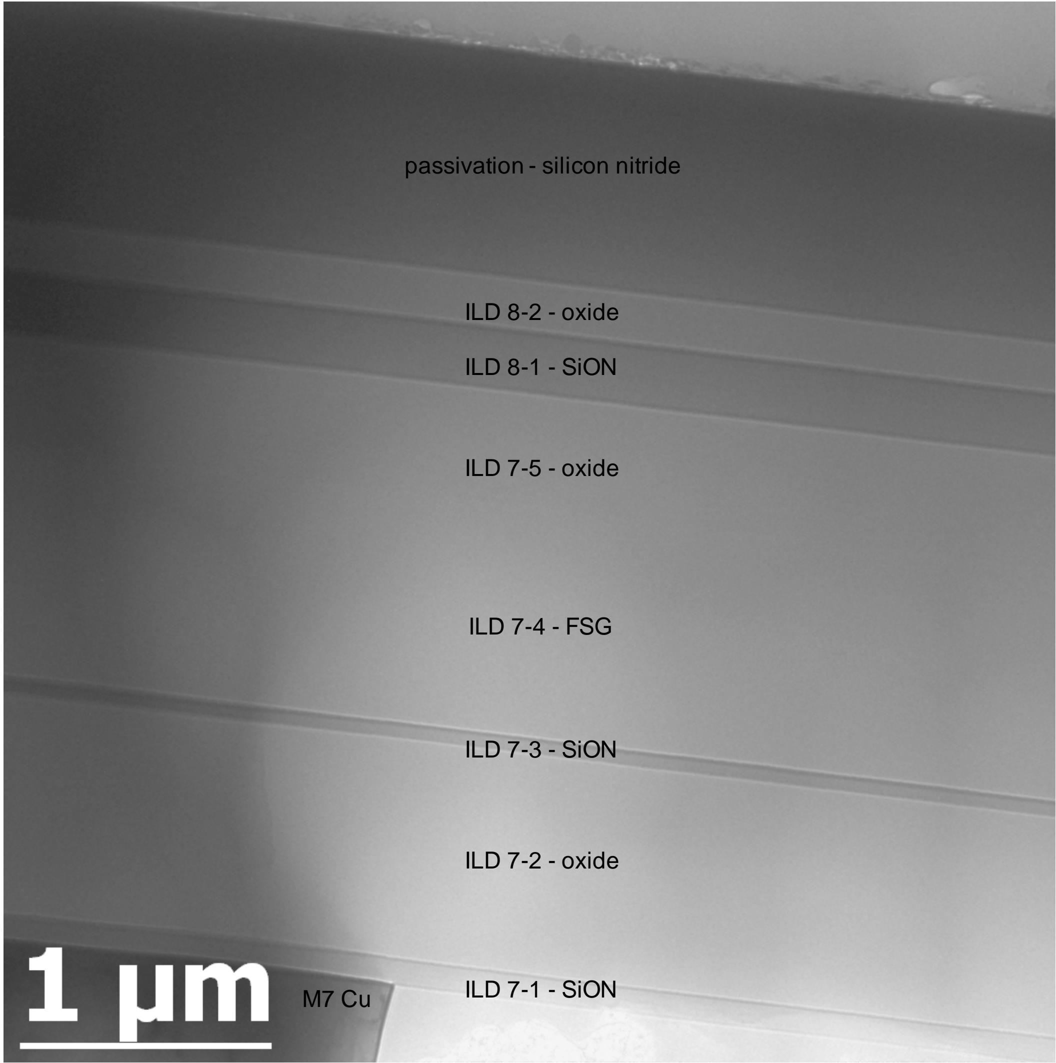

Figure 3.2.4 ILD 7 – TEM

Figure 3.2.5 shows an overview of the ILD 3 through ILD 5 layers. ILD 5 uses an FSG line dielectric, while the underlying ILD 1 through ILD 4 layers use SiOC line and via dielectrics to lower the capacitance between the aggressively pitched metal lines used at these levels.

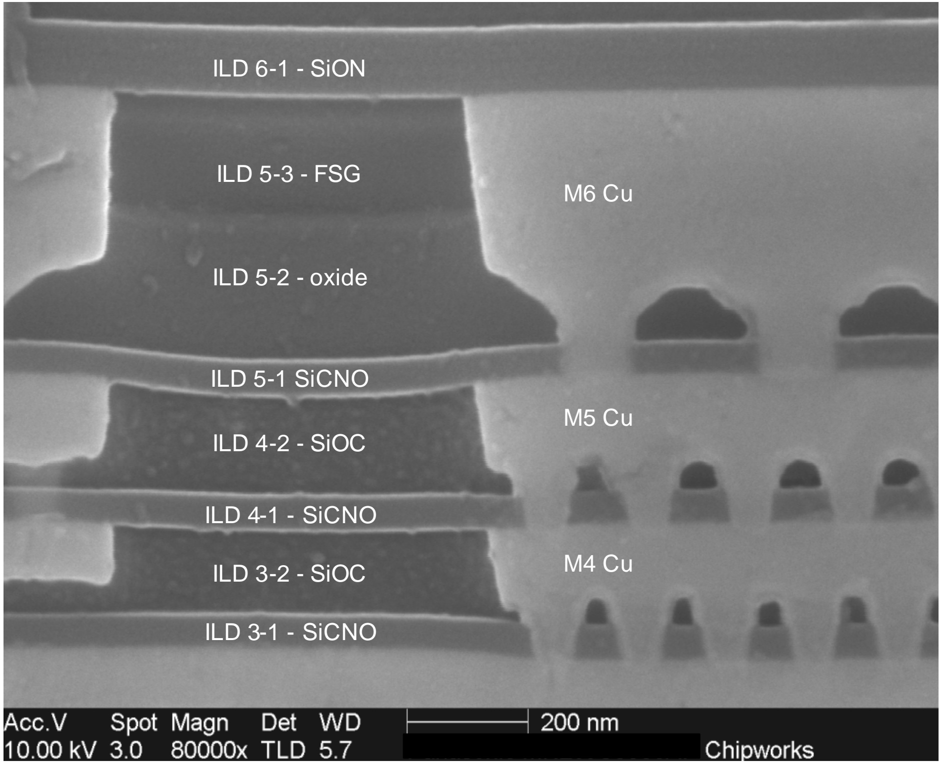

Figure 3.2.5 ILD 3, ILD 4, and ILD 5

Figure 3.2.6 shows the 0.45 µm thick ILD 5. ILD 5-1 is a 45 nm thick bi-layer of SiCNO serving to seal the metal 5 Cu. While these two layers are not resolved in Figure 3.2.6, they are delineated for the lower level ILDs as shown in Figure 3.2.7 through Figure 3.2.9. The two layers likely have different densities, which yield the TEM contrast. Their elemental compositions appear to be the same as determined by TEM-EDS.

ILD 5-2 is an undoped oxide serving as the via dielectric. ILD 5-3 is an FSG serving as the line dielectric.

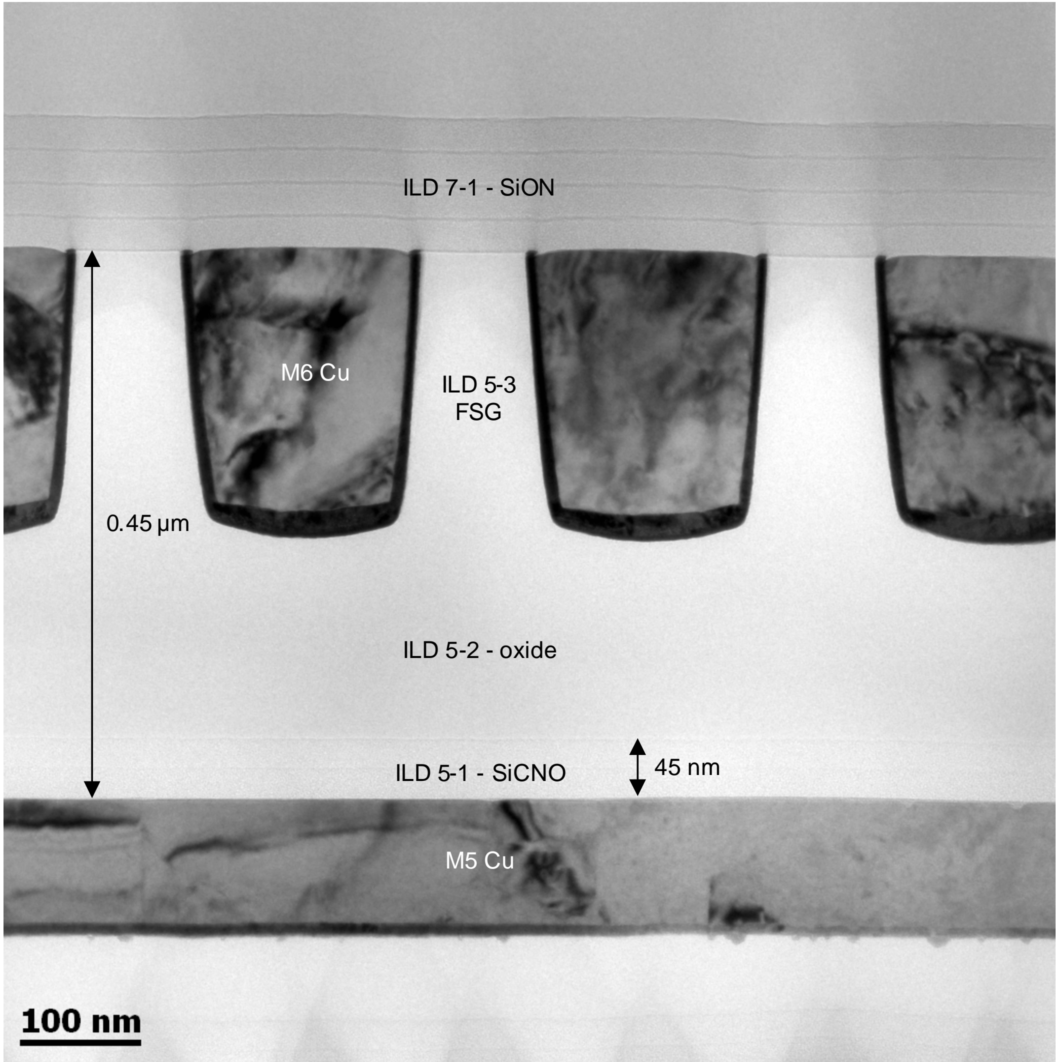

Figure 3.2.6 TEM of ILD 5 – TEM

Figure 3.2.7 shows the 0.20 µm thick ILD 4. The bi-layered SiCNO ILD 4-1 is about 0.05 µm thick, while the SiOC ILD 4-2 is about 0.15 µm thick. The ILD 1 through ILD 4 layers are comparable in thickness and feature the same composition.

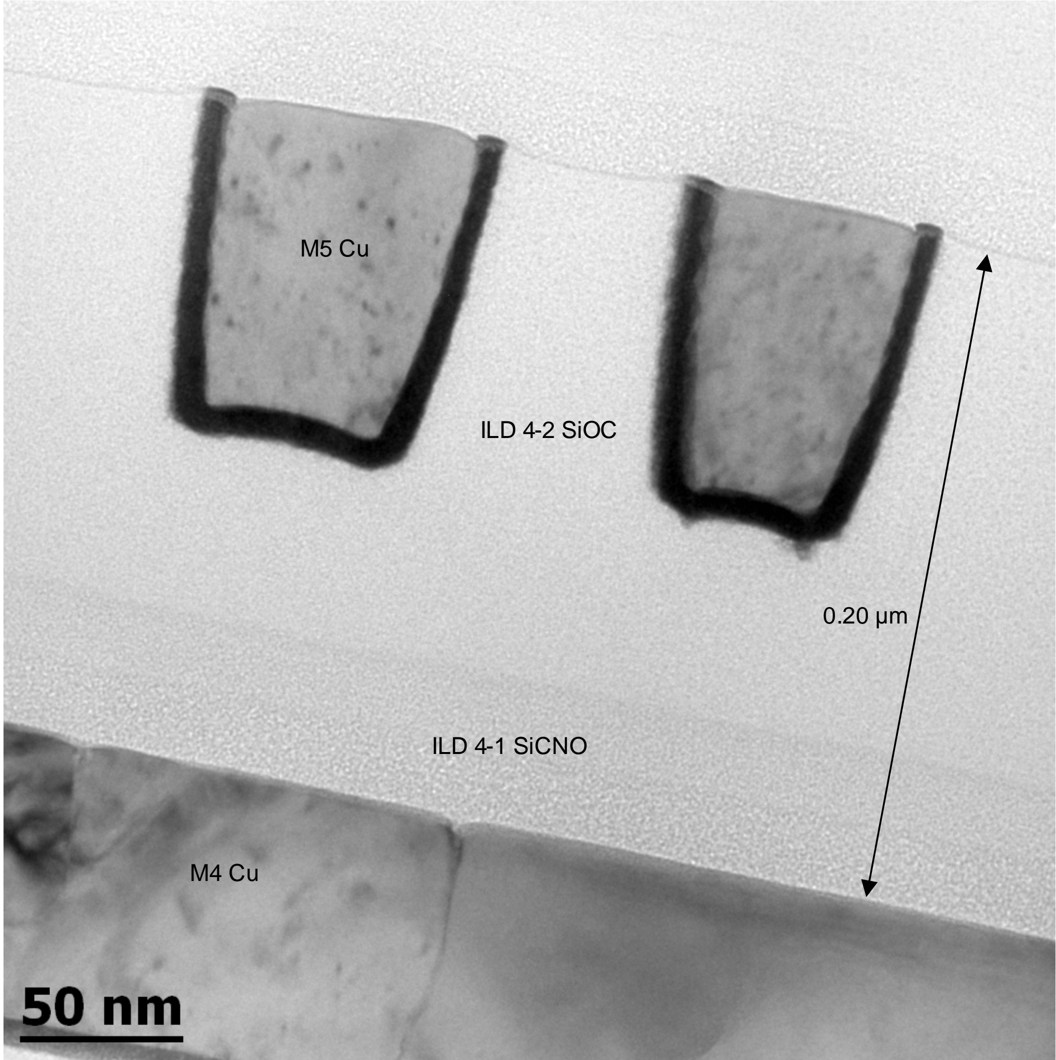

Figure 3.2.7 ILD 4 – TEM

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Figure 3.2.8 shows the 0.23 µm thick ILD 3.

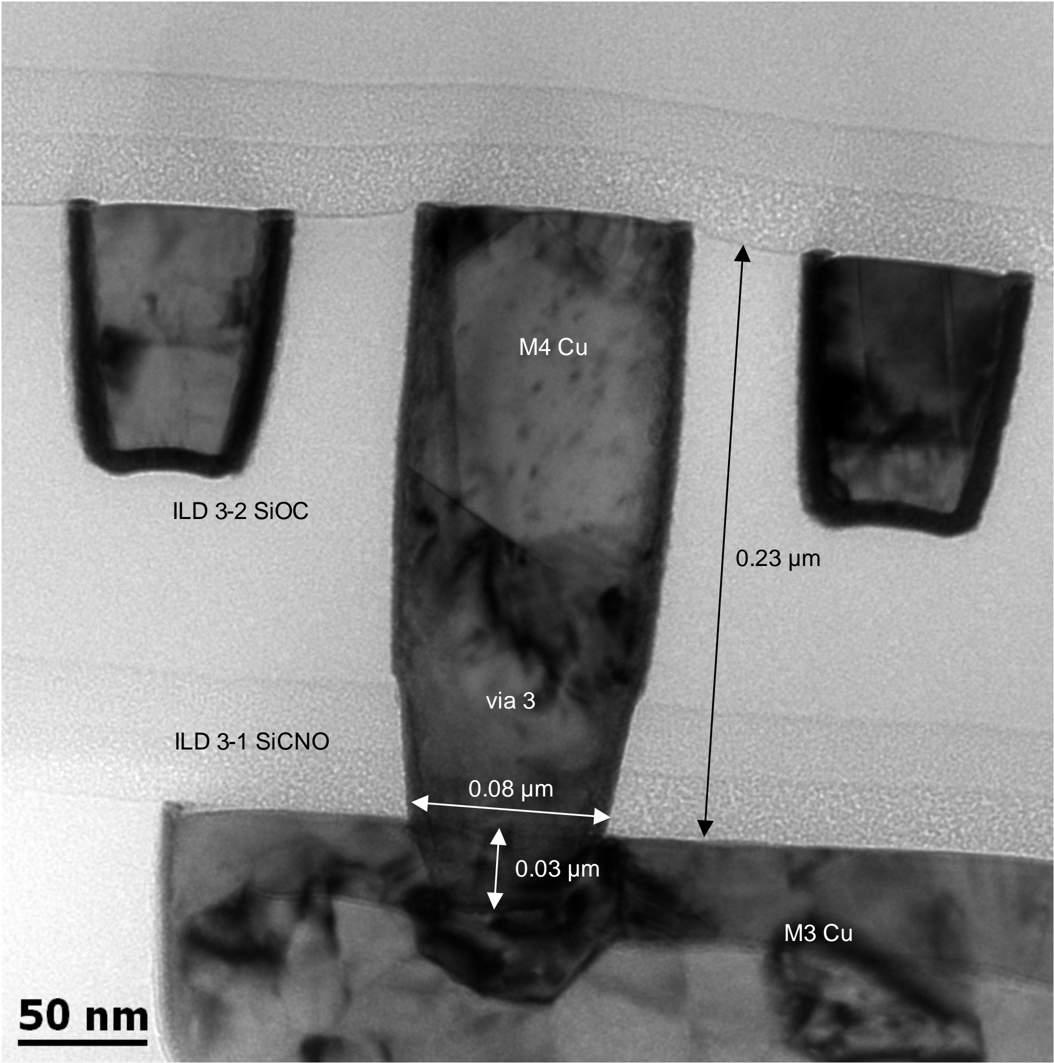

Figure 3.2.8 ILD 3 – TEM

Figure 3.2.9 shows the 0.21 μm thick ILD 2. The two SiCNO layers making up the ILD 2-1 are clearly delineated in this image.

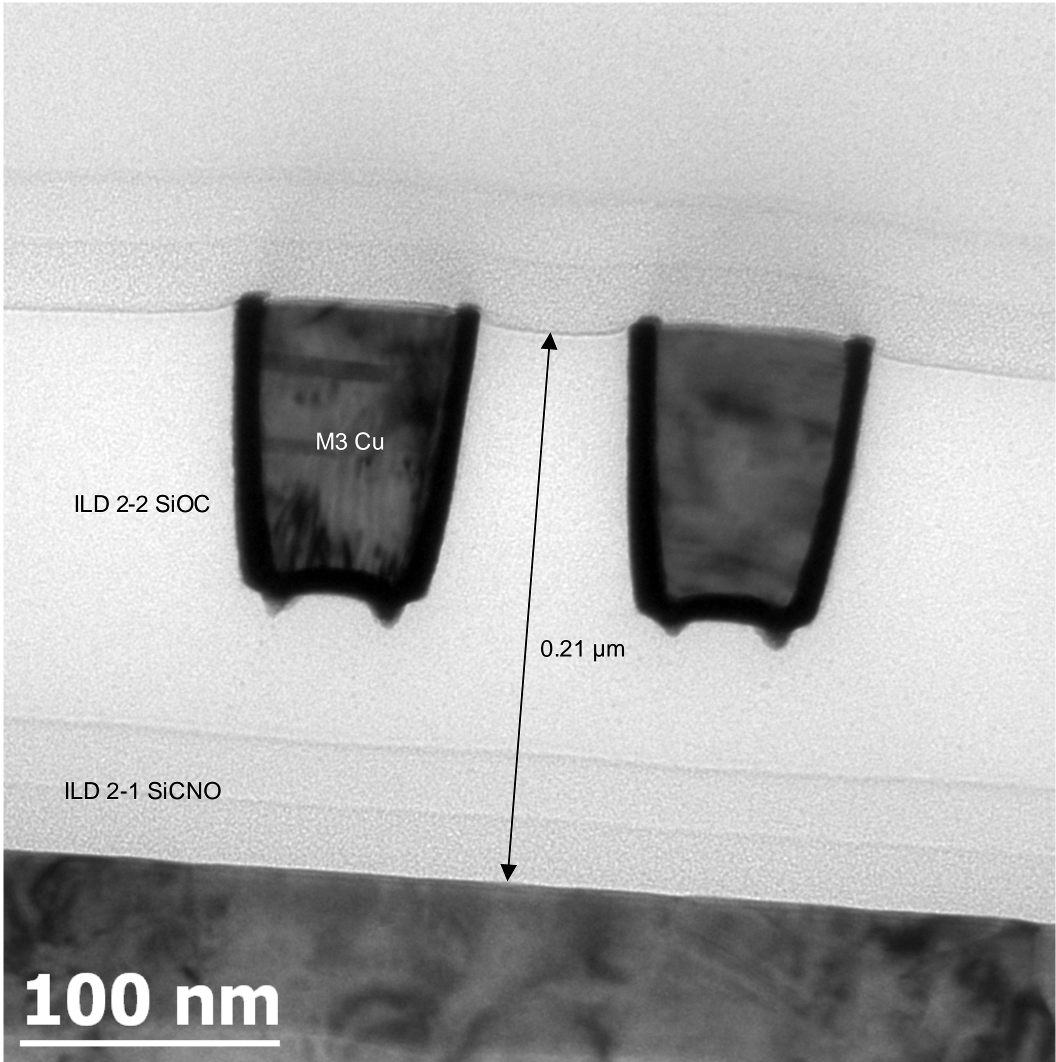

Figure 3.2.9 ILD 2 – TEM

Figure 3.2.10 shows the 0.21 µm thick ILD 1.

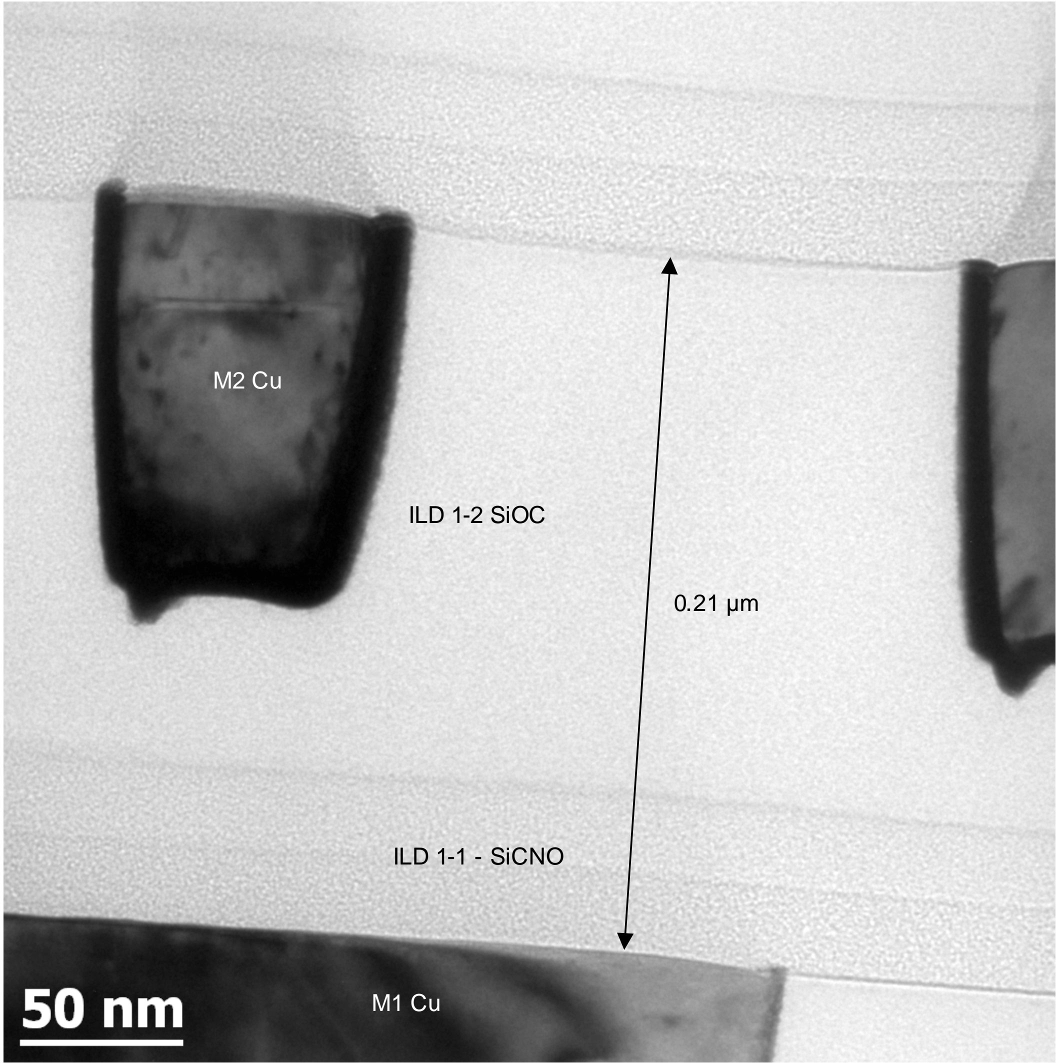

Figure 3.2.10 ILD 1 – TEM

Figure 3.2.11 and Figure 3.2.12 are SEM and TEM views of the PMD, respectively. PMD 1 is an approximately 0.01 µm thick oxynitride, serving as the contact etch stop layer (CESL). PMD 2 is an approximately 0.12 µm thick undoped oxide. PMD 3 is an approximately 0.21 µm thick undoped oxide. The varied response of PMD 2 and PMD 3 to our oxide etch suggests PMD 2 may be a CVD oxide while PMD 3 may be an HDP oxide. PMD 2 and PMD 3 serve as the contact dielectric.

PMD 4 is an undoped oxide, serving as the metal 1 trench etch stop layer. PMD 5 is an 0.08 µm thick SiOC, serving as the metal 1 line dielectric.

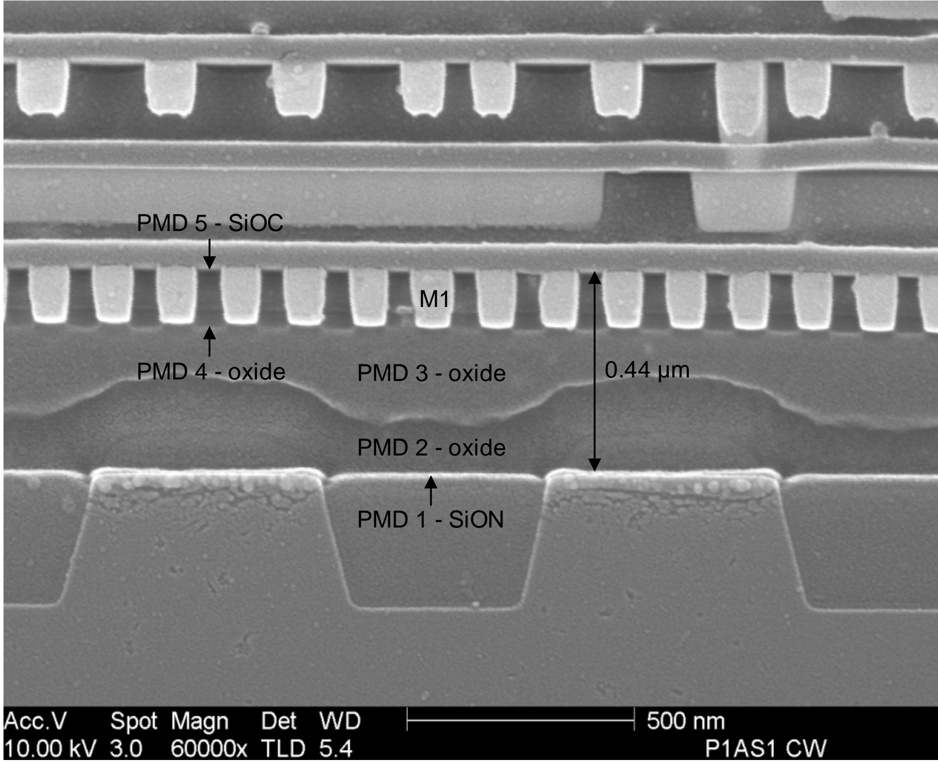

Figure 3.2.11 PMD Overview

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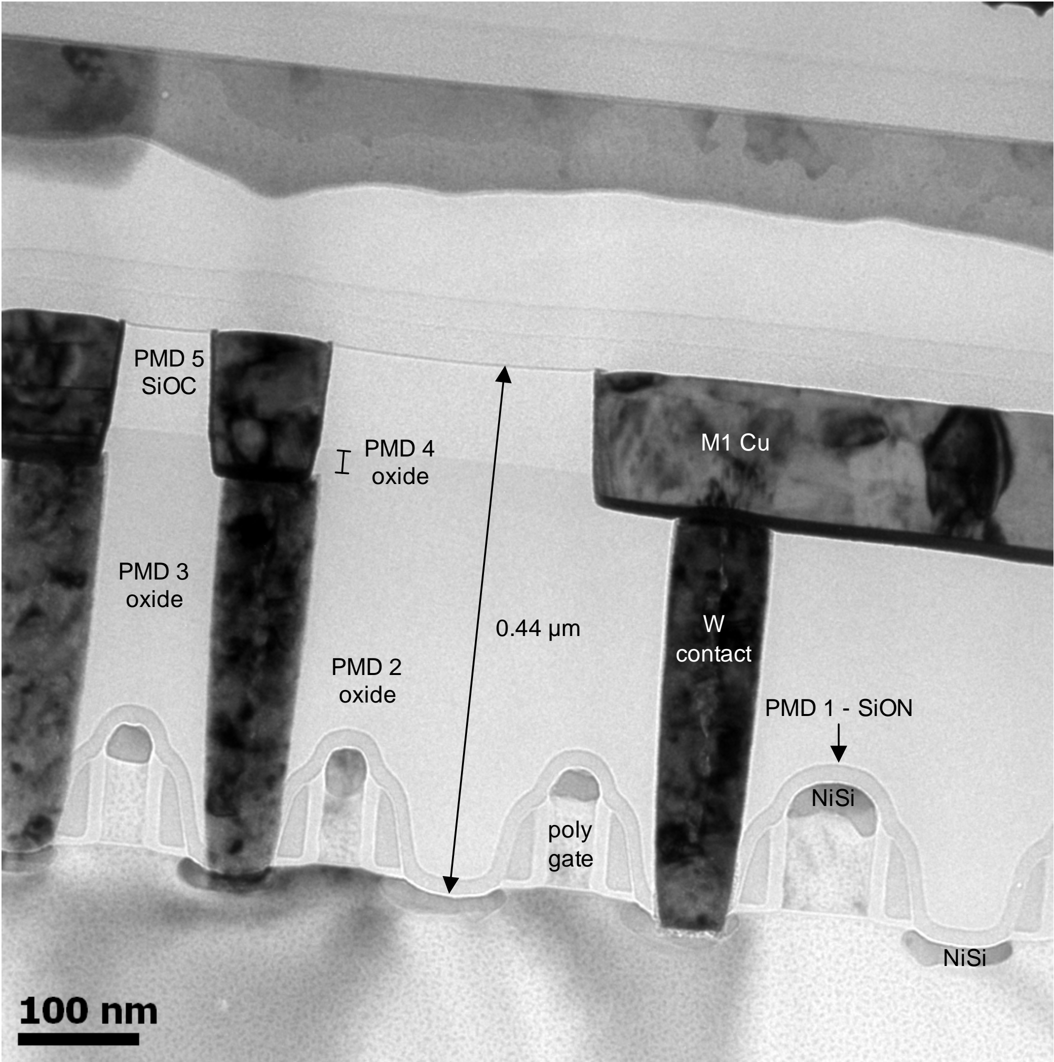

Figure 3.2.12 PMD – TEM

Figure 3.2.13 shows the TEM-EDS spectrum of the silicon nitride passivation.

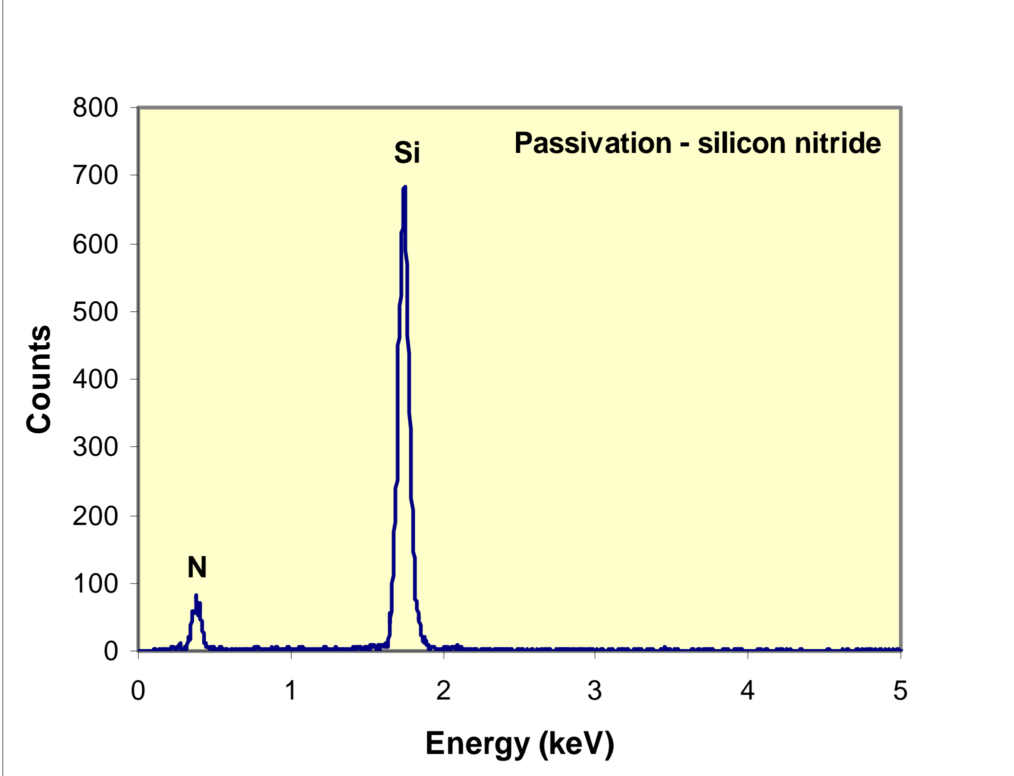

Figure 3.2.13 TEM-EDS Spectrum of Passivation

Figure 3.2.14 shows the TEM-EDS spectra of the ILD 7-4 FSG and ILD 7-5 undoped oxide. These spectra are representative of the ILD 6-4 and 6-5 layers.

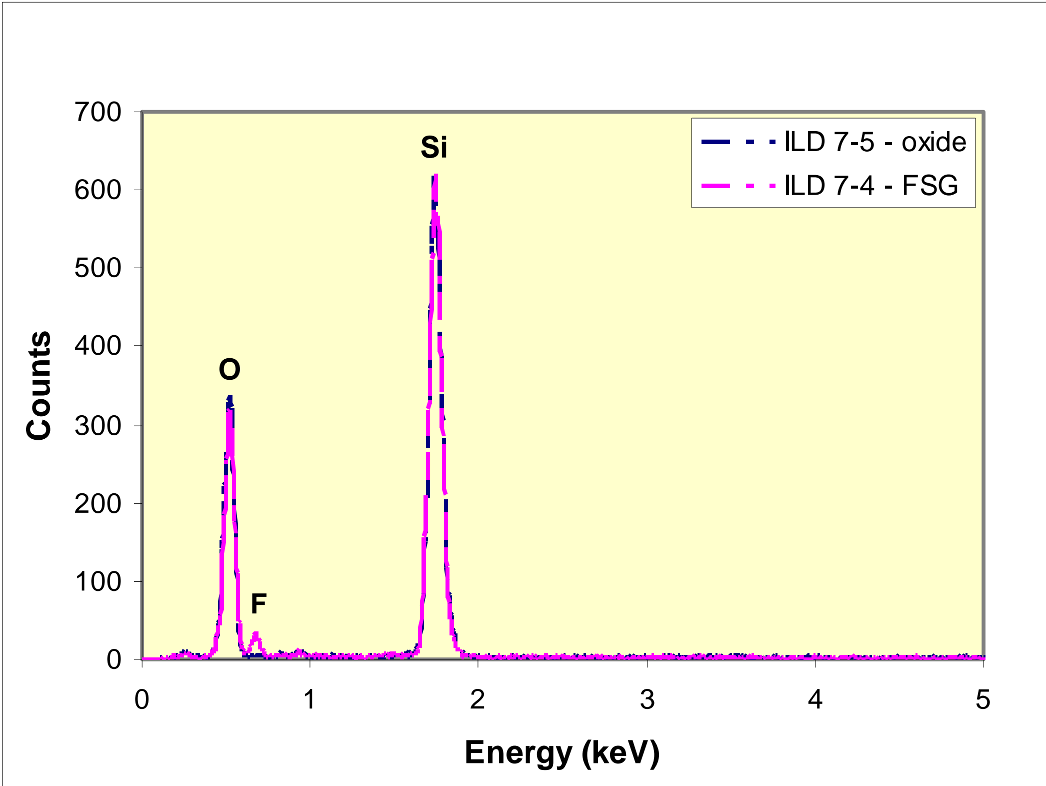

Figure 3.2.14 TEM-EDS Spectra of ILD 7-4 and ILD 7-5

Figure 3.2.15 shows the TEM-EDS spectra of the multilayered ILD 7-1 SiON, ILD 7-2 undoped oxide, and ILD 7-3 SiON. These spectra are representative of the ILD 6-1 through 6-3 layers.

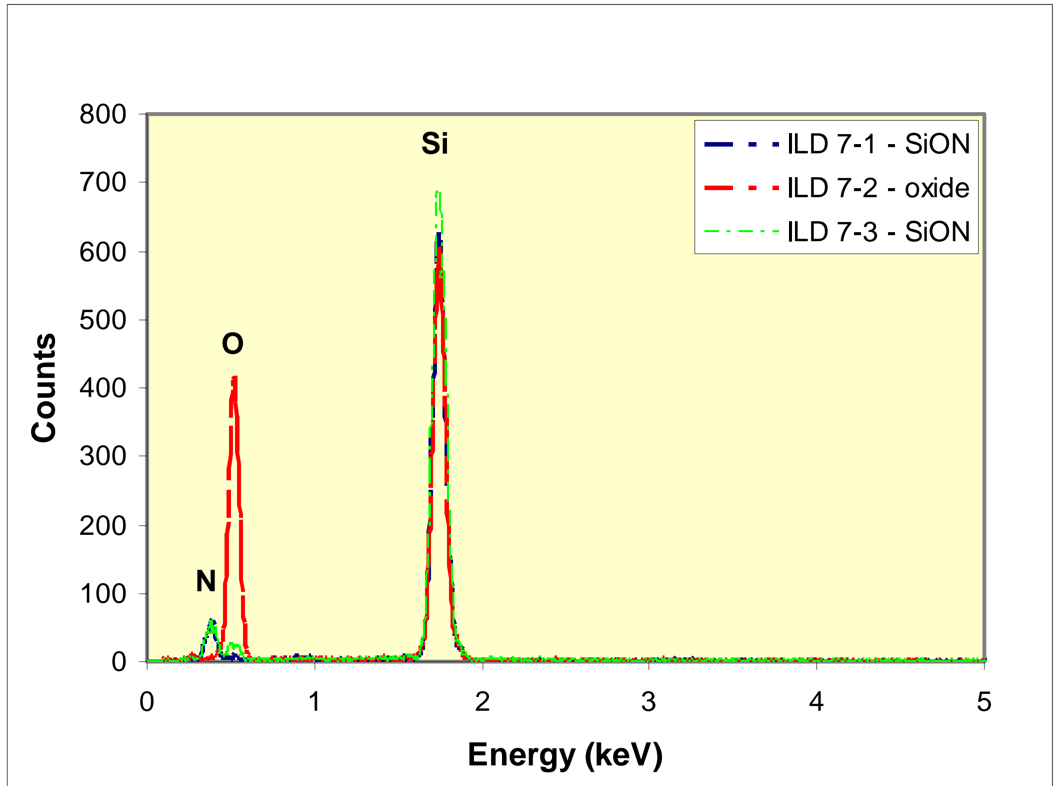

Figure 3.2.15 TEM-EDS Spectra of ILD 7-1 through ILD 7-3

Figure 3.2.16 shows the TEM-EDS spectra of the bi-layered ILD 5-1 SiOC, ILD 5-2 undoped oxide, and ILD 5-3 FSG.

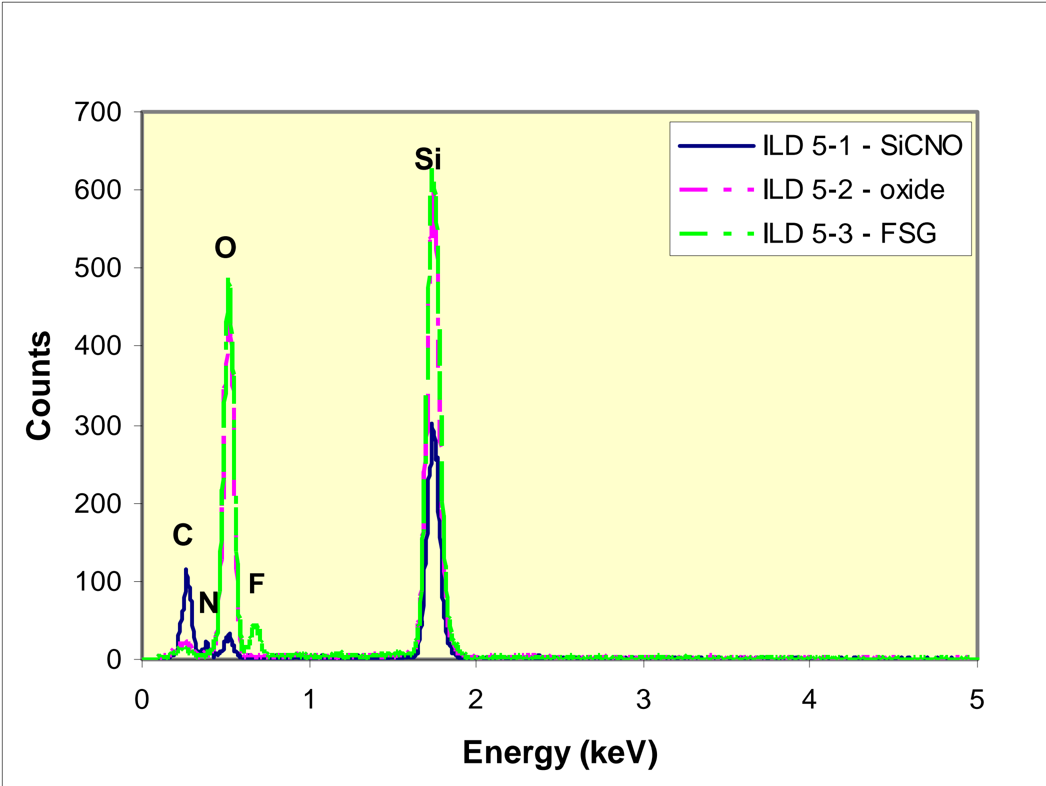

Figure 3.2.16 TEM-EDS Spectra of ILD 5

Figure 3.2.17 shows the TEM-EDS spectra of the bi-layered ILD 1-1 SiONC and ILD 1-2 SiOC. These spectra are representative of the ILD 2 through ILD 4 composition.

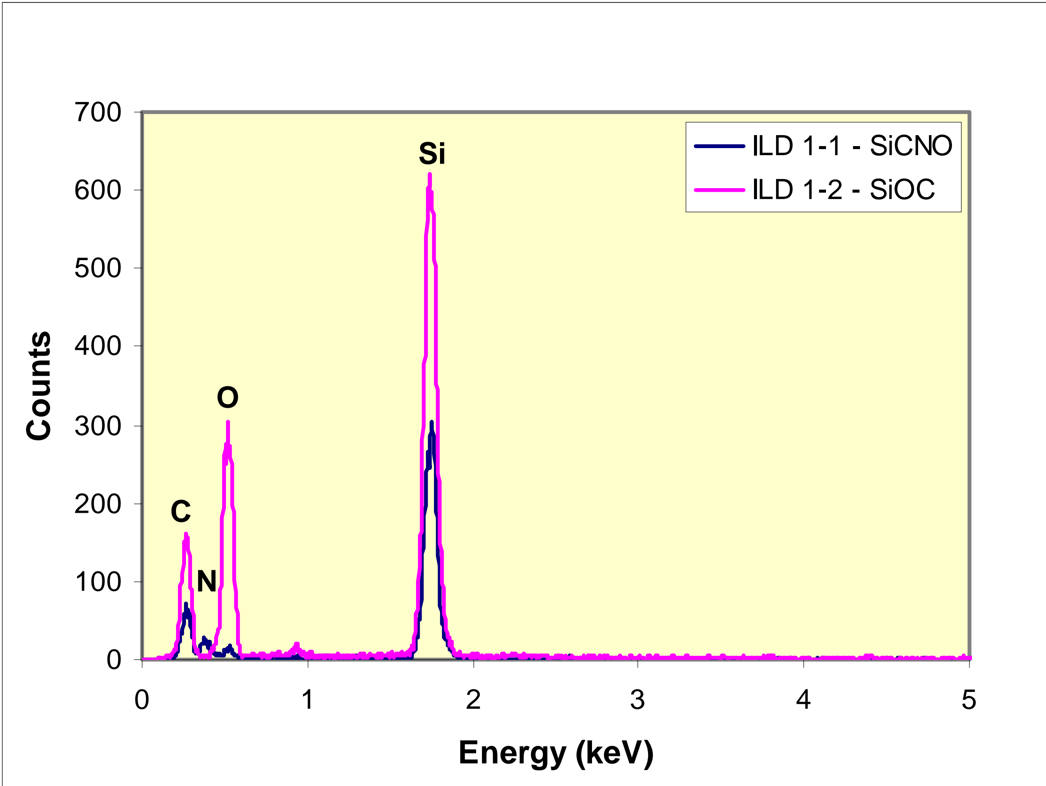

Figure 3.2.17 TEM-EDS Spectra of ILD 1

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Figure 3.2.18 shows the TEM-EDS spectra of the SiON PMD 1, undoped oxide PMD 2, PMD 3 and PMD 4, and SiOC PMD 5.

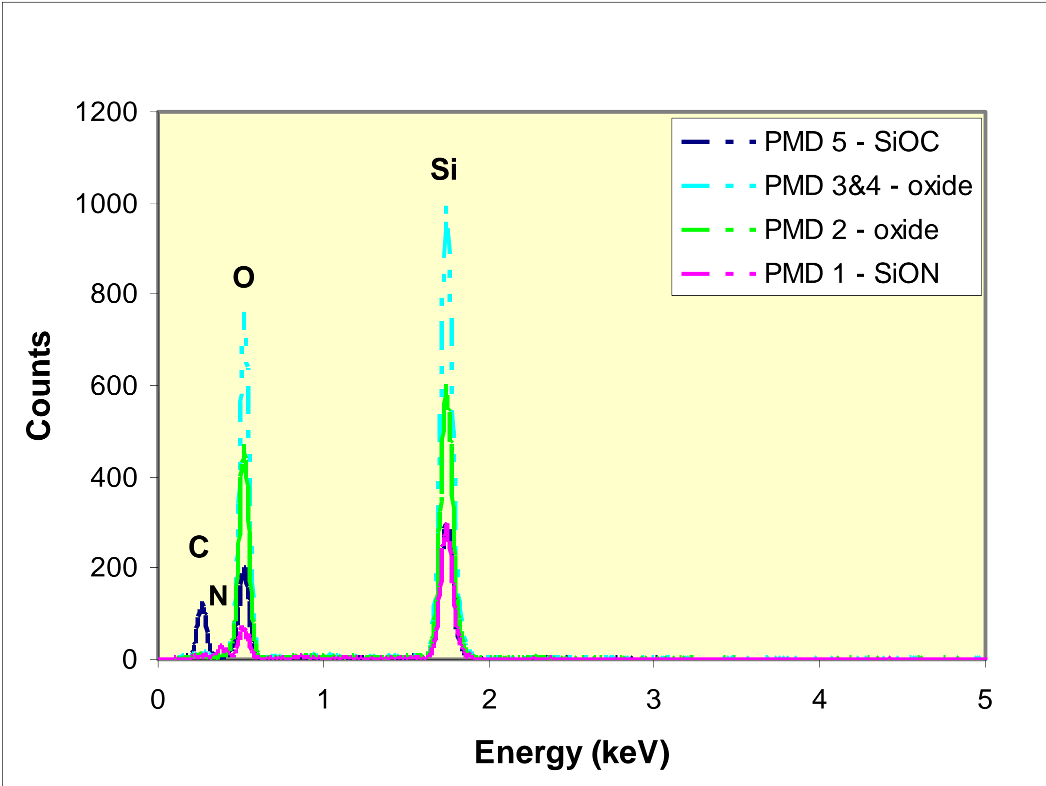

Figure 3.2.18 TEM-EDS Spectra of PMD

3.3 Metallization

The XXXX uses eight levels of damascene Cu for the die interconnect, and a single level of Al for the bond pads and top level busses. Metal 1 is single damascene Cu, while metal 2 through metal 8 are dual damascene Cu. All of the Cu lines use a single Ta-based liner. The Al metal 9 layer uses a TiN/Ti barrier.

Table 3.3.1 and Table 3.3.2 list the metallization vertical and horizontal dimensions, respectively. The minimum pitch metal found on the part is 0.14 µm for metal 1 through metal 5 lines.

The TEM-EDS spectra resulting from the metal line elemental analysis are presented in Figure 3.3.14 through Figure 3.3.16.

Layer	Composition (Top to Bottom)	Layer Thicknesses (µm) (Top to Bottom)	Aspect Ratio
Metal 9	Al/TiN/Ti	1.60 (1.31/0.12/0.17)	0.07
Metal 8	Cu/Ta-based	1.60	1.8
Metal 7	Cu/Ta-based	1.60	1.8
Metal 6	Cu/Ta-based	0.25	1.3
Metal 5	Cu/Ta-based	0.12	1.5
Metal 4	Cu/Ta-based	0.11	1.4
Metal 3	Cu/Ta-based	0.12	1.3
Metal 2	Cu/Ta-based	0.13	1.6
Metal 1	Cu/Ta-based	0.13	1.4

Table 3.3.1 Metallization – Vertical Dimensions

Layer	Width (µm)	Space (µm)	Pitch (µm)
Metal 9	24.0	8.6	32.6
Metal 8	0.92	0.71	1.63
Metal 7	0.92	0.71	1.63
Metal 6	0.19	0.09	0.28
Metal 5	0.08	0.06	0.14
Metal 4	0.08	0.06	0.14
Metal 3	0.08	0.06	0.14
Metal 2	0.08	0.06	0.14
Metal 1	0.09	0.05	0.14

Table 3.3.2 Metallization – Horizontal Dimensions

Figure 3.3.1 shows the 24.0 µm wide, 32.6 µm minimum pitch metal 9 lines. These lines are used for both top level busses and bond pads. The outline of the 12.8 µm minimum pitch via 8s, are also seen.

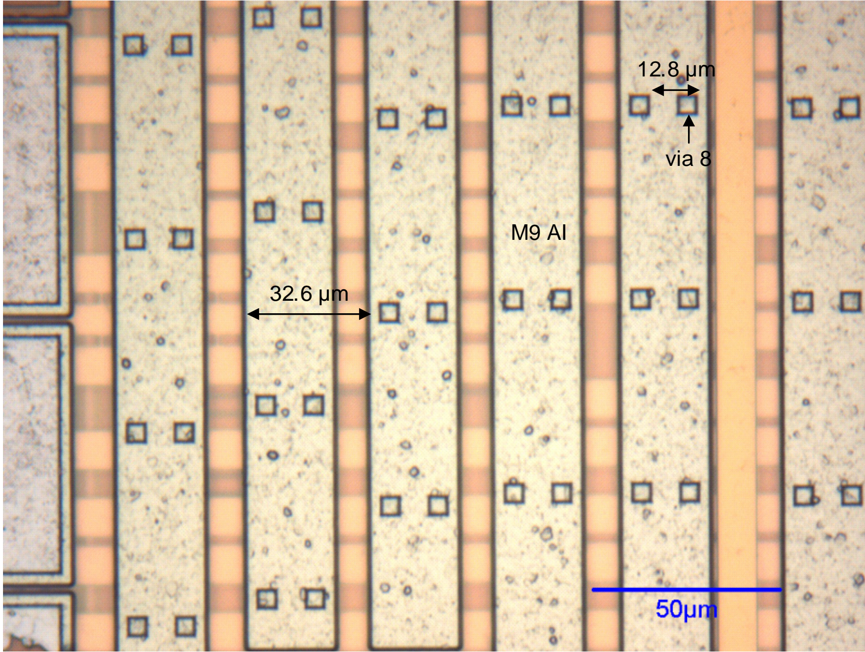

Figure 3.3.1 Minimum Pitch Metal 9

Figure 3.3.2 shows the 1.60 µm thick metal 9. The Al body is 1.57 µm thick. The tops and sides of the metal 9 lines are covered with silicon nitride passivation.

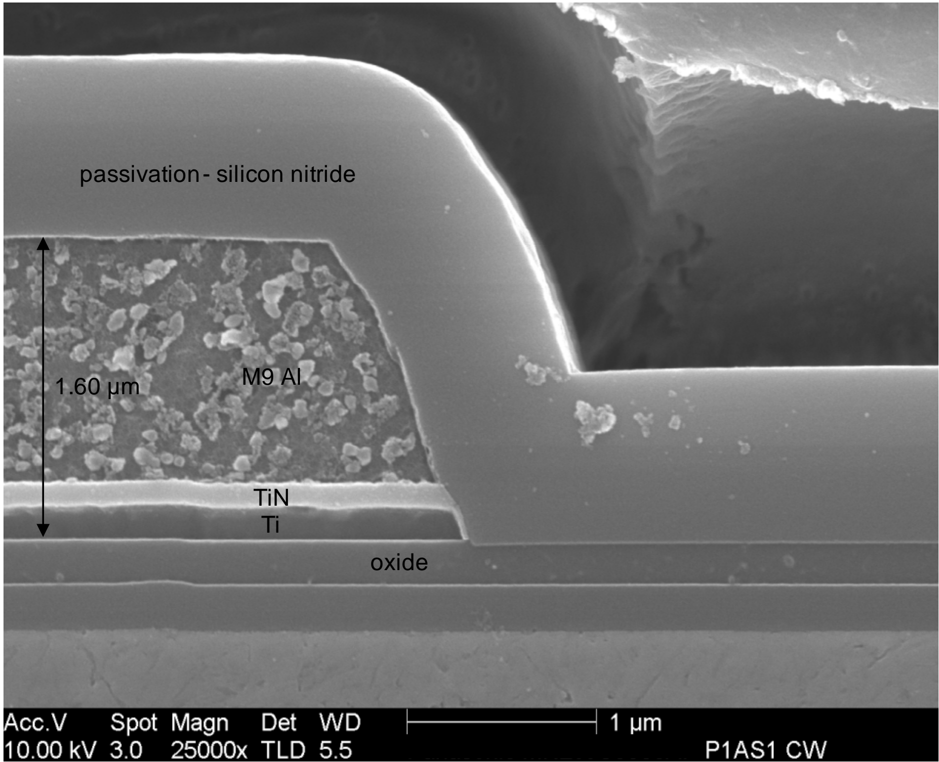

Figure 3.3.2 Metal 9

Figure 3.3.3 shows a TEM image of the 0.12 µm thick metal 9 TiN barrier and the 0.17 µm thick Ti adhesion layer.

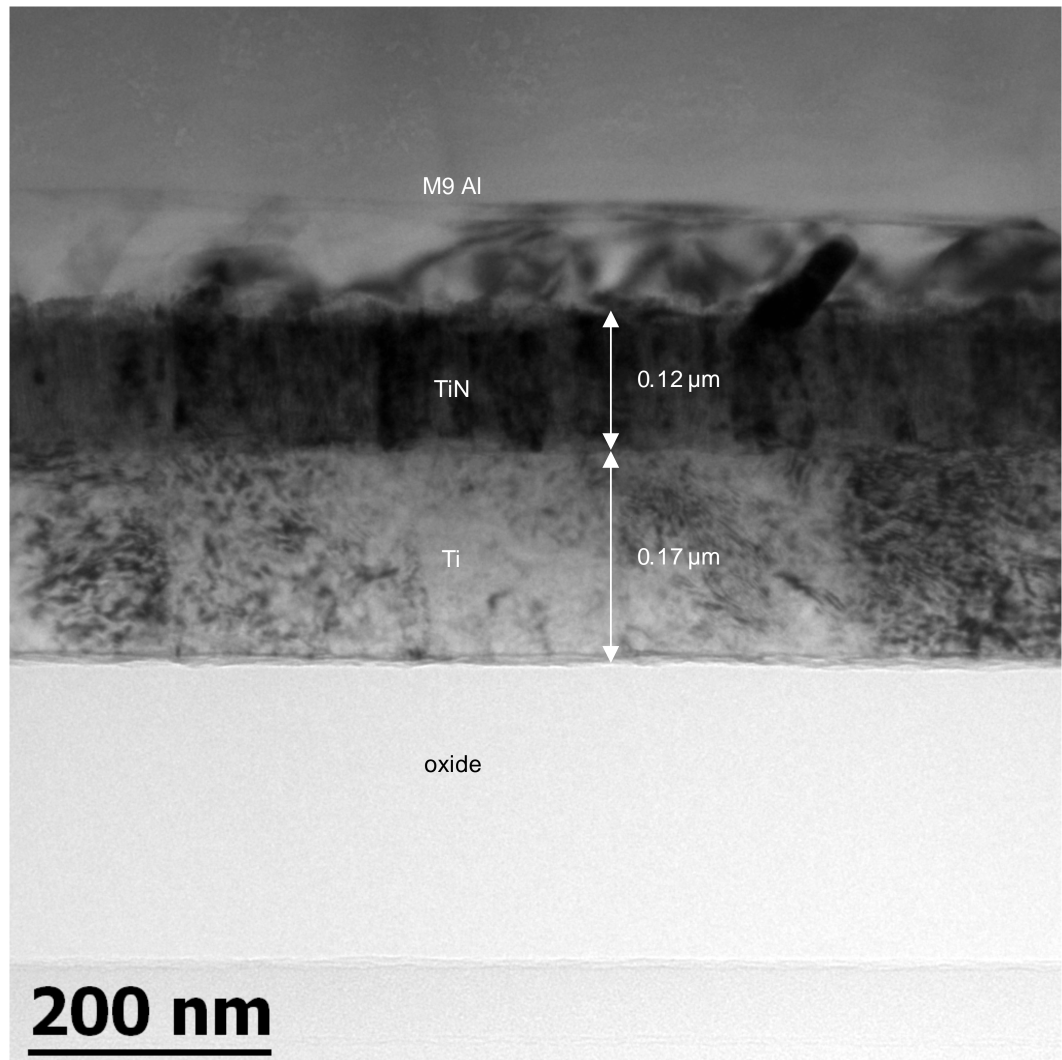

Figure 3.3.3 Metal 9 Barrier – TEM

Figure 3.3.4 shows the 1.63 µm minimum pitch, 1.60 µm thick metal 8 Cu lines. The metal 8 line dielectric is comprised of oxide and FSG. The metal 8 trenches are lined with a Ta-based liner and capped with oxynitride after CMP. A thin SiON trench etch stop layer is used, with the trench etch ending in the oxide via 7 dielectric.

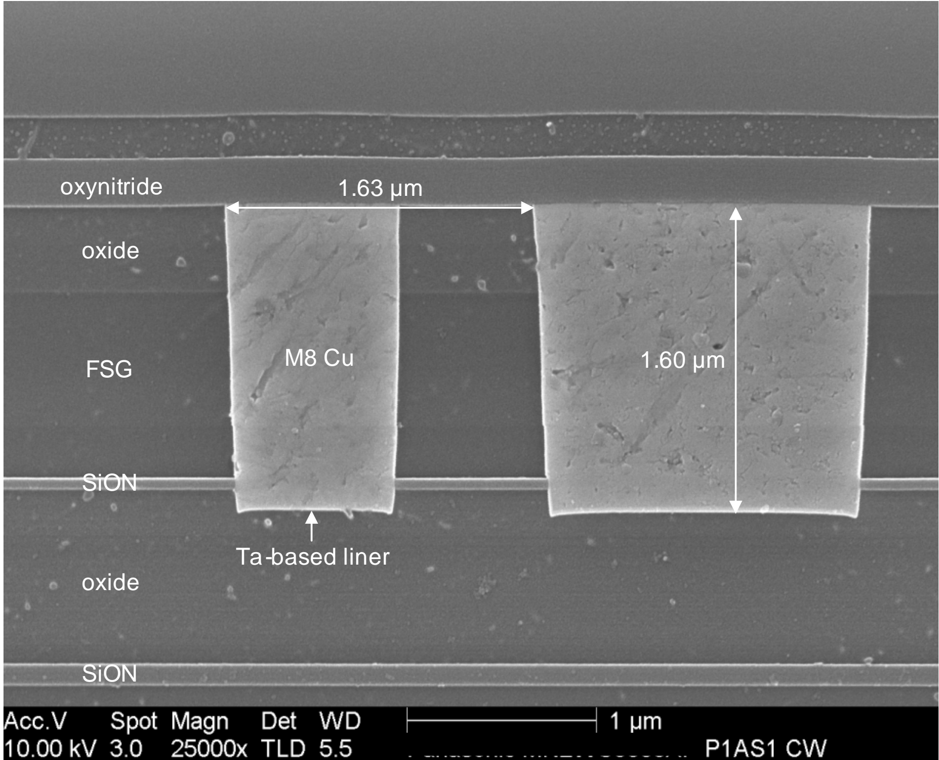

Figure 3.3.4 Minimum Pitch Metal 8

Figure 3.3.5 shows a detailed TEM view of a metal 8 liner. The liner ranges from about 8 nm thick on the sidewalls to about 16 nm thick on the trench bottom. The TEM image density indicates the inner portion of the liner to be crystalline, while the outer portion is amorphous.

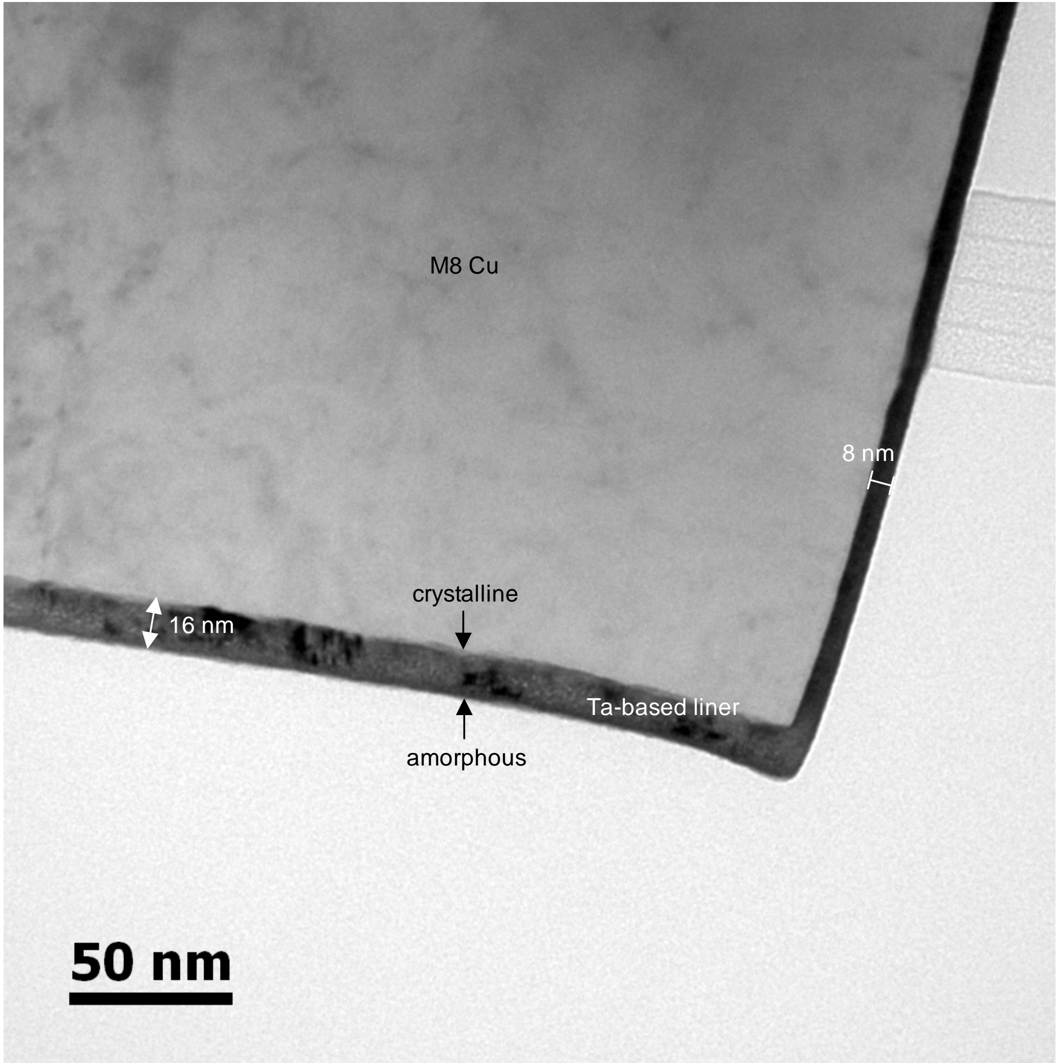

Figure 3.3.5 Metal 8 Liner – TEM

While no minimum pitch metal 7 lines were observed during our cross-sectional analysis, a minimum width metal 7 line is shown in Figure 3.2.1. The metal 7 line shown in the image matches the minimum width metal 8 line, suggesting the same design rule is used for both layers.

Figure 3.3.6 shows the 0.19 µm wide, 0.28 µm minimum pitch metal 6 lines. These lines are 0.25 µm thick. The metal 6 line dielectric is FSG. The metal 6 lines are capped with SiON after CMP. No trench etch stop is used with the timed trench etch ending in the oxide via 5 dielectric.

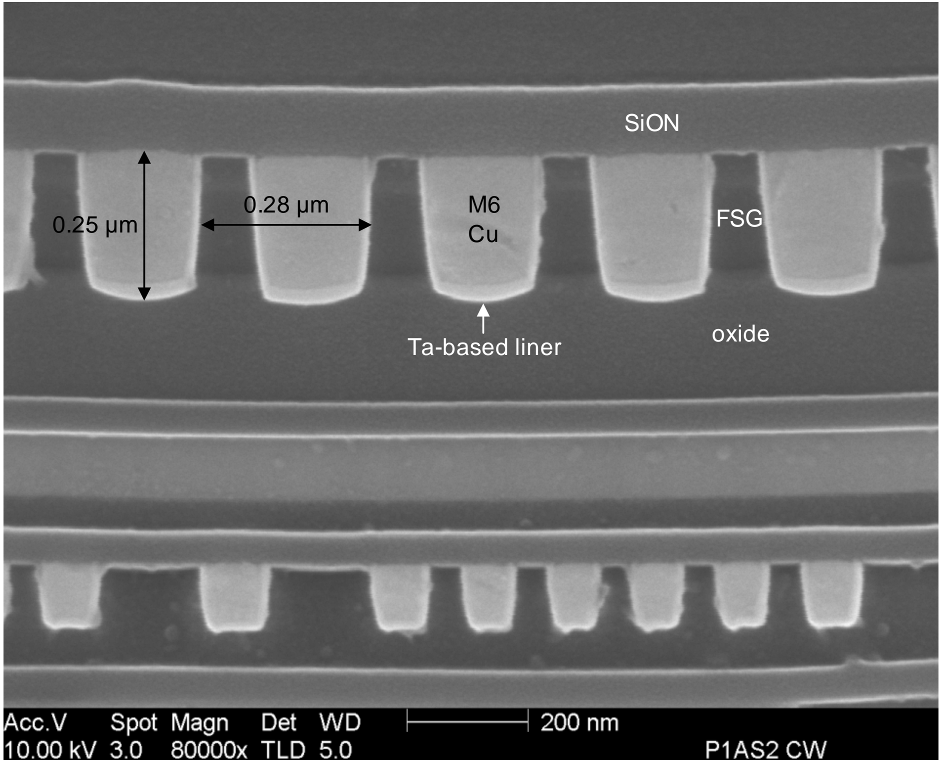

Figure 3.3.6 Minimum Pitch Metal 6

Figure 3.3.7 shows a TEM image of a pair of metal 6 lines. The Ta-based liner is about 8 nm thick on the sidewalls and about 23 nm thick on the trench bottoms.

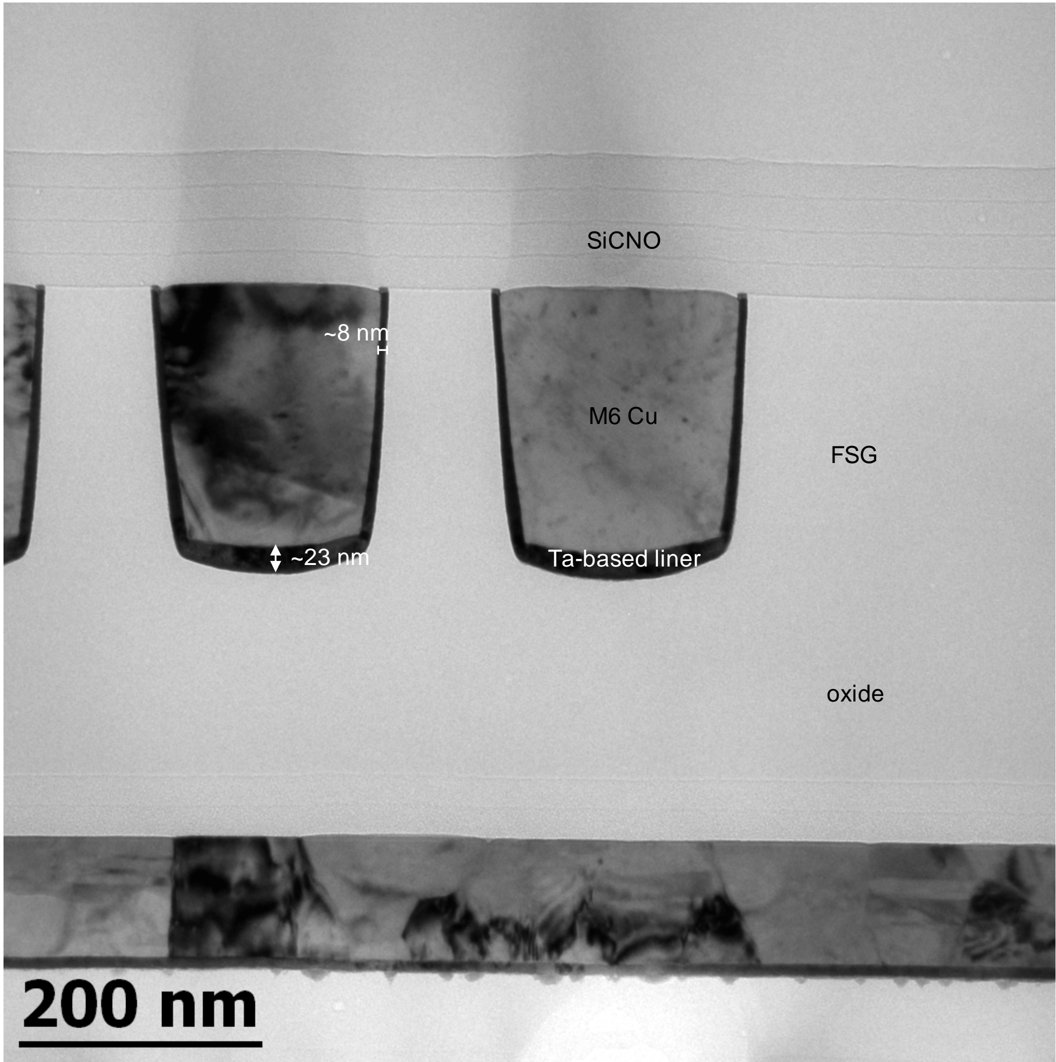

Figure 3.3.7 Metal 6 Liner – TEM

Figure 3.3.8 shows 0.14 µm minimum pitch metal 3 and metal 5 lines. This 0.14 µm metal pitch is used for the metal 1 through metal 5 lines. The metal 2 through metal 5 lines are capped with SiCNO after CMP. A timed etch is used to form the trenches in the SiOC low-k line dielectric.

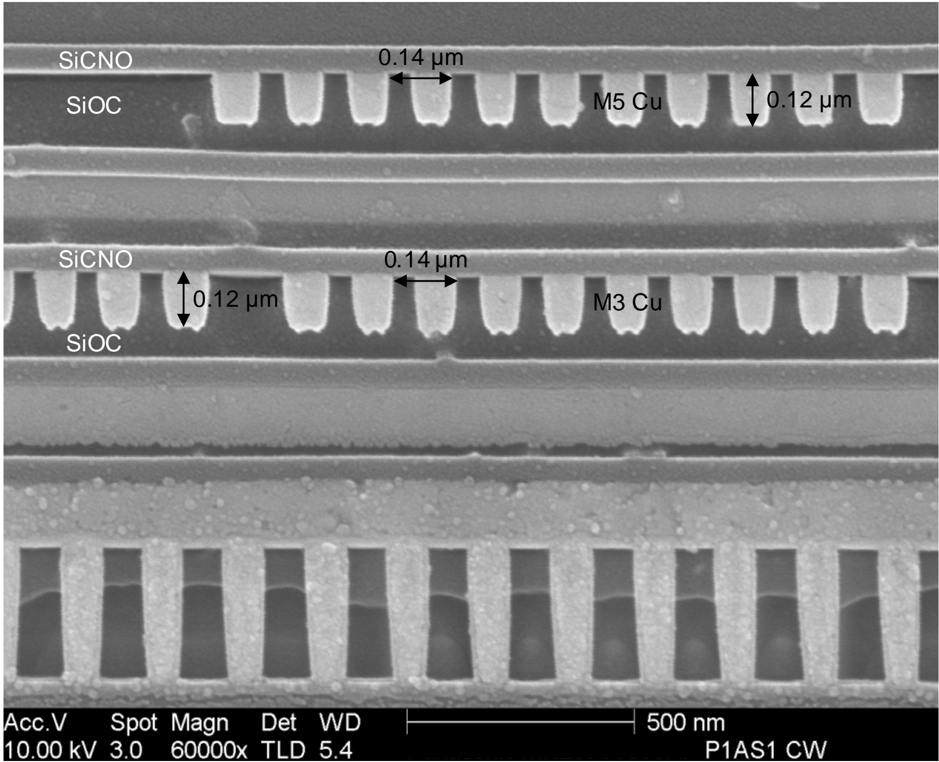

Figure 3.3.8 Minimum Pitch Metal 3 and 5

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