The Current-Carrying Corner Inherent to Trench Isolation

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Abstract—**In this paper it is shown for the first time how the characteristics of the corner MOSFET inherent to trench isolation can be extracted from hardware measurements and how the corner device must be taken into account when extracting MOSFET channel characteristics. For NFET's it is found that the corner's threshold voltage, substrate sensitivity, and sensitivity to well doping are all smaller than the channel's. The results imply that for low standby power logic applications requiring high performance, it may become necessary to locally control the well doping at the corner. However, the corner's reduced substrate sensitivity and width independence can provide a significant advantage in a DRAM cell.**

I. Introduction

LOCOS has been the traditional choice for isolation between devices in past MOSFET technologies [1]. However, as feature sizes are scaled down, trench isolation becomes a more desirable option because it eliminates the LOCOS bird's beak and is fully planar with the silicon surface (as indicated in the insert in Fig. 2) [2]–[4]. Inherent to this geometry are fringing gate fields that enhance carrier inversion within the silicon corner at the isolation edge. As a consequence, there exists a low threshold voltage (V_t) path at the silicon corner that conducts in parallel with the MOSFET channel region [4]–[8]. This parallel current-carrying corner device becomes the dominant MOSFET contributor to standby current in low standby power logic applications and to leakage in DRAM cells. The corner device can even dominate on-currents in applications such as DRAM that require narrow channel widths to achieve high density. Furthermore, there exists concern that the enhanced electric fields due to field crowding at the corner impact dielectric integrity. Hence, there is an immediate need to understand the corner device as we presently develop the ULSI technologies of the future.

In this paper it is shown for the first time how corner MOSFET current characteristics can be extracted from measurements and how the corner device must be taken into account when extracting MOSFET channel characteristics. These concepts are used to explore the control of the corner V_t by varying the p-well boron concentration of an n-channel MOSFET. The implications of the corner device for logic and DRAM applications are discussed.

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II. Results and Discussion

The n-channel MOSFET's (NFET's) built for this experiment are based on the Siemens-IBM 64-Mb DRAM process [9]. The important technology feature for this work is the use of trench isolation. The NFET gate is formed from n^+ polysilicon and gate oxide is 10 nm thick.

In Fig. 1, the saturated drain-to-source current (I_{sat}) for NFET's of equal designed length ($L_{des} = 0.5\ \mu m$) and varying designed widths (W_{des}) is plotted versus gate voltage (V_g) at a drain voltage (V_d) of 3.3 V and a substrate voltage (V_{sx}) of -1 V. A distinct discontinuity in the log (I_{sat})–V_g curves occurs at a gate voltage near the threshold of the channel (V_{tchan}). A similar discontinuity is also observed on log plots of the linear mode current (I_{lin}). Below the V_g where this discontinuity occurs, the current is dominated by width-independent corner conduction while, above it, the channel contributes a significant width-dependent component to the total current. The presence of the corner device is not obvious in the linear plot of I_{sat} nor in the linear plot of I_{lin}. However, the width-independent corner on-current can be clearly identified in the $(I_{sat})^{0.5}$–V_g curves in Fig. 2, where it is evident that the saturated corner current obeys the usual square-law V_g dependence observed at low gate overdrives (V_g–V_t). Thus, the corner-V_t (V_{tcor}) is the gate voltage at which $(I_{sat})^{0.5}$ is extrapolated to be zero. The net transconductance of the two corner devices bounding the NFET channel is proportional to the squared slope ($\gamma_{cor} \cong 8\ \mu A/V^2$) of the $(I_{sat})^{0.5}$–V_g curve in the corner-dominated region. For these devices it was empirically found that the current at the extrapolated V_{tcor} was $\cong 4 \times (0.5\ \mu m/L_{des})$ nA and was independent of V_{sx}.

To first order, V_{tchan} is the voltage at which the width-dependent total current begins to deviate from the extrapolation of the corner current. The total current at V_{tchan} includes a significant corner current $[\gamma_{cor} \times (V_{tchan} - V_{tcor})^2]$ component and a channel current $[40 \times (W_{des}/L_{des})$ nA] component. For the NFET's in Fig. 1, the corner component dominates over the channel component. Therefore, the standard current definition for V_{tchan}

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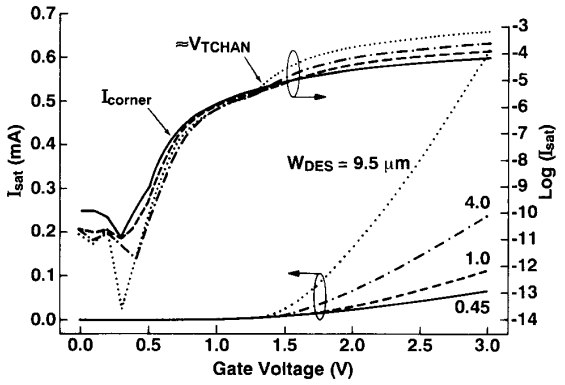

Fig. 1. The corner device current contribution is not obvious in the linear plot of I_{sat}. However, a distinct discontinuity in the log (I_{sat})–V_g curves occurs at a gate voltage near V_{tchan}. ($V_{sx} = -1$ V, $V_d = 3.3$ V).

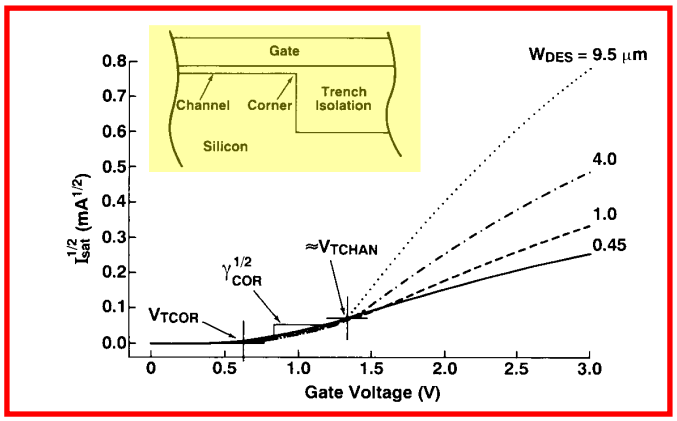

Fig. 2. The width-independent corner on-current can be identified in the $(I_{sat}^{0.5})$–V_g curves. The corner V_t (V_{tcor}) is the gate voltage at which $(I_{sat})^{0.5}$ is extrapolated to be zero.

$[I_{Vt} = 40 \times (W_{des}/L_{des})$ nA] would lead to misleading results, such as predicting that V_{tchan} decreases with width, as illustrated in Fig. 3. The corner must also be taken into account to accurately determine channel widths of the devices in Fig. 1, since its transconductance is comparable to that of a 0.1-μm-wide channel.

The V_{tchan} and V_{tcor} sensitivities to surface-channel V_t-adjust implant dose were determined by using these simple corner characterization concepts and are shown in Fig. 4. Three observations are made: 1) $V_{tcor} < V_{tchan}$; 2) the corner's V_{sx} sensitivity is approximately half the channel's; and 3) the corner's dose sensitivity is much less than the channel's . These results are a consequence of the fringing fields at the silicon corner, which enhance gate control and increase the ratio of the gate capacitance to the depletion capacitance at the corner. Although V_{tcor} was increased from 0.5 to 1 V, V_{tchan} was simultaneously increased from 0.9 to 1.7 V. Thus, it may become necessary to locally increase the doping concentration at the corner above the channel concentration in order to decrease corner off-current without degrading the channel current drive [4].

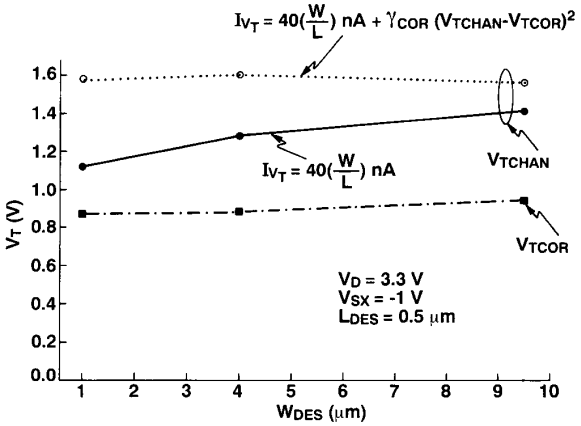

Fig. 3. The extrapolated corner V_t, the traditional channel V_t defined by the current level $I_{vt} = 40 \times (W_{des}/L_{des})$ nA that only accounts for channel current, and the channel V_t defined by the current $I_{vt} = [40 \times (W_{des}/L_{des}) + \gamma_{cor} \times (V_{tchan} - V_{tcor}^2]$ that also accounts for the corner current are plotted versus designed channel width (W_{des}). ($V_{sx} = -1$ V, $V_d = 3.3$ V).

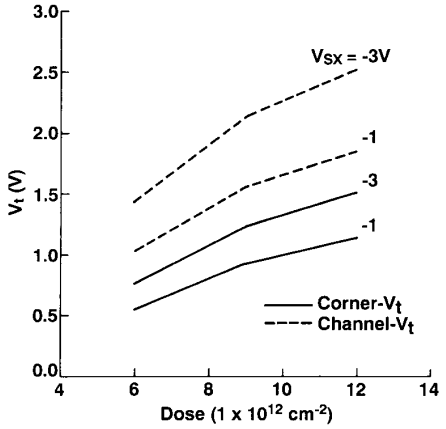

Fig. 4. The measured corner V_t (V_{tcor}) and channel V_t (V_{tchan}) are plotted versus the dose of the surface-channel V_t-adjust 12-keV boron implant. ($V_{sx} = -1$ and -3 V, $V_d = 3.3$ V).

In contrast, the corner device offers advantages in applications such as DRAM's that use narrow devices. First, even at equal V_t's, the corner's contribution to on-current becomes comparable to the channel's and is independent of width variations. For the devices built in this work, the corner would contribute 30% to the total current of a 0.30-μm-wide device. Furthermore, since DRAM cell device currents are limited by the source-follower mode, the corner's weak substrate sensitivity offers an even more significant advantage

III. Summary

To provide a better understanding of the corner MOSFET inherent to trench isolation, it has been shown how corner MOSFET characteristics can be extracted from hardware measurements and how the corner device must

be taken into account when extracting MOSFET channel characteristics. For NFET's it was found that the corner's threshold voltage, substrate sensitivity, and dose sensitivity were all smaller than the channel's. The results implied that, for low standby power logic applications requiring high performance, it may become necessary to locally control the well doping at the corner. However, the corner's reduced substrate sensitivity and width independence can provide a significant advantage in a DRAM cell.

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