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United States Patent [19]

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Corbin, II et al.

[45] Date of Patent: Mar. 17, 1992

- [54] METHOD AND APPARATUS FOR DESIGNING INTEGRATED CIRCUITS 4,500,963 2/1985 Smith et al. 364/488
- 4,554,625 11/1985 Otten 364/491
- 4,577,276 3/1986 Dunlop et al. 364/491
- [75] Inventors: Ludlow V. Corbin, II; Steven G. Danielson, both of Seattle; Richard E. Oettel, Bellevue; Mark E. Rossman, Redmond; James E. Thiele, Seattle, all of Wash. 4,580,228 4/1986 Note 364/300
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- 4,667,290 5/1987 Goss et al. 364/300
- [73] Assignee: Cascade Design Automation Corporation, Bellevue, Wash. 4,700,317 10/1987 Watanabe et al. 364/488

Primary Examiner—Parshotam S. Lall
 Assistant Examiner—V. N. Trans
 Attorney, Agent, or Firm—Seed and Berry

- [21] Appl. No.: 374,485
- [22] Filed: Jun. 29, 1989

[57] ABSTRACT

A method and apparatus for determining integrated circuit layouts from a virtual circuit description and specification of a technology. Starting with high-level descriptions of a circuit, a virtual geometric description of the circuit is developed using a virtual grid described in terms of reference points relative to a substrate surface. The relationships among the reference points are expressed as fractions of variables that can also be used to define the design rules. When the technology is specified, the relationships among the reference points is determined, as in the layout of the integrated circuit.

Related U.S. Application Data

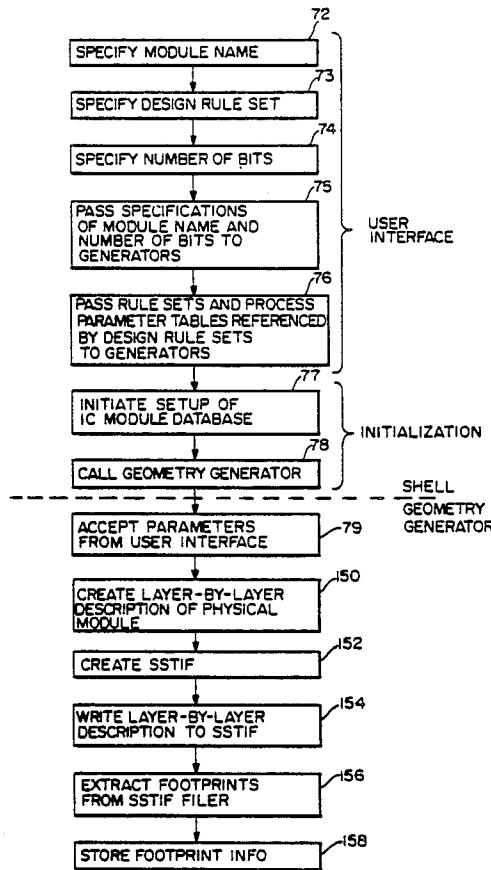
- [63] Continuation of Ser. No. 917,917, Oct. 10, 1986, abandoned.
- [51] Int. Cl.⁵ G06F 15/60
- [52] U.S. Cl. 364/491; 364/490; 364/489; 364/488
- [58] Field of Search 364/488, 489, 490, 491, 364/200

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- H 354 10/1987 Rubin 364/491

16 Claims, 9 Drawing Sheets



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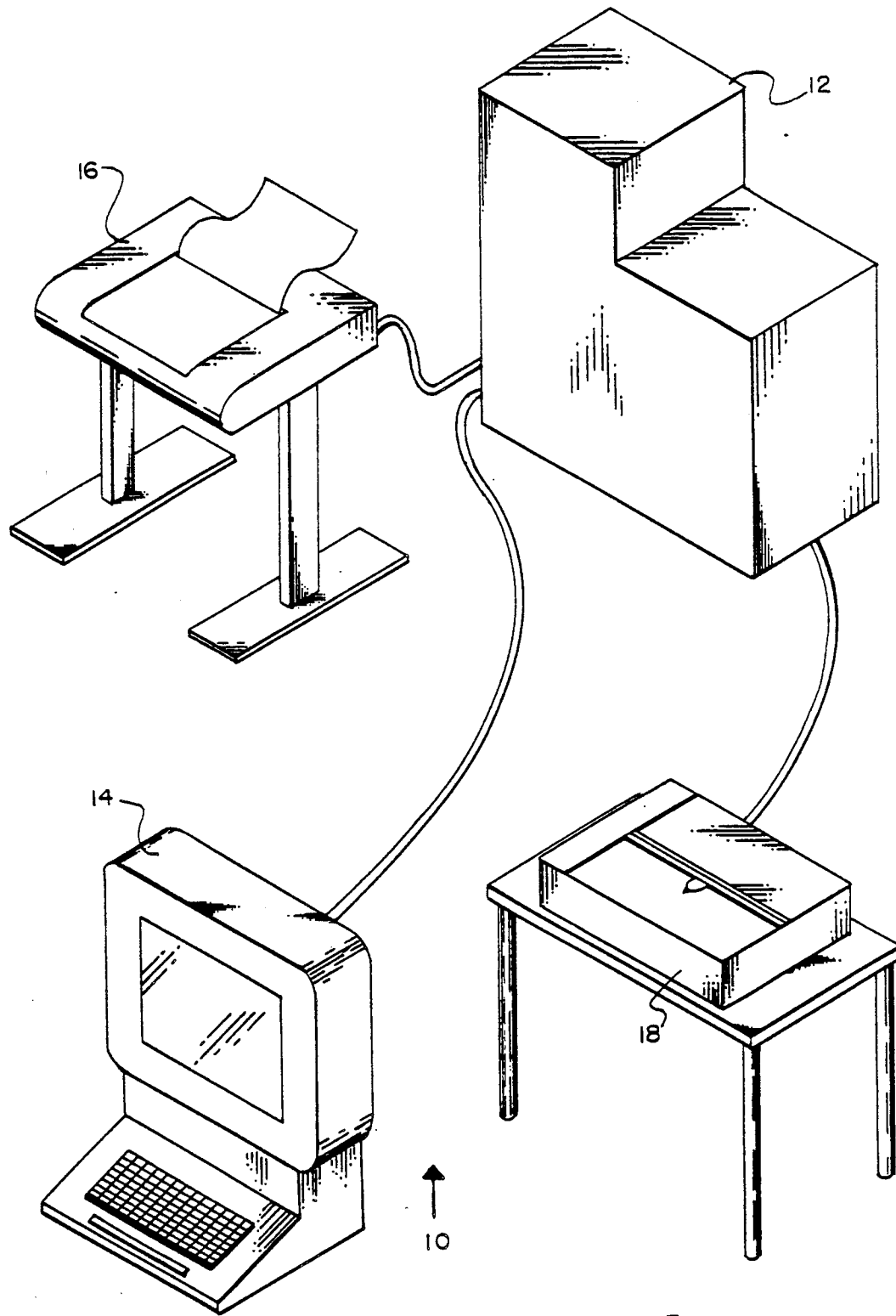


FIG. 1

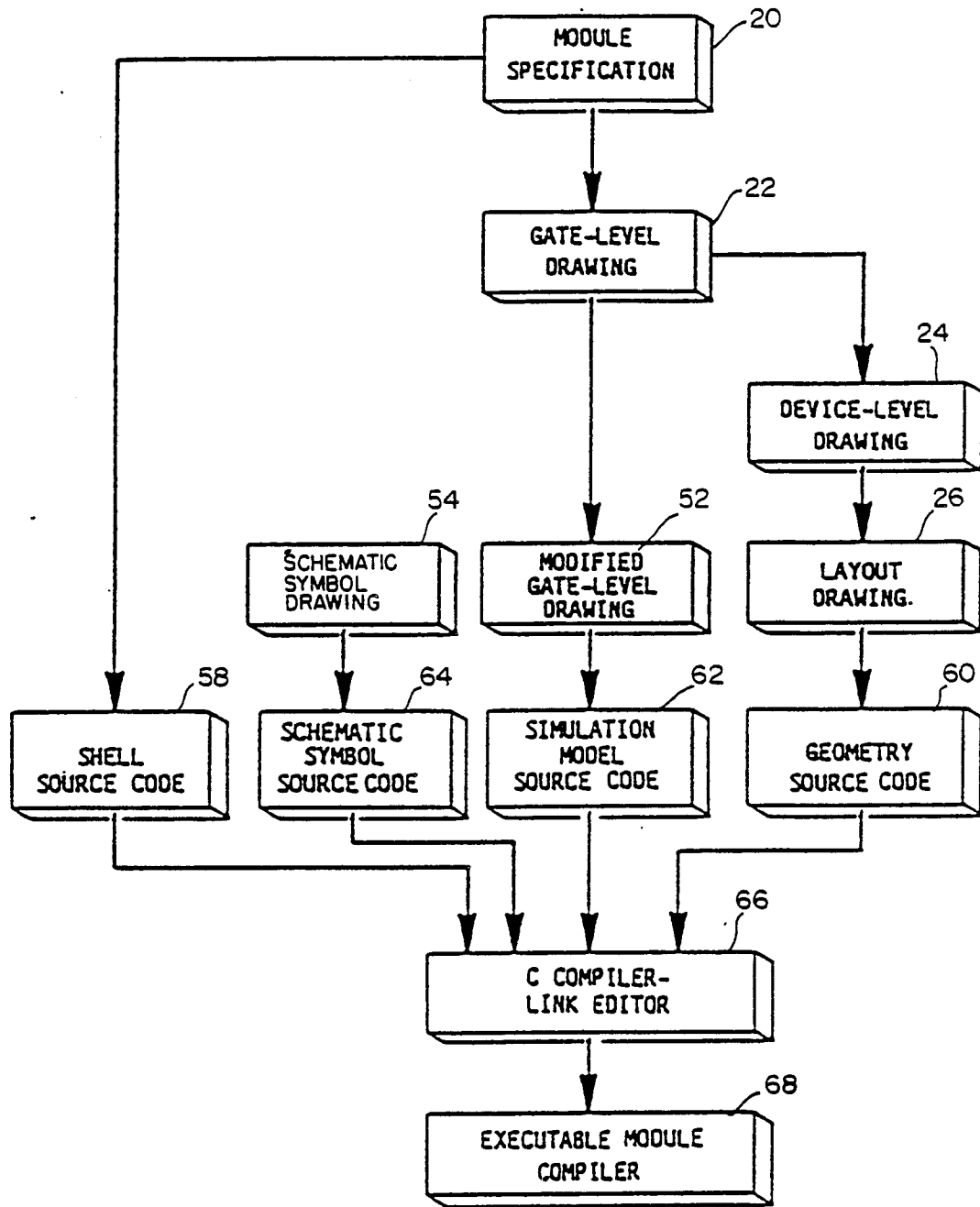


FIG. 2

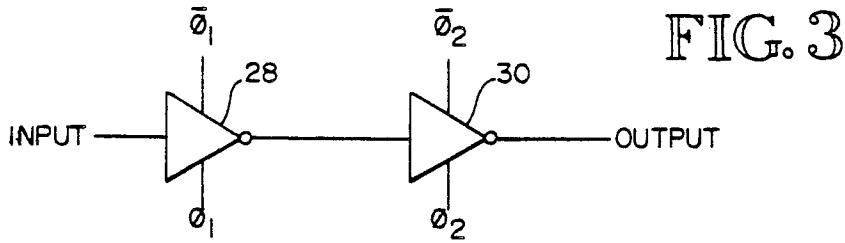


FIG. 3

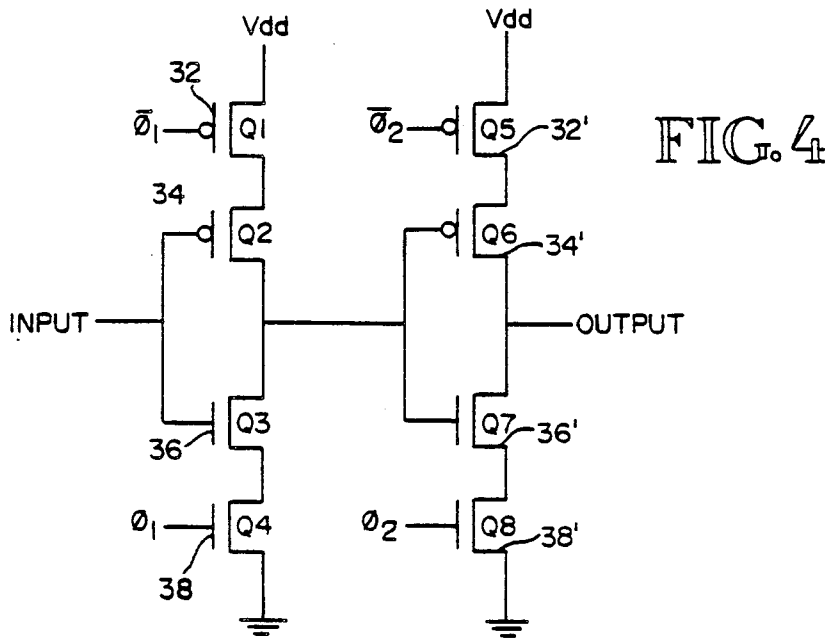
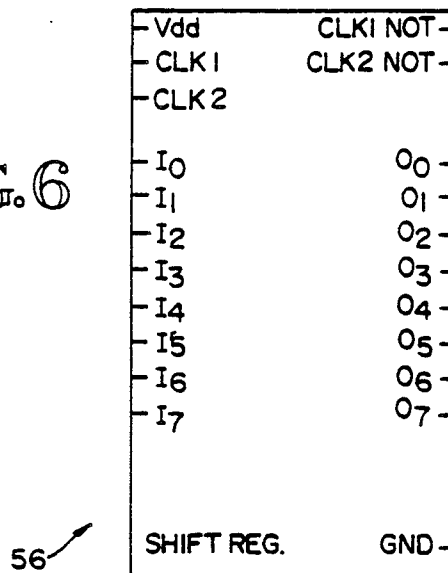


FIG. 4

FIG. 6



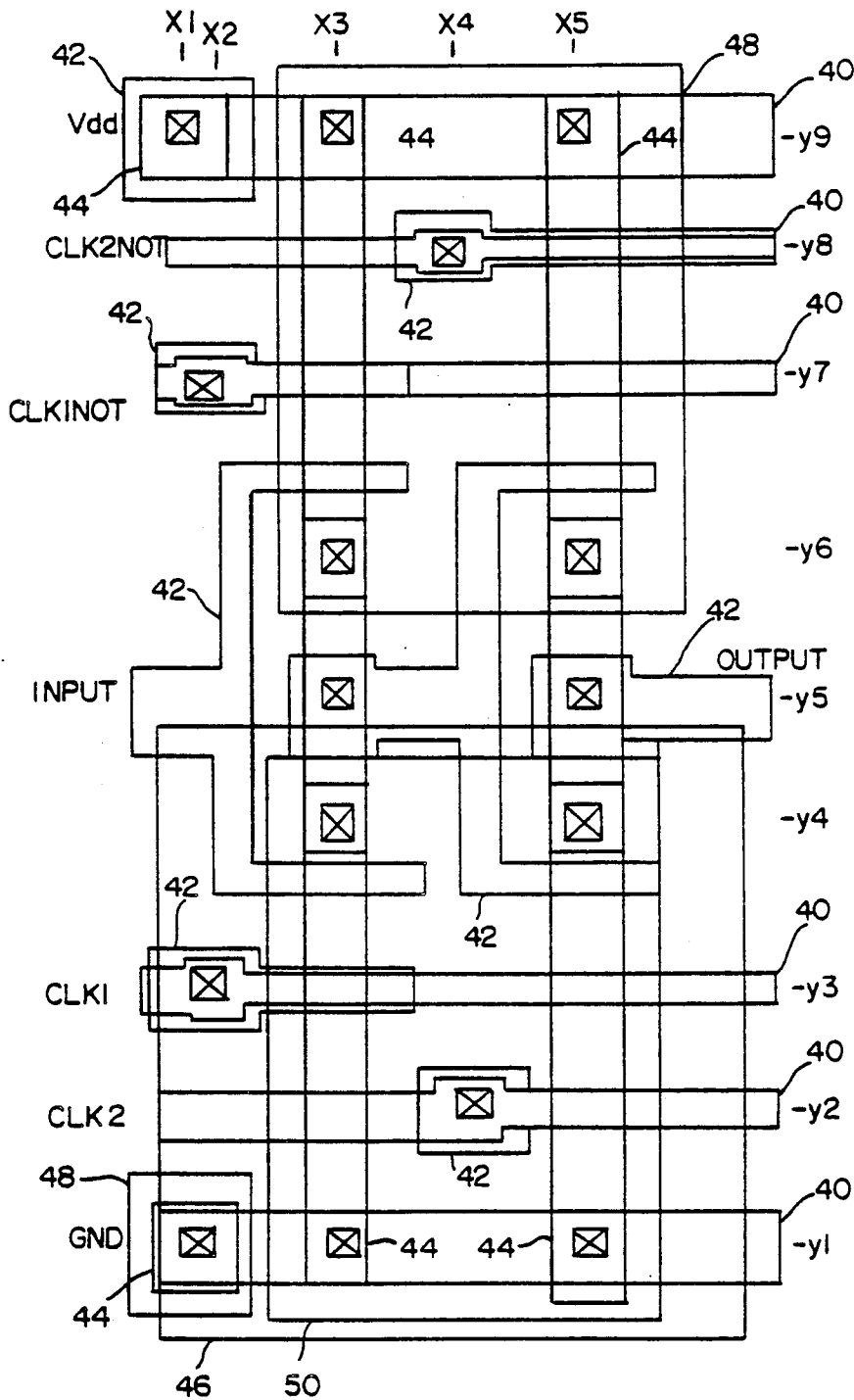


FIG. 5

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