

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,  
Petitioner,

v.

GODO KAISHA IP BRIDGE 1,  
Patent Owner.

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Case IPR2016-01246<sup>1</sup>  
Patent 7,126,174 B2

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**PETITIONER'S OBJECTIONS TO PATENT OWNER'S EVIDENCE  
SUBMITTED DURING THE PRELIMINARY PROCEEDING**

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<sup>1</sup> Case IPR2016-01247 has been consolidated with this proceeding.

In accordance with 37 C.F.R. § 42.64(b)(1), Petitioner Taiwan Semiconductor Manufacturing Company, Ltd. hereby submits a list of objections to Patent Owner IP Bridge's Exhibits 2001 through 2011 submitted during the preliminary proceeding, identified in the chart below:

<b>Exhibit Number</b>	<b>Description</b>
2001	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner's Preliminary Response filed in IPR2016-01246 on October 5, 2016
2002	Schematic illustration of the Chemical Mechanical Polishing process from Steigerwald, Murarka, and Gutmann, <i>Chemical Mechanical Planarization of Microelectronic Materials</i> (1997).
2003	Schematic illustration of the Chemical Mechanical Polishing process from the Motorola Company. SCSolutions.com. Accessed September 30, 2016. <a href="http://www.scsolutions.com/chemical-mechanicalplanarization-cmp-controllers-0">http://www.scsolutions.com/chemical-mechanicalplanarization-cmp-controllers-0</a>
2004	Photograph of a Chemical Mechanical Polishing Tool from the Applied Materials Company. BusinessWire.com. Accessed October 5, 2016. <a href="http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion">http://www.businesswire.com/news/home/20040711005007/en/Applied-Materials-Revolutionizes-Planarization-Technology-Breakthrough-Reflexion</a>
2005	Troxel, Boning, McIlrath "Semiconductor Process Representation." <i>Wiley Encyclopedia of Electrical and Electronics</i> , pp. 139 –147 (1999).
2006	U.S. Patent No. 6,052,319 to Jacobs
2007	U.S. Patent No. 6,952,656 to Cordova et al.
2008	Hunt, "Low Budget Undergraduate Microelectronics Laboratory." <i>University Government Industry Microelectronics Symposium</i> , pp. 81-87 (2006).
2009	U.S. Patent No. 7,074,709 to Young

Exhibit Number	Description
2010	Burckel, “3D-ICs created using oblique processing.” <i>Advances in Patterning Materials and Processes XXXIII</i> , pp. 1–12 (2016).
2011	Declaration of Dr. E. Fred Schubert, Ph.D. in support of Patent Owner’s Preliminary Response filed in IPR2016-01247 on October 7, 2016

**I. Objection to Paragraphs 33–159 of Patent Owner’s Exhibit 2001 and Paragraphs 33–149 of Patent Owner’s Exhibit 2011—Unreliable “Expert” Testimony**

Petitioner objects to Exhibits 2001 and 2011 because they contain unreliable testimony under Fed. R. Evid. 702 and *Daubert v. Merrell Dow Pharm., Inc.*, 509 U.S. 579 (1993). Dr. Schubert’s declaration includes numerous purported “expert” opinions on matters for which Dr. Schubert has failed to establish himself as an expert. Based on paragraphs 13–21 of Ex. 2001 and Ex. 2011,<sup>2</sup> Dr. Schubert has not established himself as someone possessing sufficient knowledge, skill, experience, training, and/or education regarding LDD (lightly doped drain) MOSFETs. Although he may have experience with III-V compound

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<sup>2</sup> Dr. Schubert claims to have included his *curriculum vitae* as “Exhibit A” to Ex. 2001 and Ex. 2011, but no “Exhibit A” appears to have been filed or served on Petitioner.

semiconductors and light-emitting devices,<sup>3</sup> such devices are vastly different from the LDD Si MOSFET devices at issue in these proceedings.

Dr. Schubert does not claim to have significant experience designing or making LDD Si MOSFET devices, let alone during the relevant time period.<sup>4</sup>

Nevertheless, Dr. Schubert repeatedly opines about the understanding of a person of ordinary skill in the art during the relevant period with respect to LDD Si MOSFET devices.

## **II. Objection to Patent Owner's Exhibits 2002, 2003, 2004, 2005, 2008, and 2010—Failure to Authenticate**

Patent Owner has not submitted evidence to authenticate Exhibits 2002, 2003, 2004, 2005, 2008, and 2010, making them inadmissible under Fed. R. Evid. 901.

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<sup>3</sup> See, e.g., Ex. 2001 & 2011 at ¶¶ 14–16; <https://www.rpi.edu/dept/cfes/researchers/Fred%20Schubert.html> (last visited Jan. 7, 2017).

<sup>4</sup> Although MOSFETS may be included in some of the subject matter of courses taught by Dr. Schubert, he provides no evidence regarding the type of information taught relative to MOSFETs, the depth of its treatment, or why mere inclusion of MOSFETs in a course establishes him as an expert relative to the design and fabrication of LDD MOSFETs (or even one of ordinary skill in the art).

**III. Objection to Patent Owner's Exhibits 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, and 2010—Improper Incorporation By Reference**

Neither of Patent Owner's Preliminary Responses cites Exhibits 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, or 2010; they only appear in Dr. Schubert's declarations (Exhibits 2001 and 2011), and therefore are improperly incorporated by reference in violation of 37 C.F.R. § 42.6(a)(3).

**IV. Objection to Patent Owner's Exhibits 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, and 2010—Irrelevant and Non-Probative Evidence**

Patent Owner's Exhibits 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, and 2010 are irrelevant to any material facts at issue in these proceedings, and any probative value Patent Owner may try to assign them is substantially outweighed by their tendency to confuse the issues, mislead the Board, waste time, and needlessly present cumulative evidence. These exhibits are therefore inadmissible under Fed. R. Evid. 401, 402, and 403.

Citations to Exhibits 2002, 2003, and 2004 appear only in footnotes to paragraph 61 of Dr. Schubert's declarations (Exhibits 2001 and 2011). Paragraph 61 of both declarations reads, in its entirety, as follows:

61. CMP is a process that includes a polishing pad that is soaked with a chemical solution. The semiconductor wafer is slightly pressed onto the polishing pad. The semiconductor wafer and polishing pad are subjected to rotating motions to ensure uniformity of the CMP process. CMP includes a chemical-etching component and a

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