United States Patent [19]

Niu et al.

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[54] **NETWORK INTERFACE DEVICE ARCHITECTURE FOR STORING TRANSMIT AND RECEIVE DATA IN A RANDOM ACCESS BUFFER MEMORY ACROSS INDEPENDENT CLOCK DOMAINS**

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[73] Assignee: **Advanced Micro Devices, Inc.,** Sunnyvale, Calif.

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[22] Filed: **Sep. 3, 1998**

[51] Int. Cl.^{7} **G06F 13/36**; G06F 13/12; G06F 15/76; H04L 12/54; H04L 12/413

[52] U.S. Cl. **710/129**; 710/52; 710/56; 710/57; 710/58; 710/60; 710/130; 709/213; 709/234; 709/236; 714/805; 714/811

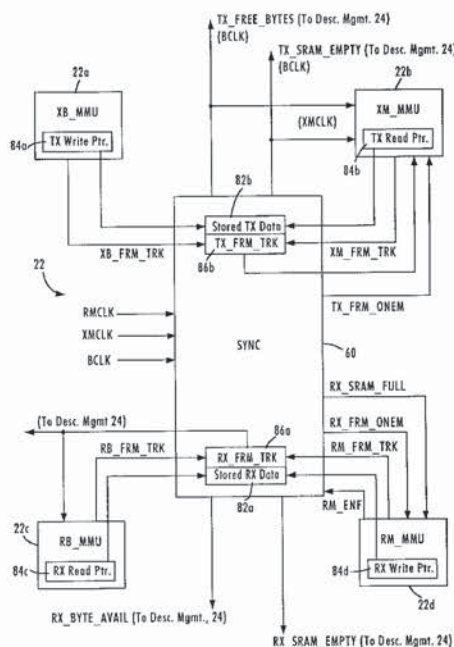[58] Field of Search 710/61, 52, 56, 710/57, 58, 60, 129, 105, 130; 713/400, 600; 709/213, 234, 236; 712/32; 714/805, 811; 370/381, 517, 463

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Primary Examiner—Thomas C. Lee
Assistant Examiner—Katharina Schuster

[57] **ABSTRACT**

A network interface device includes a random access transmit buffer and a random access receive buffer for transmission and reception of transmission and receive data frames between a host computer bus and a packet switched network. The network interface device includes a memory management unit having read and write controllers for each of the transmit and receive buffers, where each write controller operates in a clock domain separate from the corresponding read controller. The memory management unit also includes a synchronization circuit that controls arbitration for accessing the random access memories between the read and write controllers. The synchronization circuit asynchronously monitors the amount of data stored in the random access transmit and receive buffer by asynchronously comparing write pointer and read pointer values stored in gray code counters, where each counter is configured for changing a single bit of a counter value in response to an increment signal. A descriptor management unit is used to control DMA reading and writing of transmit data and receive data from and to system memory, respectively, based on descriptor lists, respectively. A pipelining architecture also optimizes transfer of data between the buffers, the PCI bus, and the media access controller.
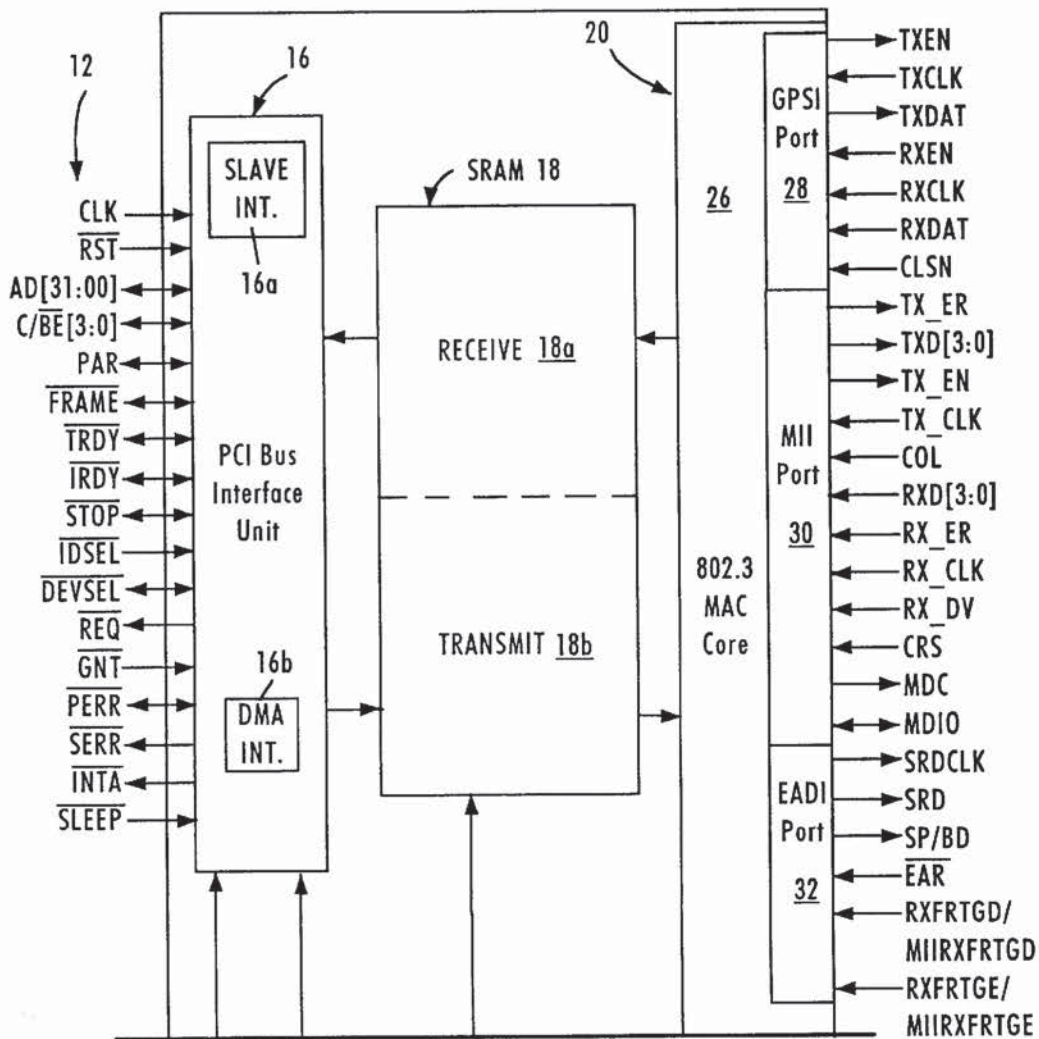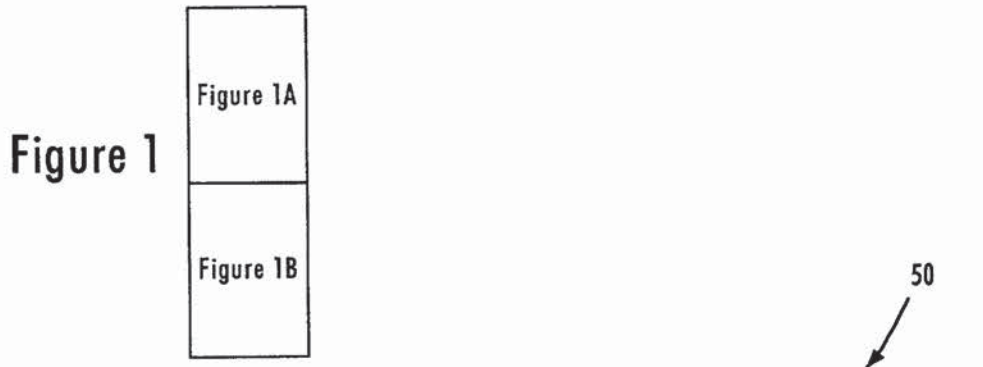
38 Claims, 11 Drawing Sheets

Figure 1

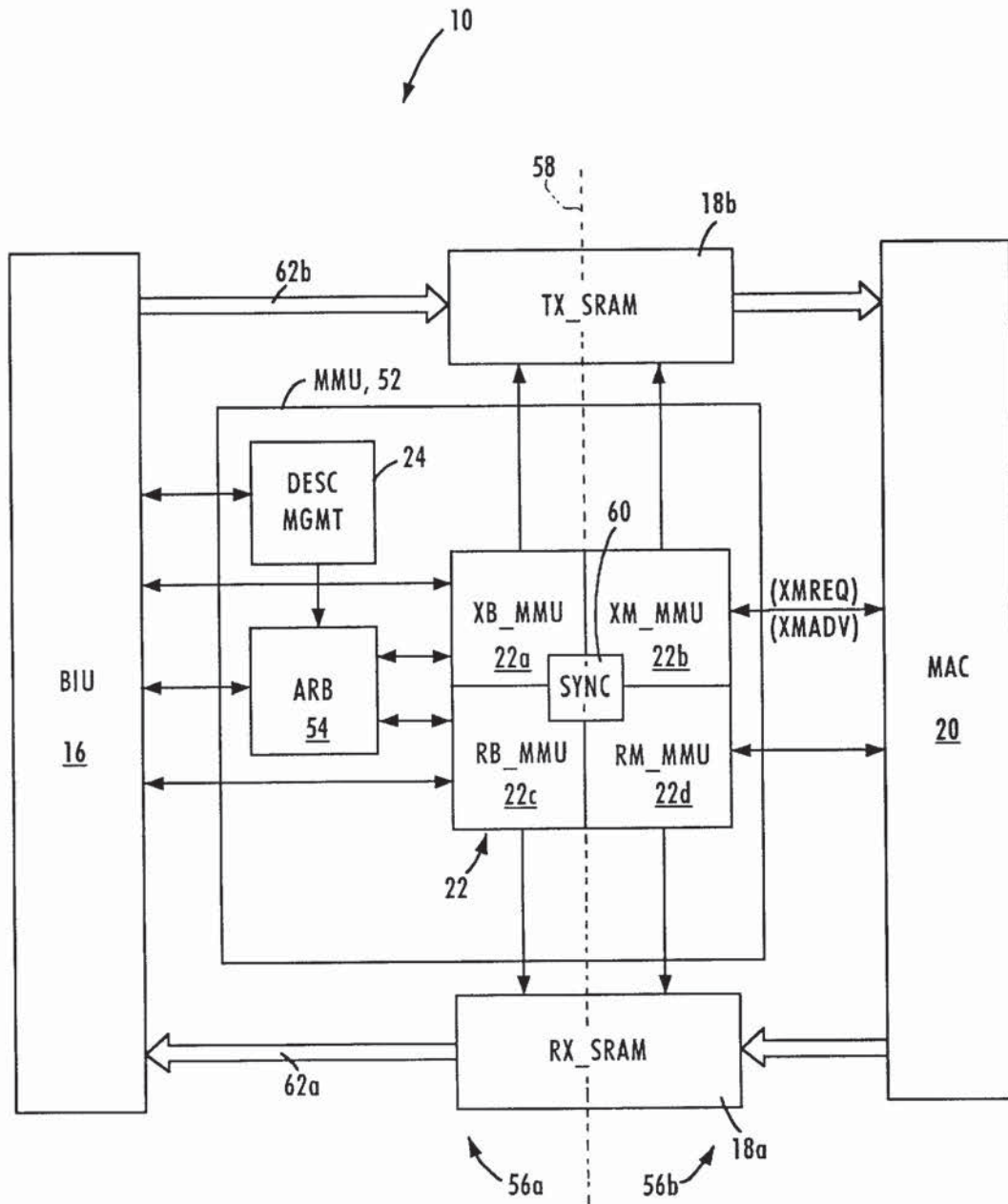| Figure 1A |
|-----------|
| Figure 1B |
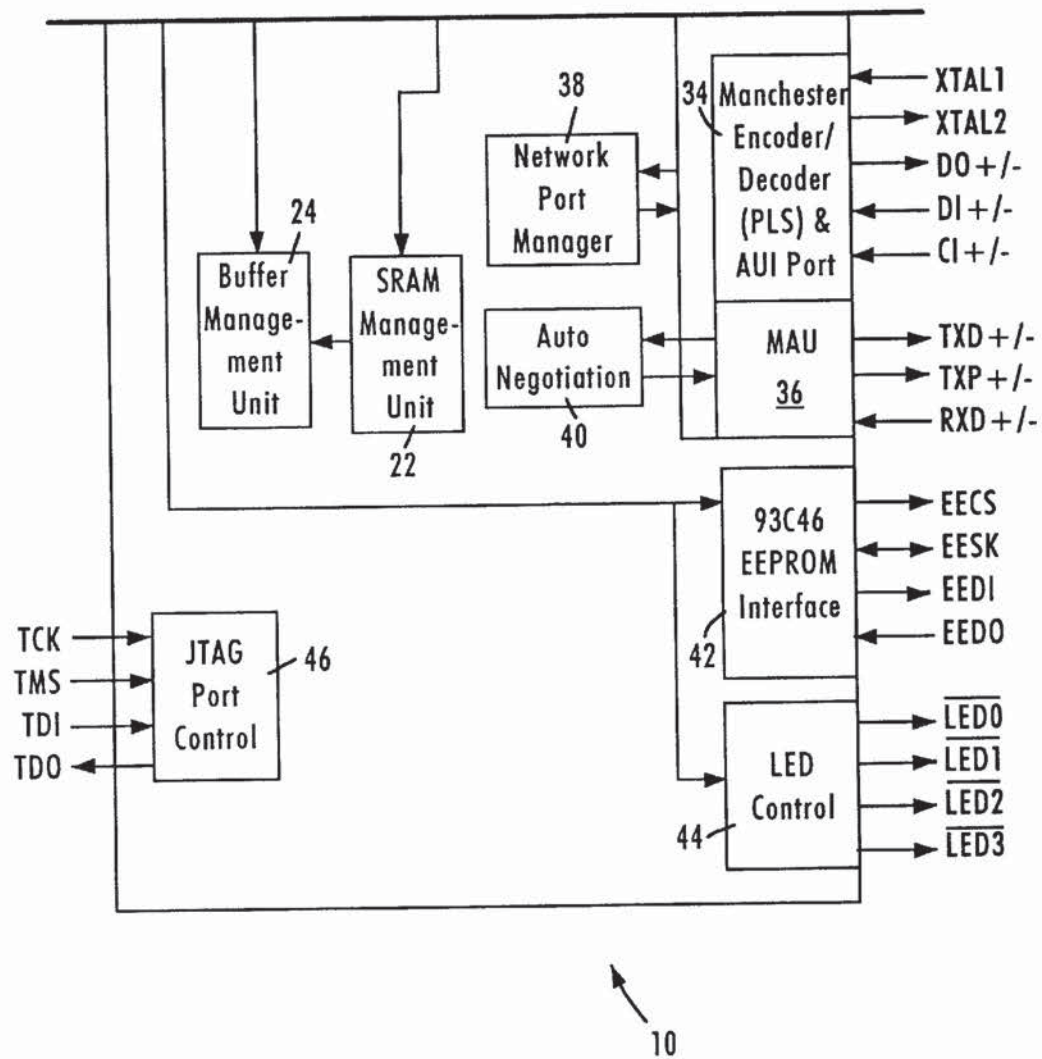
Figure 1A

Figure 1B

Figure 2

Figure 3

Figure 6

DOCKET ALARM
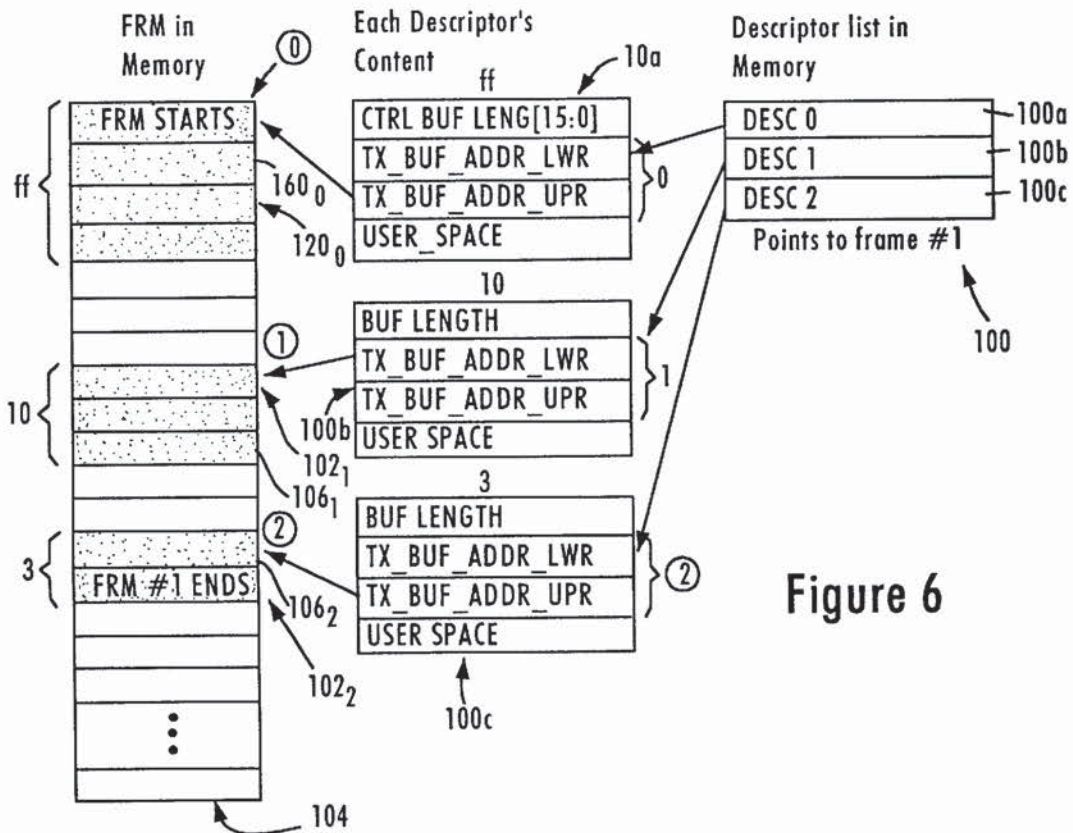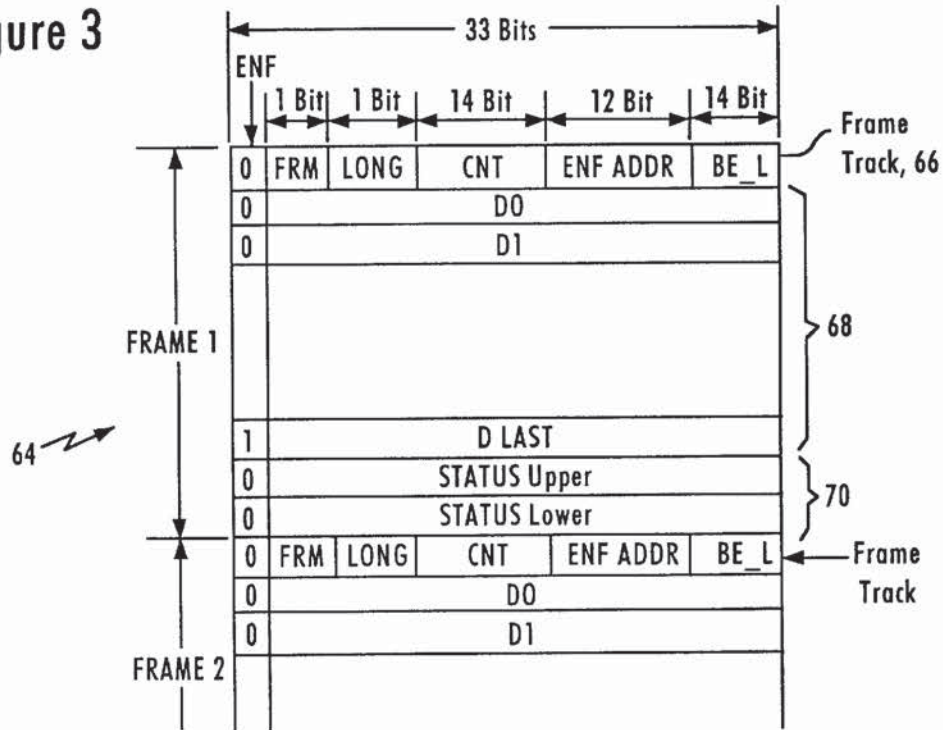
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