UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Panasonic Inc., *et al.*,
Petitioners

v.

Papst Licensing GMBH & CO. KG,
Patent Owner

Case No: IPR2016-01213
U.S. Patent No. 8,504,746

SECOND DECLARATION OF DR. PAUL F. REYNOLDS

I, Dr. Paul F. Reynolds, Ph.D., declare as follows:

1.   I am providing this declaration in support of Petitioners' Reply to address issues raised by the Patent Owner in its Response (Paper 17) for IPR 2016-01213.

2.   In addition to the information considered in connection with my original declaration, I also have considered the Board's Decisions on Institution, the Patent Owner's Response and exhibits, and the deposition testimony of Patent Owner's expert.

I.   Yamamoto's System Control Circuit 20

3.   In its response, Patent Owner asserts that "Yamamoto does not disclose that its system control circuit 20 is involved in transferring data from the hard disk to a computer." Response at 18-19. In my opinion this is incorrect. The flow chart in Fig. 31 of Yamamoto describes a program running in the system control circuit 20 ("SCC") that manages the operating modes of the Yamamoto camera (Ex. 1401, Col. 22:36-37). A POSITA would have understood that as part of the process at Step 106 of setting the camera in external hard disk mode, the SCC 20 would output control signals to control the operation of interface circuit 65 and R/D control circuit 66 to cause those circuits to enable data transfer from the hard disk 71 to an external computer.   (Ex. 1401, Col. 7:60-64 and Cols. 22-23).

4.	A POSITA would have also understood that when in external hard disk mode, SCC 20 would prevent other circuits of the camera from accessing hard disk 71, to prevent access conflicts, because of all of the other operations it already performs: SCC 20 monitors the operation of mode switch 19, it monitors for the presence of an external computer that could request access to the (possibly emulated—*see* SCSI emulation, *infra*) hard disk (Ex. 1401, col. 23:30-43), and it manages timing of writes to the hard disk (*e.g.*, Ex. 1401, Fig. 23 and col. 18:37-19:10; Fig. 26 and col. 20:59-21:27). Additionally, a POSITA would have understood that SCC 20 would also prevent the other camera circuits from sending image data directly from the optical image processing circuitry to the external computer as they would in scanner mode. (*See* Ex. 1401, Col. 23:4-22). For example, Yamamoto discloses that when in hard disk mode a SET WINDOW command, which is permitted during scanner mode operation, "can not be received by the still video camera, so that the scanning operation and the trimming operation are prohibited." (Ex. 1401, Col. 23:40-43). A POSITA would have understood that SCC 20, "control[ling] the still video camera as a whole" (Ex. 1401, Col. 6:6-10) manages the different camera operation modes, including preventing operations inappropriate for the current mode (such as SET WINDOW outside of scan mode). (Ex. 1401, Fig. 31 and Cols. 22-23). A POSITA would therefore have understood that Yamamoto's SCC 20 controls data transfer, at least

to the extent that it initiates the external hard disk mode, and prevents other circuits from operating in different modes while the external computer is requesting access to the hard disk via the camera's interface circuit 65.

5.   In its Response, Patent Owner asserts that "Yamamoto's system control circuit 20 is a limited device…" Response, p. 23. Yamamoto describes his still video camera as one "in which a system control circuit 20 including a ***microcomputer or micro-processor*** is mounted to control the still video camera as a whole." (Emphasis added) (Ex. 1401, Col. 6:7-10). Nowhere in his patent has Yamamoto placed any limitations on his "system control circuit 20 including a microcomputer or micro-processor," nor has he described it or characterized it as a "limited device."   The SCC, as Yamamoto has explicitly stated, includes a microcomputer or microprocessor. (See also Ex. 1403, Reynolds Decl., ¶ 46)

6.   At the priority dates of the Tasler patents '144 and '746 a POSITA would have known and understood that a broad set of microcomputers and microprocessors was available to system designers. These microcomputers and microprocessors ranged in computation power and application up to and including being the central computing components in desktop computers. A POSITA would have known and understood that even less powerful microcomputers and microprocessors (and micro-controllers, e.g. the widely used members of the low power Intel 8051 family), would have been fully capable of performing

computations that included many of the functions described for Yamamoto's camera. For example, these less powerful, often low power, processors would have been fully capable of performing the relatively simple task of emulating a SCSI device that was actually implemented using a non-SCSI device, for example an IDE hard drive or a non-SCSI optical drive. (*See also* Ex. 1403, Reynolds Decl., ¶ 74).

7.   SCSI emulation is not a demanding operation. A POSITA would have known that a processor performing emulation of a SCSI device would need to be able to receive SCSI commands (and accompanying parameters) and to perform a simple mapping to an equivalent command for the device implementing the emulated SCSI device. A POSITA would have known that many low power processors available at the priority date of the Tasler patents could have performed this command processing, and therefore controlled data transfer to an external computer, even if the data transferred from the hard disk to the external computer did not pass back through the SCC. Because SCC 20 is a microprocessor and it lies on the path between I/F circuit 65 and R/D control circuit 66, a POSITA would have understood Yamamoto disclosed a reasonable implementation in which the processor-based system control circuit 20 performed SCSI emulation as described here when implementing Yamamoto's camera.

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