PRELIMINARY

AMD

Am79C971

PCnet™-*FAST*
Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus

DISTINCTIVE CHARACTERISTICS

- **Single-chip Fast Ethernet controller for the Peripheral Component Interconnect (PCI) local bus**
  - — 32-bit glueless PCI host interface
  - — Supports PCI clock frequency from DC to 33 MHz independent of network clock
  - — Supports network operation with PCI clock from 15 MHz to 33 MHz
  - — High performance bus mastering architecture with integrated Direct Memory Access (DMA) Buffer Management Unit for low CPU and bus utilization
  - — PCI specification revision 2.1 compliant
  - — Supports PCI Subsystem/Subvendor ID/Vendor ID programming through the EEPROM interface
  - — Supports both PCI 5.0-V and 3.3-V signaling environments
  - — Plug and Play compatible
  - — Supports an unlimited PCI burst length
  - — Big endian and little endian byte alignments supported
- **Integrated 10BASE-T and 10BASE-2/5 (AUI) Physical Layer Interface**
  - — Single-chip IEEE/ANSI 802.3, IEC/ISO 8802-3 and Blue Book Ethernet-compliant solution
  - — Automatic Twisted-Pair receive polarity detection and correction
  - — Internal 10BASE-T transceiver with Smart Squelch to Twisted-Pair medium
  - — IEEE 802.3 and N-Way-compliant auto-negotiable 10BASE-T interface
- **Supports General Purpose Serial Interface (GPSI)**
- **Media Independent Interface (MII) for connecting external 10- or 100-Megabit per second (Mbps) transceivers**
  - — IEEE 802.3-compliant MII
  - — Intelligent Auto-Poll™ external PHY status monitor and interrupt
  - — Includes intelligent on-chip Network Port Manager that provides auto-port selection between MII, on-chip 10BASE-T port, and AUI without software support
  - — Supports both auto-negotiable and non auto-negotiable external PHYs
  - — Supports 10BASE-T, 100BASE-TX/FX, 100BASE-T4, 100BASE-T2, and any future IEEE 802.3-compliant MII PHYs at full- or half-duplex
- **Internal/external loopback capabilities on all ports**
- **Supports patented External Address Detection Interface (EADI)**
  - — Receive frame tagging support for internetworking applications
- **Dual-speed CSMA/CD (10 Mbps and 100 Mbps) Media Access Controller (MAC) compliant with IEEE/ANSI 802.3 and Blue Book Ethernet standards**
- **Full-duplex operation supported in AUI, 10BASE-T, MII, and GPSI ports with independent Transmit (TX) and Receive (RX) channels**
- **Flexible buffer architecture**
  - — Large independent internal TX and RX FIFOs
  - — SRAM-based FIFO buffer extension supporting up to 128 kilobytes (Kbytes)
  - — 1/2 Gigabit per second (Gbps) internal data bandwidth
  - — Programmable FIFO watermarks for both TX and RX operations
  - — RX frame queuing for high latency PCI bus host operation
  - — Programmable allocation of buffer space between RX and TX queues
- **Extensive LED status support**
- **EEPROM interface supports jumperless design and provides through-chip programming**
  - — Supports full programmability of half-/full-duplex operation for external 100 Mbps PHYs through EEPROM mapping

- **Supports optional Boot PROM and 1 Megabyte (Mbyte) Flash for diskless node application**
- **Look-Ahead Packet Processing (LAPP) data handling technique reduces system overhead by allowing protocol analysis to begin before the end of a receive frame**
- **Includes Programmable Inter Packet Gap (IPG) to address less network aggressive MAC controllers**
- **Offers the Modified Back-Off algorithm to address the *Ethernet Capture Effect***
- **IEEE 1149.1-compliant JTAG Boundary Scan test access port interface and NAND tree test mode for board-level production connectivity test**
- **Implements low-power management for critical battery powered application and green PCs**
  - — Includes two power-saving sleep modes (sleep and snooze)
  - — Integrated Magic Packet™ technology support for remote power of networked PCs
- **Software compatible with AMD PCnet Family and LANCE/C-LANCE register and descriptor architecture**
- **Compatible with the existing PCnet Family driver/diagnostic software**
- **160-pin PQFP package**

GENERAL DESCRIPTION

The Am79C971 controller is a single-chip 32-bit full-duplex, 10/100-Megabit per second (Mbps) highly-integrated Ethernet system solution, designed to address high-performance system application requirements. It is a flexible bus mastering device that can be used in any application, including network-ready PCs and bridge/router designs. The bus master architecture provides high data throughput in the system and low CPU and system bus utilization. The Am79C971 controller is fabricated with AMD's advanced low-power Complementary Metal Oxide Semiconductor (CMOS) process to provide low operating and standby current for power sensitive applications.

The Am79C971 controller is a complete Ethernet node integrated into a single VLSI device. It contains a bus interface unit, a Direct Memory Access (DMA) Buffer Management Unit, an ISO/IEC 8802-3 (IEEE 802.3)-compliant Media Access Controller (MAC), a large Transmit FIFO and a large Receive FIFO, optional SRAM-based FIFO extension with support for up to 128K bytes of external frame buffering, an IEEE 802.3u-compliant MII, an IEEE 802.3-compliant Twisted-Pair Transceiver Media Attachment Unit (10BASE-T MAU), and an IEEE 802.3-compliant Attachment Unit Interface (AUI). Both proprietary full-duplex and IEEE 802.3 compliant half-duplex operation are supported on the MII, AUI, GPSI, and 10BASE-T MAU interfaces. 10-Mbps operation is supported through the MII, AUI, and 10BASE-T MAU interfaces, and 100 Mbps operation is supported through the MII. The 10BASE-T MAU interface includes an IEEE 802.3-compliant auto-negotiation implementation, which will automatically negotiate between half- and full-duplex with another IEEE 802.3-compliant auto-negotiation 10BASE-T device.

The Am79C971 controller is register compatible with the LANCE (Am7990) Ethernet controller, the C-LANCE (Am79C90) Ethernet controller, and all Ethernet controllers in the PCnet Family (*except* ILACC (Am79C900)), including the PCnet-ISA controller (Am79C960), PCnet-ISA+ controller (Am79C961), PCnet-ISA II controller (Am79C961A), PCnet-32 controller (Am79C965), PCnet-PCI controller (Am79C970), and PCnet-PCI II controller (Am79C970A). The Buffer Management Unit supports the LANCE and PCnet descriptor software models.

The 32-bit multiplexed bus interface unit provides a direct interface to the PCI local bus, simplifying the design of an Ethernet node in a PC system. The Am79C971 controller provides the complete interface to an Expansion ROM or Flash device allowing add-on card designs with only a single load per PCI bus interface pin. With its built-in support for both little and big endian byte alignment, this controller also addresses non-PC applications. The Am79C971 controller's advanced CMOS design allows the bus interface to be connected to either a +5-V or a +3.3-V signaling environment. A compliant IEEE 1149.1 JTAG test interface for board-level testing is also provided, as well as a NAND tree test structure for those systems that cannot support the JTAG interface.

The Am79C971 controller supports auto-configuration in the PCI configuration space. Additional Am79C971 controller configuration parameters, including the unique IEEE physical address, can be read from an external nonvolatile memory (EEPROM) immediately following system reset.

The integrated Manchester encoder/decoder (MENDEC) eliminates the need for an external Serial Interface Adapter (SIA) in the system. The built-in GPSI allows the MENDEC to be bypassed.

In addition, the device provides programmable on-chip LED drivers for transmit, receive, collision, receive polarity, link integrity, activity, link active, or jabber status. The Am79C971 controller also provides an EADI to allow external hardware address filtering in

internetworking applications and a receive frame tagging feature.

For power sensitive applications where low standby current is desired, the device incorporates two sleep functions to reduce overall system power consumption, excellent for notebooks and green PCs. In conjunction with these low power modes, the PCnet-*FAST* controller also has integrated functions to support Magic Packet technology, an inexpensive technology that allows remote wake up of green PCs.

The controller has the capability to automatically select either the MII, AUI, or Twisted-Pair transceiver. Only one interface is active at any one time. Any of the network interfaces can be programmed to operate in either half-duplex or full-duplex mode (AUI full-duplex only supports the 10BASE-F standard).

The dual Transmit and Receive FIFOs optimize system overhead, providing sufficient latency tolerance at 10 Mbps and for 100-Mbps systems where low latencies can be guaranteed during frame transmission and reception.

In highly loaded 10-Mbps systems, such as servers or when using the controller in a 100-Mbps environment, the additional frame buffering capability provided by a 16-bit wide SRAM interface provides high performance and high latency tolerance on the system bus and network.

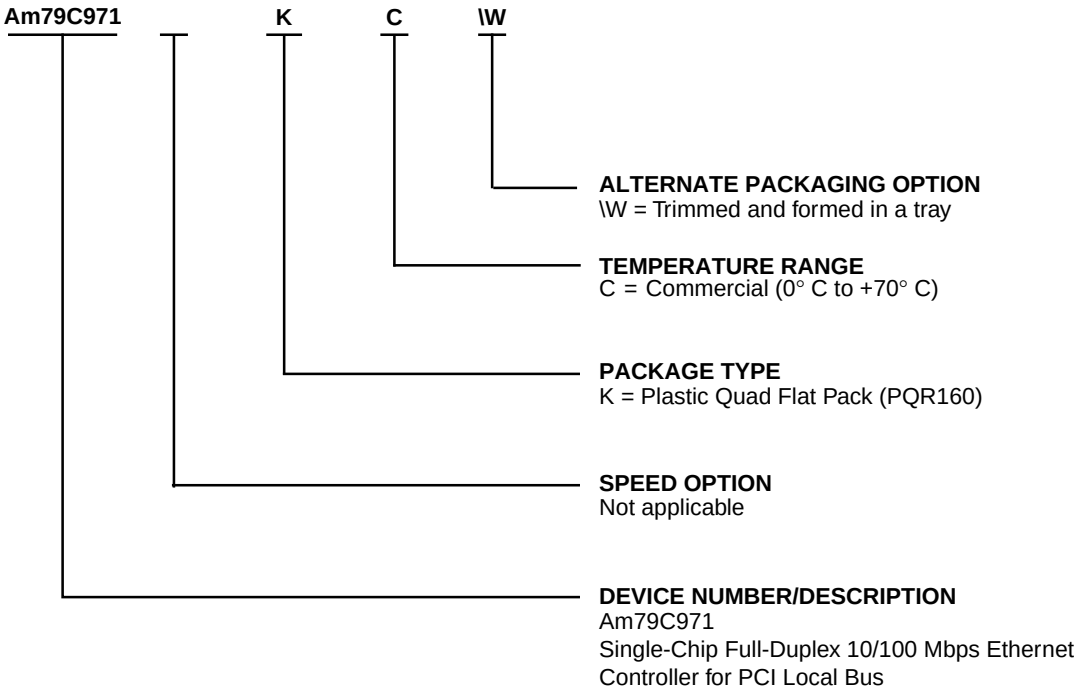
The Am79C971 controller can use up to 128 Kbytes of SRAM as an extension of its dual Transmit and Receive FIFOs. When no SRAM is used, the Am79C971 controller's FIFOs are programmed to bypass the SRAM interface.

ISO/IEC 8802-3 and IEEE 802.3 will be used interchangeably when referring to half-duplex 10 Mbps networks. IEEE 802.3 or IEEE 802.3u will be used interchangeably only when referring to half-duplex 100-Mbps Ethernet networks, since the IEEE standard is not ISO approved yet. Full-duplex is a proprietary standard and is not approved by IEEE or ISO.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

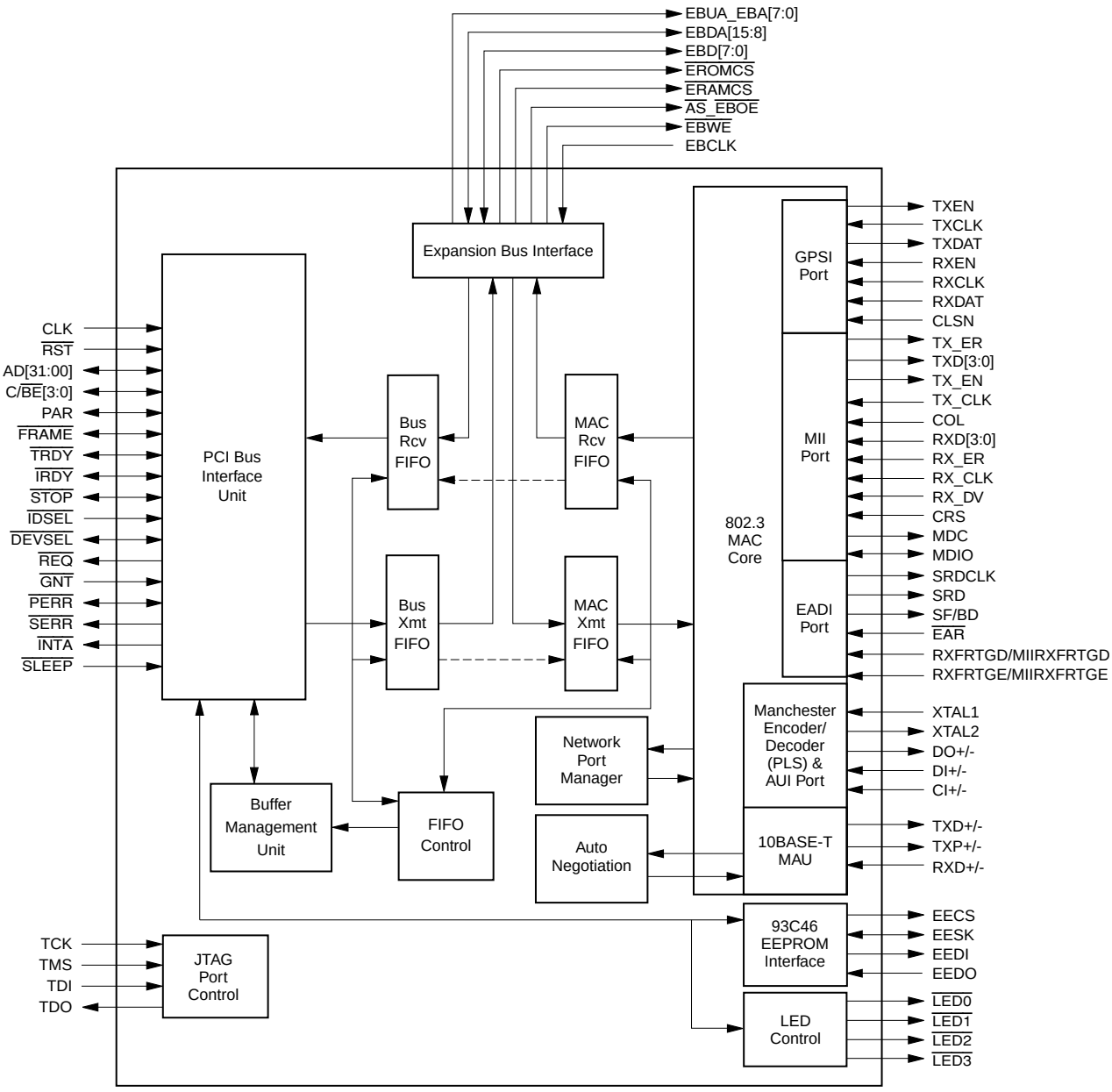


Valid Combinations	
Am79C971	KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

BLOCK DIAGRAM



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