

**11.3.4.5 Coaxial Cable to AUI Delay Characteristics.** The MAU receiver timing and delays described below shall not be exceeded or traded off against any other delays in the system.

**11.3.4.5.1 Received RF to Circuit DI Delay.** When there is no collision in progress, the delay from the end of the SFD in the received RF data signal at the coaxial cable interface to the end of the SFD on Circuit DI, shall be a maximum of 75 bit times (see Fig 11-13). The minimum is not specified, nor is the delay specified at other locations in the packet. The end of the SFD in the received RF data signal (at the coaxial cable interface) is defined as the time at which the envelope of the carrier would pass through the midpoint if the first bit following the SFD was a zero and the scrambler disabled.

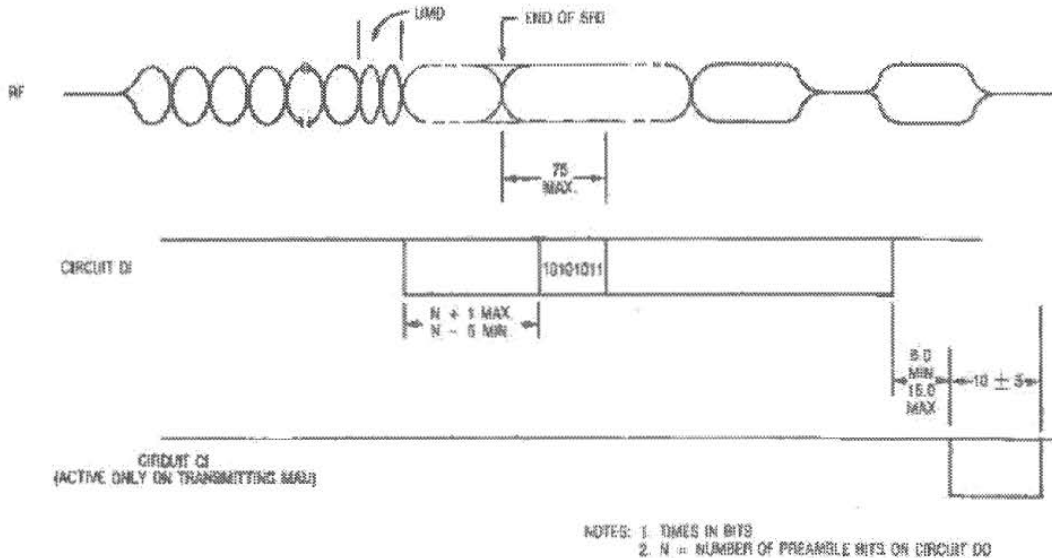


Fig 11-13  
No Collision Timing Diagram (Coax to AUI)

**11.3.4.5.2 Received RF to CE RF Output and Circuit CI Delay.** In the event that a collision is detected via the bit-by-bit comparison, the delay from the end of the bit in which the collision was detected, as represented by the RF signal, to the 50% point on the rising edge of the collision enforcement signal shall not exceed 34 bit times. The delay from the same point to the first transition of Circuit CI shall not exceed 27 bit times. Circuit CI shall cease activity no more than 31 bit times after activity on the RF interface (in both data channel and collision enforcement channel) ceases. See Fig 11-14 and Fig 11-15.

**11.3.4.5.3 Collision Enforcement to Circuit CI Delay.** In the event of a collision enforcement by another MAU, the delay from the 50% point on the rising edge of the RF collision enforcement signal to the first transition of Circuit CI shall be no more than 31 bit times. Circuit CI shall be active for a minimum of 5 bit times and shall become inactive within 31 bit times of the cessation of activity on the RF coaxial cable interface, as shown in Fig 11-15.

**11.3.4.5.4 Receive Data to SQE Test Delay.** If a collision enforcement signal is received after the ced\_window signal becomes inactive (see (9) in 11.2.3.2), or if the MAU has transmitted an SQE Test sequence, the MAU is to interpret the collision enforcement signal as an SQE Test signal. If the SQE Test sequence is correctly detected (that is, the test passes), then the delay from the last transition of Circuit DI to the first transition of Circuit CI shall be at least 6 but not more than 16 bit times. Circuit CI shall remain active for  $10 \pm 5$  bit times. Only the transmitting MAU shall assert its Circuit CI as a result of successful completion of the SQE Test sequence.

If a collision enforcement signal is received before the ced\_window signal becomes inactive, the MAU shall interpret it as a collision enforcement and the timing of 11.3.4.5.3 shall apply.

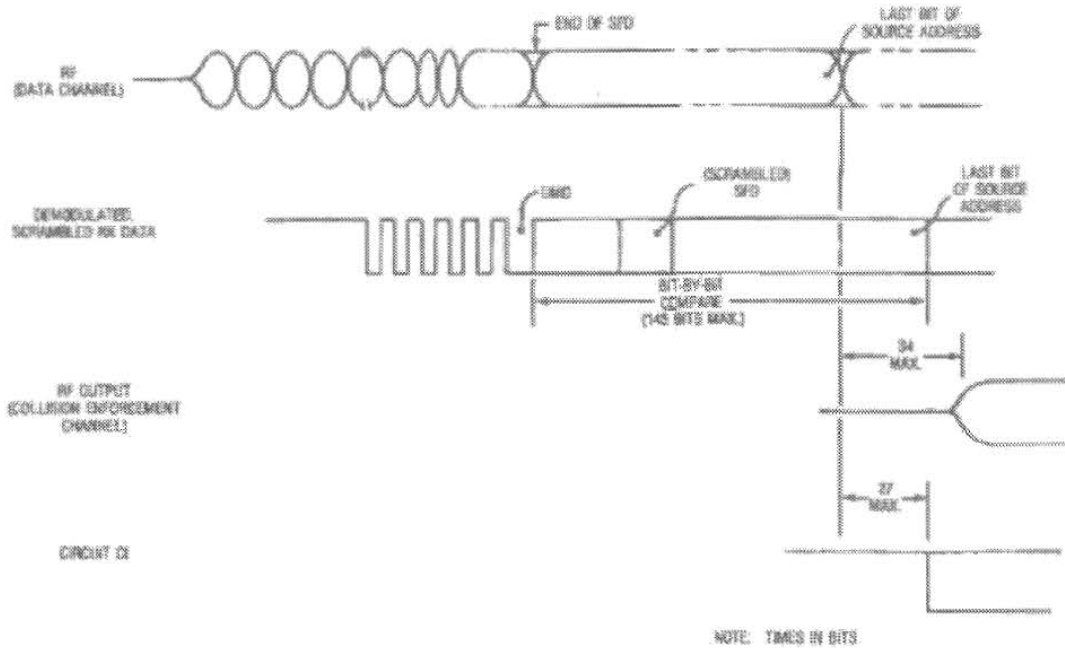


Fig 11-14  
Collision Timing Diagram (RF Data to RF Collision Enforcement)

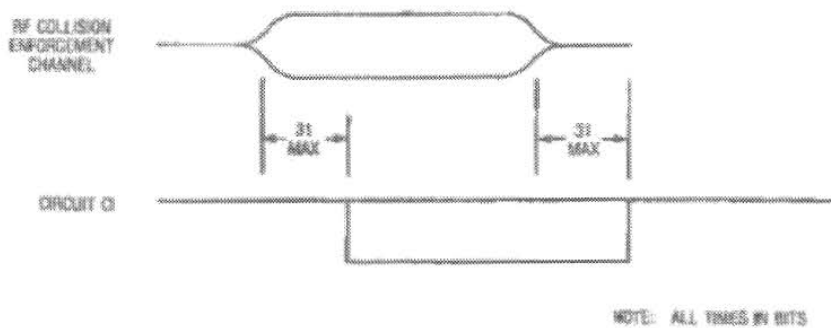


Fig 11-15  
Collision Timing Diagram (Coaxial Cable Interface to AUI Circuit CI)

**11.3.4.6 Delay from Circuit DO to Circuit DI.** The time delay from a bit on Circuit DO at the AU Interface to the corresponding bit on Circuit DI at the AU Interface is equal to the round trip delay of the MAU connected back-to-back with itself (that is, in RF loopback) plus the round trip delay through the cable system at the location of the MAU. Therefore, the delay is a function of the location of the MAU on the cable system. It is never less than the transmitter delay plus the postamble length plus the time to detect loss of carrier or presence of the SQE Test signal. See Fig 11-16 for the timing relationship when the cable has zero length.

When the MAU is transmitting a short packet (less than 576 bits), the timing for Circuit CI during the SQE Test sequence shall be the same as it is for normal length packets. If the MAU transmits a short packet (less than 576 bits) that encounters a collision and if the SQE Test sequence has not been

transmitted when the collision is detected by the MAU, then the timing for Circuit CI shall be the same as it is for any normal collision.

**11.3.4.7 Interpacket Gap Requirement.** The MAU shall be able and ready to transmit data presented to it by the DTE no later than 90 bit times after the last bit of a received packet was presented by the MAU at its AUI.

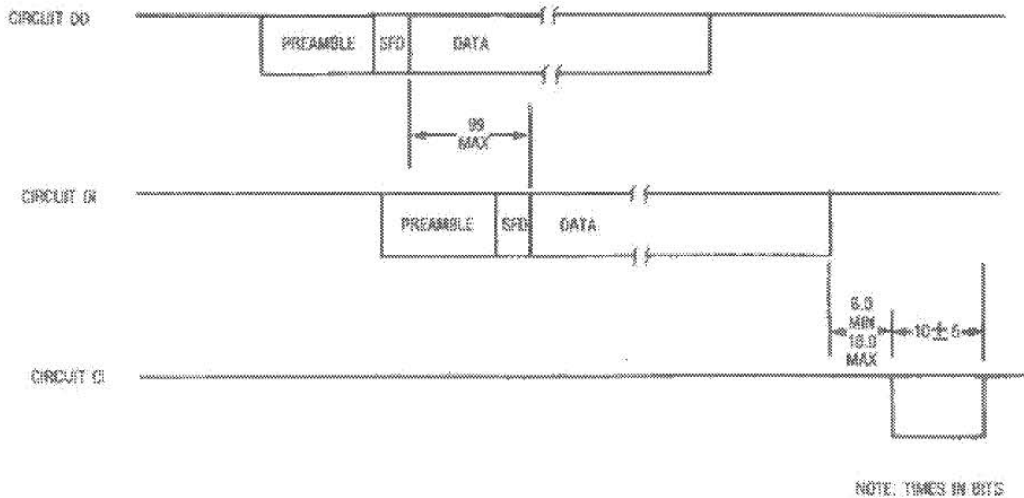


Fig 11-16  
Timing at AUI for Zero-Length Coax

**11.3.4.8 Bit Error Rate.** The MAU shall have a Bit Error Rate (BER) as measured at the AUI lower than one error in  $10^8$  in a "zero-length coax" test environment (that is, a coaxial cable connection sufficiently short to have negligible delay and transmission impairments). It shall have this BER for receive signal levels in the range specified in 11.3.1.1.3 and in the presence of  $-28.3$  dBmV rms/14 MHz white Gaussian noise. This represents a 24.3 dB signal-to-noise ratio for the specified minimum signal level,  $-4$  dBmV rms. For the same BER in a "system" environment (as opposed to zero-length coax), a 26 dB signal-to-noise ratio is required.

The MAU shall meet the BER requirements specified above when receiving strings of up to 33 consecutive identical bits.

**11.3.5 Reliability.** Component failures within the MAU electronics should not impede communication among other MAUs on the broadband coaxial cable. Connectors and other passive components comprising the means of connecting the MAU to the coaxial cable shall be designed to minimize the probability of total network failure. The MAU shall be designed to provide an MTBF of at least 1 000 000 hours without causing communication failure among other stations attached to the broadband local network medium.

## 11.4 System Considerations

**11.4.1 Delay Budget and Network Diameter.** The delay budget for the broadband MAU and rest of the Physical Layer is tabulated in Table 11.4-1. This table includes allocations for trunk cables (the backbone cables in the system), drop cables (a length of 25 m is assumed), etc. The velocities of propagation assumed are included in the table; use of other types of cables will alter the system diameter accordingly. The types of cables, including the mix of drop and trunk cable lengths, can be altered as long as the total

propagation delay from the most distant MAU to the headend does not exceed 70 bit times. The total delay budget of 576 bit times includes allowance for the preamble and SFD (64 bits).

Table 11.4-1 tabulates delay allocations for a dual-cable system with no headend delay. In translated single-cable systems, the headend translator delay reduces the maximum trunk cable distance by  $[D/(3 \times CV)]$ , where  $D$  is the delay in nanoseconds, and  $CV$  is the cable velocity in nanoseconds per meter. For 3.83 ns/m velocity trunk cable, this reduction is  $[\text{Delay (ns)} / 7.66]$  m.

**Table 11.4-1**  
**Broadband Dual-Cable Systems—Physical Layer Delay Budget**

Delay Element	Maximum Allowed Value (Bits)
DTE1 starts to put out first bit	0.00
First bit from DTE1 at AUI	3.00
AUI Cable (50 m at 5.13 ns/m)	2.57
Circuit DO to Tx RF Out	24.00
Tx Drop Cable (25 m at 4.27 ns/m)	1.05
Tx Trunk Cable (1800 m at 3.83 ns/m)	68.95
Rx Trunk Cable (25 m at 4.27 ns/m)	68.95
Rx Drop Cable (25 m at 4.27 ns/m)	1.05
End of Bit Comparison (last bit of source address)	100.00
Rx RF to Collision Enforcement RF Out (from RX bit that is found to be in error to collision enforcement out)	34.00
Tx Drop Cable (25 m at 4.27 ns/m)	1.05
Tx Trunk Cable (1800 m at 3.83 ns/m)	68.95
Rx Trunk Cable (1800 m at 3.83 ns/m)	68.95
Rx Drop Cable (25 m at 4.27 ns/m)	1.05
Rx Collision Enforcement to Circuit CI	31.00
AUI Cable (50 m at 5.13 ns/m)	2.57
DTE1 Detects Collision Presence	3.00
DTE1 Jams Channel	32.00
Allowance for Traps, Splitters, Amplifiers, and Margin	3.96
<b>Total</b>	<b>576.00</b>

**11.4.2 MAU Operation with Packets Shorter than 512 Bits.** The MAU transmits an SQE Test sequence onto the RF medium after every transmitted packet. If the frame plus preamble and SFD is less than the `cod_window` in length, a receiving MAU cannot distinguish the SQE Test signal from a collision enforcement signal due to a collision. Therefore, operation of the MAU with data frames shorter than 512 bits may cause all other receiving MAUs to see a collision. The transmitting MAU, however, recognizes the SQE Test because that MAU was the one that transmitted the test. An MAU transmitting a short packet that encounters a collision can distinguish the resulting collision enforcement from an SQE Test signal by the fact that the transmitting MAU will not have transmitted the SQE Test sequence unless the packet is shorter than the round trip delay on the cable plant. In the latter instance, the transmitting MAU may not detect a collision enforcement.

**11.5 Characteristics of the Coaxial Cable System.** The cable system upon which the broadband MAU operates shall meet the following electrical and mechanical requirements.

**11.5.1 Electrical Requirements.** The electrical requirements of the cable system are listed in Table 11.5-1. Each parameter is applicable over the frequency range to be used by the broadband MAU.

Adjacent channel signal levels shall be consistent with the requirements of 11.3.1.1.4.

**Table 11.5-1**  
**Cable System Electrical Requirements**

Impedance	75 $\Omega$
Return Loss	14 dB min
Transmit Level	+30 dBmV $\pm$ 2 dB
Receive Level	+6 dBmV $\pm$ 10 dB
Maximum Receive Noise Level	-30 dBmV/14 MHz
Loss Variation* (per 18 MHz band)	2 dB min, 52 dB max
Path Loss (between any transmit port and receive port, including loss variation)	36 dB min, 59 dB max
Group Delay Variation	
—around data carrier	20 ns/10 MHz max
—over 18 MHz band	34 ns max

\* Not including headend.

**11.5.2 Mechanical Requirements.** The connection of the cable system to the broadband MAU is via a standard F-series screw-on male connector. For the dual-cable case, two such connectors are required: one for transmit and the other for receive.

**11.5.3 Delay Requirements.** The maximum length of the cable system is constrained by the allowable round trip delay from the farthest transmitting MAU to the farthest receiving MAU. Table 11.4-1 allows 140 bit times round trip delay in the cable system. For trunk cable propagation velocity of 3.83 ns/m, this allows 3600 m of trunk cable (round trip; 1800 m from the farthest point to the headend), and 25 m of 4.27 ns/m velocity drop cable at each MAU. In addition, 50 m of AUI cable is allowed on each MAU, therefore allowing, in this case, a maximum of 3750 m DTE to DTE separation. These lengths will be different if cables of different propagation velocity are used. This is acceptable so long as the maximum delay is not exceeded.

For single-cable systems, the maximum delay of 140 bit times includes the delay through the headend. The maximum cable system length must be reduced appropriately, as described in 11.4.1.

## 11.6 Frequency Translator Requirements for the Single-Cable Version

**11.6.1 Electrical Requirements.** The headend frequency translator performance is included in the cable system characteristics specified in 11.5, except as defined in Table 11.6-1.

**Table 11.6-1**  
**Frequency Translator Requirements**

Group Delay Variation	
—around data carrier frequency	20 ns/10 MHz max
—between data carrier and CE center frequency	50 ns max
Amplitude Variation (from 8 MHz below the input data carrier frequency to 1 MHz above the CE center frequency)	2 dB max
Translation Frequency	per Table 11.3-1

The frequency translator contributes to total cable system delay and shall be labeled by the vendor with the input-to-output delay in the band of operation. The effect on network length can then be computed per 11.4.1.

**11.6.2 Mechanical Requirements.** The input and output mechanical interface shall be 75  $\Omega$  female F-series coaxial connectors. The connection to the broadband medium shall be through a coaxial cable with a mating male F-series connector.

## 11.7 Environmental Specifications

**11.7.1 Safety Requirements.** This subsection sets forth a number of recommendations and guidelines related to safety concerns. This list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to assure compliance with the appropriate standards.

Local area network cable systems, as described in this section, are subject to at least four direct electrical safety hazards during their use, and designers of connecting equipment should be aware of these hazards. The hazards are as follows:

- (1) Direct contact between local network components and power or lighting circuits
- (2) Static charge buildup on local network cables and components
- (3) High-energy transients coupled onto the local network cabling system
- (4) Potential differences between safety grounds to which various network components are connected

These electrical safety hazards, to which all similar cabling systems are subject, should be alleviated for a local network to perform properly. In addition to provisions for properly handling these faults in an operational system, special measures shall be taken to ensure that the intended safety features are not negated when attaching or detaching equipment from the local area network medium of an existing network.

Sound installation practice, as defined in applicable national and local codes and regulations, shall be followed in every instance in which such practice is applicable.

### 11.7.2 Electromagnetic Environment

**11.7.2.1 Susceptibility Levels.** Sources of interference from the environment include electromagnetic fields, electrostatic discharges, transient voltages between earth connections, etc.

The physical MAU hardware shall meet its specifications when operating in an ambient plane wave field of:

- (1) 2 V/m from 10 kHz through 30 MHz
- (2) 5 V/m from 30 MHz through 1 GHz

MAUs meeting this section should provide adequate RF ground return to satisfy the EMC specification.

**11.7.2.2 Emission Levels.** The physical MAU hardware shall comply with the applicable national and local regulations for emission levels.

**11.7.3 Temperature and Humidity.** The MAU and associated cable system are expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling such as shock and vibration. Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

## 12. Physical Signaling, Medium Attachment, and Baseband Medium Specifications, Type 1BASE5

### 12.1 Introduction

**12.1.1 Overview.** 1BASE5 is a 1 Mb/s CSMA/CD network based on twisted pair wiring. Each DTE (Data Terminal Equipment) is star-connected to a shared hub through two pairs that function as transmit and receive channels. Hubs can be cascaded, and DTEs can be connected to any hub. Packets transmitted by a DTE are propagated by the hub to a higher-level hub if one exists; otherwise the hub broadcasts the packet back down to all DTEs and lower-level hubs. Packets received by a hub from a higher-level hub are retransmitted to all attached DTEs and lower-level hubs. If two or more DTEs or lower-level hubs transmit concurrently, the hub generates a collision-presence signal that the DTEs detect as a collision. Hubs between a transmitting DTE and the header (highest level) hub propagate data or the collision-presence signal to the header hub; this hub in turn broadcasts the packet or collision signal to all DTEs and lower-level hubs.

**12.1.2 Scope.** The 1BASE5 specification builds upon the first six major sections of this standard; the remaining major sections (other than this one, of course) do not apply to 1BASE5. That is, the Media Access Control (MAC) and Physical Signaling (PLS) Service Specifications are used in common with the other implementations of this standard, but the Physical Medium Attachment (PMA) sublayer, transmission medium, and hub functions for Type 1BASE5 are specified in this section. The relationship of the 1BASE5 specification to the OSI Reference Model and the IEEE 802.3 CSMA/CD LAN Model is shown in Fig 12-1.

#### 12.1.3 Definitions

**bit cell.** The time interval used for the transmission of a single data (CD0 or CD1) or control (CVH or CVL) symbol.

**bit rate (BR).** The rate of data throughput on the medium (in b/s or Hz, whichever is more appropriate to the context). See 12.3.2.4.1.

**bit time (BT).** The duration (of transmission) of one bit symbol (bit cell) (1/BR). See 12.3.2.4.1.

**carrier sense.** In a local area network, an ongoing activity of a data station to detect whether another station is transmitting. Note that the signal provided by the PLS to the PMA sublayer indicates that one or more DTEs are currently transmitting.

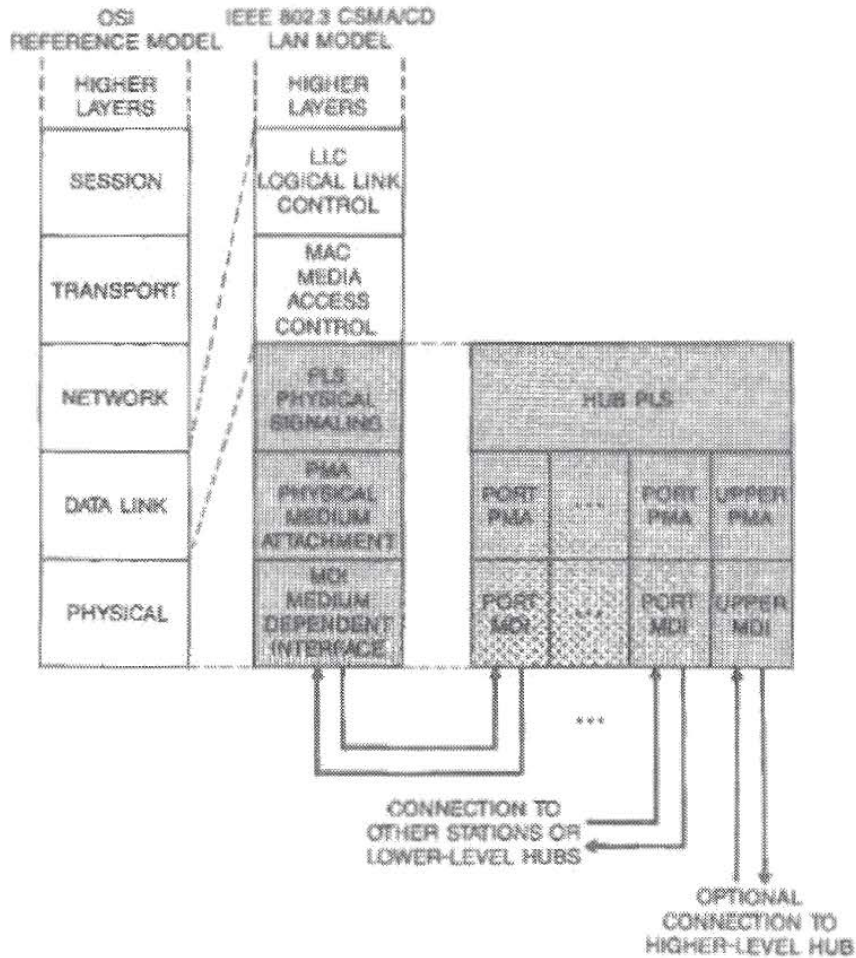
**Clocked Data One (CD1).** A Manchester encoded data "1." A CD1 is encoded as a LO for the first half of the bit cell and a HI for the second half of the bit cell.

**Clocked Data Zero (CD0).** A Manchester encoded data "0." A CD0 is encoded as a HI for the first half of the bit cell and a LO for the second half of the bit cell.

**Clocked Violation HI (CVH).** A symbol that deliberately violates Manchester encoding rules, used as part of the Collision Presence signal. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and a transition from HI to LO at the end of the bit cell.

**Clocked Violation LO (CVL).** A symbol that deliberately violates Manchester encoding rules, used as part of the Collision Presence signal. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and a transition from LO to HI at the end of the bit cell.

**collision.** A condition that results from concurrent transmissions on the physical medium.



**Fig 12-1**  
IBASE5 Relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model

**Collision Presence (CP).** The non-Manchester signal generated by hubs to report collisions and some error conditions. See 12.3.2.4.3 for details.

**header hub (HH).** The highest-level hub in a hierarchy of hubs. The HH broadcasts signals transmitted to it by lower-level hubs or DTEs, such that they can be received by all DTEs that may be connected to it, either directly or through intermediate hubs. See 12.2.1 for details.

**hub.** A device used to provide connectivity between DTEs. Hubs perform the basic functions of restoring signal amplitude and timing, collision detection and notification, and signal broadcast to lower-level hubs and DTEs.

**idle (IDL).** A signal condition where no transition occurs on the transmission line. It is used to define the time between packets. See 12.3.2.4.4 for details.

**intermediate hub (IH).** A hub that occupies any level below the header hub in a hierarchy of hubs. See 12.2.1 for details.



**Jabber Function.** A mechanism for controlling abnormally long transmissions.

**special link (SL).** A transmission system that replaces the normal medium. See 12.8 for details.

**12.1.4 General Characteristics.** Type 1BASE5 has the following general characteristics:

- (1) 1 Mb/s signaling rate, Manchester encoded
- (2) Twisted pair wiring
- (3) Point-to-point interconnection of DTEs to hubs, with one twisted pair serving as the upward link, the other as the downward link
- (4) Data pairs can coexist in the same telephone cable bundles as voice pairs
- (5) When a hub receives signals from a DTE or lower-level hub, it propagates them to a higher-level hub if one exists; otherwise, the hub broadcasts the signals back down to the DTEs and lower-level hubs
- (6) When a hub receives signals concurrently from two or more DTEs or lower-level hubs, it generates a unique collision presence signal, and distributes it as in (5) above
- (7) DTE-to-hub and hub-to-hub interfaces are electrically isolated at both ends
- (8) Up to five hub levels are allowed
- (9) Hubs serve as repeaters
- (10) Maximum DTE-to-hub and hub-to-hub distance is approximately 250 m for telephone wiring (cable-type dependent; see 12.7)
- (11) Special links may be used to extend some DTE-to-hub or hub-to-hub distances to 4 km

**12.1.5 Compatibility.** This specification calls out one principal compatibility interface, namely PMA-to-Medium. It is intended that different implementations of DTEs and hubs be able to interoperate in 1BASE5 networks.

**12.1.6 Objectives of Type 1BASE5 Specification**

- (1) Provide for low-cost networks, as related to both equipment and cabling
- (2) Make it possible to use telephone-type building wiring, and in particular spare wiring when available
- (3) Provide for easy installability, reconfigurability, and service
- (4) Ensure interconnectability of independently developed DTEs and hubs
- (5) Ensure fairness of DTE access
- (6) Provide a communication channel with a resultant mean bit error rate, at the physical layer service interface, of less than one part in  $10^8$  (on the order of one part in  $10^9$  at the link level)

## 12.2 Architecture

**12.2.1 Major Concepts.** Type 1BASE5 is a 1 Mb/s CSMA/CD network. DTEs are connected to hubs (and hubs to other hubs) by point-to-point wiring, resulting in a star topology network. Data transmissions are Manchester encoded.

An elementary configuration is illustrated in Fig 12-2. In this instance, each DTE is connected to the hub via separate transmit and receive channels (normally two twisted pairs). The hub serves as the point of concentration and performs two major functions: signal regeneration/retiming (repeating) and collision detection. When only one DTE transmits, the hub repeats the signals, compensating for amplitude and phase distortion, and broadcasts to all DTEs. When a hub detects two or more DTEs transmitting concurrently, the hub generates a unique Collision Presence (CP) signal, which it broadcasts instead of the originally transmitted signals. The hub continues to send CP until it receives IDI from all lower-level DTEs. CP has the property that it can be detected by DTEs as a Manchester code violation.

The interconnection architecture does not imply any minimum, typical, or maximum number of DTEs to be connected to a given hub; this is an implementation or installation detail.

Up to five levels of hubs may be cascaded. A two-level configuration is illustrated in Fig 12-3, with a head-of-hub (HH) and intermediate hubs (IH). There can be a number of IHs; there must be one and only one HH. Each DTE or IH is connected to a hub via separate transmit and receive channels (normally two twisted pairs). An IH propagates signals from its DTEs toward the HH; it sends CP toward the HH in the event of

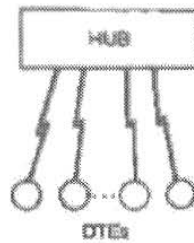


Fig 12-2  
Single Hub Network

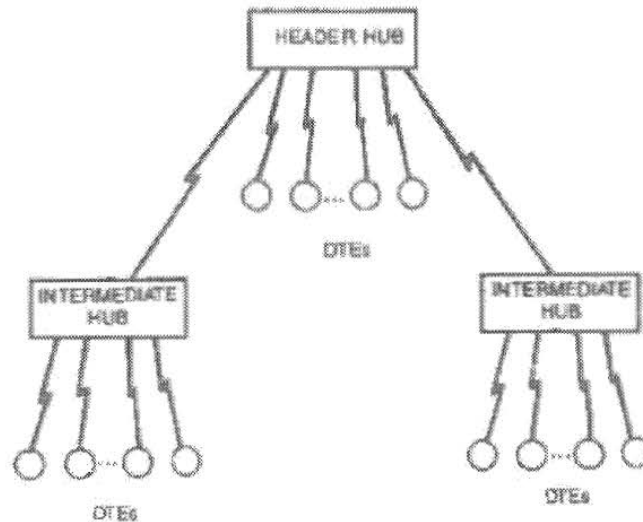


Fig 12-3  
Network with Two Levels of Hubs

a collision. The HH repeats the signals it receives from DTEs or IHs back down to all DTEs and IHs. The HH generates CP if more than one of its inputs becomes active. The IHs repeat the signals received from the HH, and broadcast to all the connected DTEs' receivers. Hubs do not distinguish whether input signals along the upward path emanate from DTEs or lower-level IHs. If a single input is active, the hub repeats the signal regardless of its source; if more than one is active, it generates CP.

A configuration involving four hub levels and a special link is illustrated in Fig 12-4. In this example, one IH is used for simple repeating (one connection upward and one connection downward). Other than having one link in and one link out, repeaters are identical to other hubs. Special links are connections, possibly containing active devices, that are used for situations requiring extra propagation delay or special transmission media.

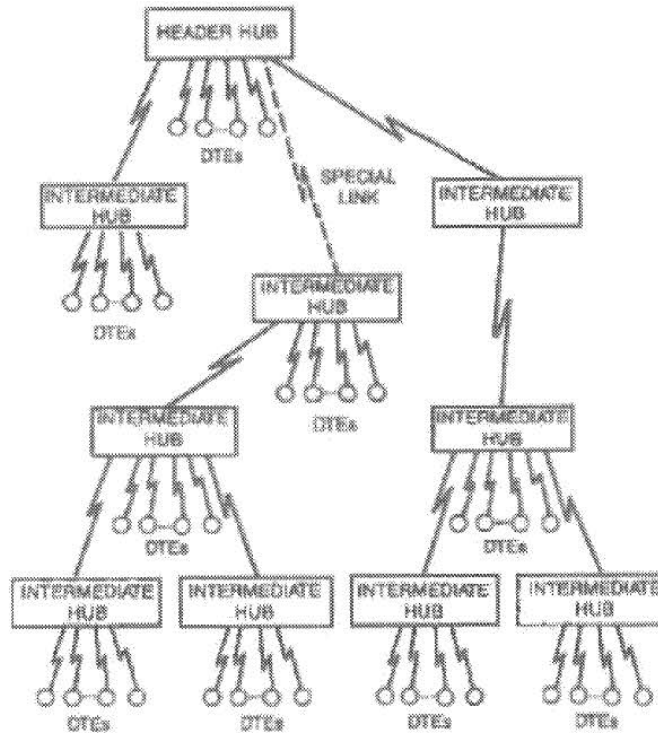


Fig 12-4  
Network with Four Levels of Hubs

**12.2.2 Application Perspective.** The primary application area for type 1BASE5 is expected to be in office environments for networking DTEs such as personal computers or other workstations. In many cases, spare wiring contained in existing telephone wire bundles will be used.

**12.2.3 Packet Structure.** Packets are transmitted from the PLS to the PMA as follows:

<silence> <preamble> <afd> <data> <etd> <silence>

The packet elements shall have the following characteristics:

Element	Characteristics
<silence>	No transitions
<preamble>	Alternating CD1 and CD0 for 256 bit times (ending in CD0)
<afd>	CD1 CD0 CD1 CD0 CD1 CD0 CD1 CD1
<data>	8 × N instances of CD0 or CD1
<etd>	First part of IDL

**12.2.3.1 Silence.** The <silence> delimiter provides an observation window for an unspecified period of time during which no transitions occur. The minimum duration of <etd> followed by <silence> is the interFrameGap defined in 4.4.2.2.

**12.2.3.2 Preamble.** The <preamble> delimiter begins a packet transmission and provides a signal for receiver synchronization. The signal shall be an alternating pattern of CD1 and CD0. This pattern shall be transmitted by the DTE for a minimum of 56 bit times at the beginning of each packet. The last bit of the preamble (that is, the final bit of preamble before the start-of-frame delimiter) shall be a CD0.

The DTE is required to supply at least 56 bits of preamble in order to satisfy system requirements. System components consume preamble bits in order to perform their functions. The number of preamble bits sourced ensures an adequate number of bits are provided to each system component to correctly implement its function.

**12.2.3.3 Start-of-Frame Delimiter.** The <afd> indicates the start of a frame, and follows the preamble.

**12.2.3.4 Data.** The <data> in a transmission shall be in multiples of eight (8) encoded data bits (CD0s and CD1s).

**12.2.3.5 End-of-Transmission Delimiter.** The <etd> indicates the end of a transmission and serves to turn off the transmitter. The signal shall be the first part of an IDL.

### 12.3 DTE Physical Signaling (PLS) Specification

**12.3.1 Overview.** This section defines logical characteristics of the DTE PLS sublayer for IBASE5. The relationship of this specification to the entire standard is shown in Fig 12-5. The sublayer and its relationship to the MAC and PMA sublayers are described in an abstract way and do not imply any particular implementation.

#### 12.3.1.1 Summary of Major Concepts

- (1) There are two channels between the PLS and PMA sublayers. Output data are passed through the output channel and input data and control (CP) are passed through the input channel.
- (2) Each direction of data transfer through the PLS operates independently and simultaneously (that is, the PLS is full duplex).

**12.3.1.2 Application Perspective.** The DTE PLS sublayer performs the following functions:

- (1) Encodes OUTPUT\_UNITS from the MAC sublayer into a Manchester encoded waveform that it sends to the PMA sublayer output circuit
- (2) Decodes a Manchester encoded waveform from the PMA sublayer input circuit into INPUT\_UNITS, CARRIER\_STATUS, and SIGNAL\_STATUS

**12.3.2 Functional Specification.** This section provides a detailed model for the DTE PLS sublayer.

Many of the terms used in this section are specific to the interface between this sublayer and the MAC sublayer. These terms are defined in the service specification for the PLS sublayer (see 6.3).

**12.3.2.1 PLS-PMA Interface.** The PLS and PMA communicate by means of the following messages:

Message	Meaning	Source
<i>output</i>	Output information	PLS
<i>output_idle</i>	No data to be output	PLS
<i>input</i>	Input information	PMA
<i>input_idle</i>	No input information	PMA

**12.3.2.1.1 *output* Message.** The PLS sublayer sends an *output* message to the PMA sublayer when the PLS sublayer receives an OUTPUT\_UNIT from the MAC sublayer.

The physical realization of the *output* message is a CD0 or a CD1 sent by the PLS to the PMA. The PLS sends a CD0 if the OUTPUT\_UNIT is a ZERO or a CD1 if the OUTPUT\_UNIT is a ONE. This message is time-coded. That is, once this message has been sent, the function is not completed until one bit time later.

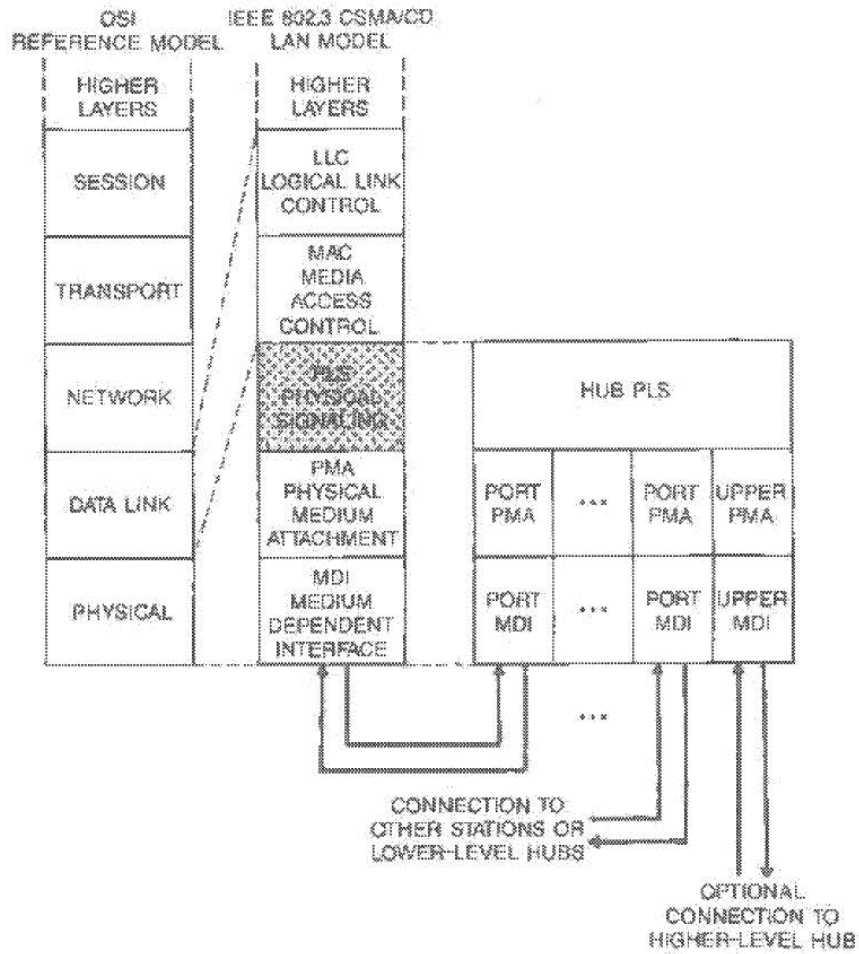


Fig 18-5  
Station Physical Signaling, Relationship to the ISO OSI Reference Model  
and the IEEE 802.3 CSMA/CD LAN Model

The *output* message cannot be sent again until the bit cell being sent as a result of sending the previous *output* message is complete.

**12.3.2.1.2 output\_idle Message.** The PLS sublayer sends an *output\_idle* message to the PMA sublayer at all times when the MAC sublayer is not in the process of transferring output data across the MAC to PLS interface. The *output\_idle* message is no longer sent (and the first OUTPUT\_UNIT is sent using the *output* message) when the first OUTPUT\_UNIT of a packet is received from the MAC sublayer. The *output\_idle* message is again sent to the PMA when DATA\_COMPLETE is received from the MAC sublayer.

The physical realization of the *output\_idle* message is IDL sent by the PLS to the PMA.

**12.3.2.1.3 input Message.** The PMA sublayer sends an *input* message to the PLS sublayer when the PMA has received a bit from the medium and is prepared to transfer this bit to the PLS.

The physical realization of the *input* message consists of data units, CD0, CD1, CVL, or CVH, derived from the incoming data stream. If ambiguity exists due to excessive noise or jitter, the PMA may send an arbitrary combination of these.

**12.3.2.1.4 *input\_idle* Message.** The PMA sublayer sends an *input\_idle* message to the PLS sublayer when the PMA sublayer does not have data to send to the PLS sublayer. This condition exists when carrier is lost or IDL is received.

**12.3.2.2 PLS-MAC Interface.** The PLS and MAC communicate by means of the following messages:

Message	Meaning	Source
OUTPUT_UNIT	Data sent to the PMA	MAC
OUTPUT_STATUS	Response to OUTPUT_UNIT	PLS
INPUT_UNIT	Data received from the PMA	PLS
CARRIER_STATUS	Indication of input activity	PLS
SIGNAL_STATUS	Indication of error/no error condition	PLS

**12.3.2.2.1 OUTPUT\_UNIT.** The MAC sublayer sends the PLS sublayer an OUTPUT\_UNIT every time the MAC sublayer has a bit to send. Once the MAC sublayer has sent an OUTPUT\_UNIT to the PLS sublayer, it may not send another OUTPUT\_UNIT until it has received an OUTPUT\_STATUS message from the PLS sublayer. The OUTPUT\_UNIT is a ONE if the MAC sublayer wants the PLS sublayer to send a CD1 to the PMA sublayer, a ZERO if a CD0 is desired, or a DATA\_COMPLETE if an IDL is desired.

**12.3.2.2.2 OUTPUT\_STATUS.** The PLS sublayer sends the MAC sublayer an OUTPUT\_STATUS in response to every OUTPUT\_UNIT received by the PLS sublayer. OUTPUT\_STATUS sent is an OUTPUT\_NEXT when the PLS sublayer is ready to accept the next OUTPUT\_UNIT from the MAC sublayer. (The purpose of OUTPUT\_STATUS is to synchronize the MAC sublayer data output with the data rate of the physical medium.)

**12.3.2.2.3 INPUT\_UNIT.** The PLS sublayer sends the MAC sublayer an INPUT\_UNIT every time the PLS receives an *input* message from the PMA sublayer. The INPUT\_UNIT is a ONE if the PLS sublayer receives a CD1 from the PMA sublayer or a ZERO if the PLS sublayer receives a CD0 from the PMA sublayer. The INPUT\_UNIT may be either ZERO or ONE if the PLS sublayer receives a CVL or CVH from the PMA sublayer.

**12.3.2.2.4 CARRIER\_STATUS.** The PLS sublayer sends the MAC sublayer CARRIER\_STATUS whenever there is a change in carrier status, as detected by the PMA. The PLS sublayer sends CARRIER\_ON when it receives an *input* message from the PMA and the previous CARRIER\_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER\_OFF. The PLS sublayer sends CARRIER\_OFF when it receives an *input\_idle* message from the PMA sublayer, and the previous CARRIER\_STATUS that the PLS sublayer sent to the MAC sublayer was CARRIER\_ON.

**12.3.2.2.5 SIGNAL\_STATUS.** The PLS sublayer sends the MAC sublayer SIGNAL\_STATUS whenever it detects the beginning or end of Collision Presence. The PLS sublayer sends SIGNAL\_ERROR when it receives *input* message CVL or CVH from the PMA sublayer and the previous SIGNAL\_STATUS the PLS sublayer sent was NO\_SIGNAL\_ERROR. The PLS sublayer sends NO\_SIGNAL\_ERROR when it receives an *input\_idle* message from the PMA sublayer and the previous SIGNAL\_STATUS that the PLS sent to the MAC sublayer was SIGNAL\_ERROR. The PLS shall send SIGNAL\_ERROR to the MAC sublayer when the Collision Presence pattern is detected; it may send SIGNAL\_ERROR any time it receives an *input* message that is neither CD0 nor CD1.

**12.3.2.3 PLS Functions.** The PLS sublayer functions consist of four simultaneous and asynchronous functions. These functions are Output, Input, Error Sense, and Carrier Sense. All of the four functions are started immediately following PowerOn. These functions are depicted in the state diagrams shown in Fig 12-8 through Fig 12-9, using the notation described in 1.2.1.

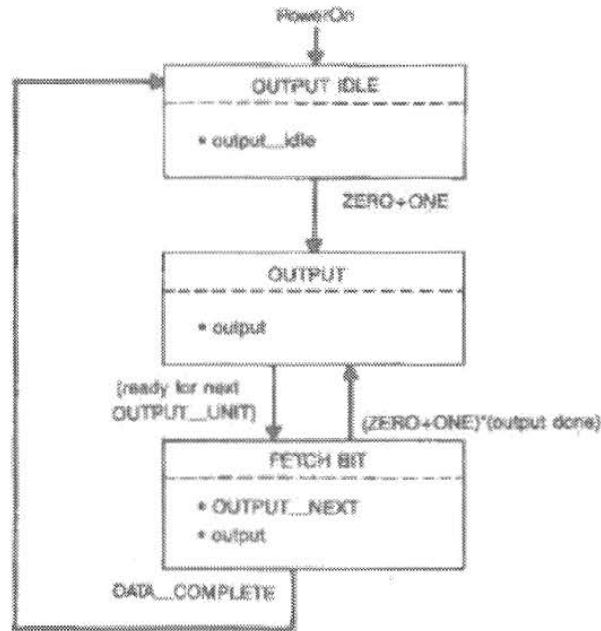


Fig 12-6  
DTE PLS Output Function

**12.3.2.3.1 State Diagram Variables.** The variables used in the state diagrams and the corresponding descriptions are the following:

*(1) Inter Process Flags*

- |                                   |  |
|-----------------------------------|--|
| <code>disable_SIGNAL_ERROR</code> | Used in the state diagrams and functions. It is used by the Input Function to prevent false collision detection by the Error Sense Function during preamble startup.                               |
| <code>protectTimer</code>         | Used by the Carrier Sense Function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer." "protectTimer_done" is satisfied when the timer has expired. |

**12.3.2.3.2 Output Function.** The Output Function transparently performs the task of data transfer from the MAC sublayer to the PMA sublayer. The state diagram of Fig 12-6 depicts the Output Function operation.

**12.3.2.3.3 Input Function.** The Input Function transparently performs the task of data transfer from the PMA sublayer to the MAC sublayer. The state diagram of Fig 12-7 depicts the Input Function operation.

**12.3.2.3.4 Error Sense Function.** The Error Sense Function performs the task of sending `SIGNAL_STATUS` to the MAC sublayer at the beginning and end of the Collision Presence pattern. The state diagram of Fig 12-8 depicts the Error Sense Function operation.

**12.3.2.3.5 Carrier Sense Function.** The Carrier Sense Function performs the task of sending `CARRIER_STATUS` to the MAC sublayer whenever the input becomes active or idle, as detected by the PMA sublayer. The state diagram of Fig 12-9 depicts the Carrier Sense Function operation.

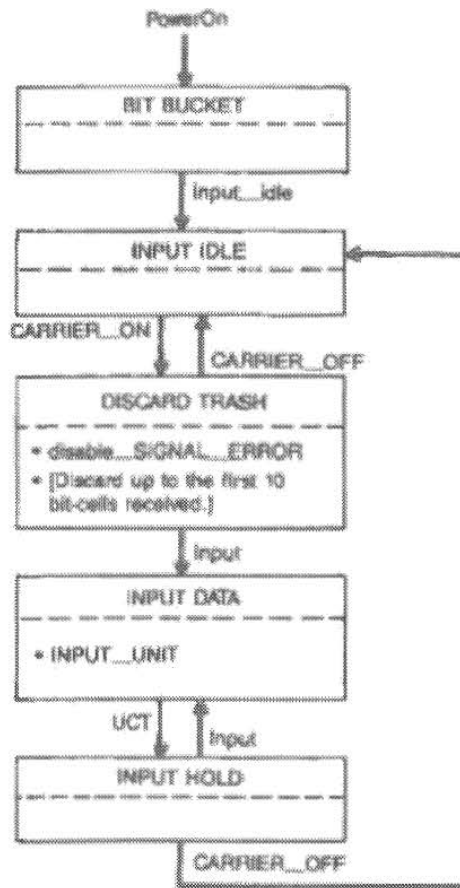


Fig 12-7  
DTE PLS Input Function

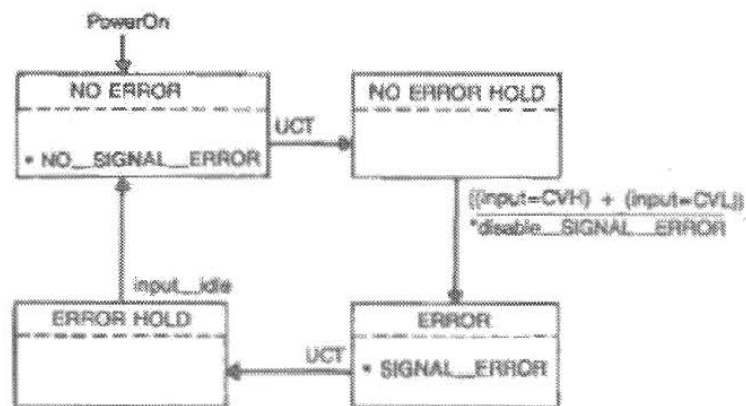


Fig 12-8  
DTE PLS Error Sense Function



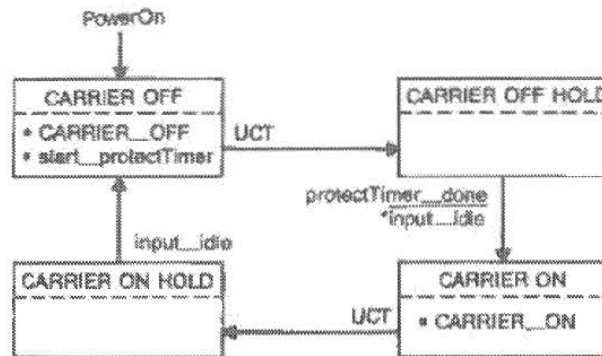


Fig 12-9  
DTE PLS Carrier Sense Function

A timer may be used by the Carrier Sense Function to implement the protection period described in 12.5.3.2.3. It is started by "start-protectTimer" and asserts "protectTimer\_done" after 0 to 30  $\mu$ s since starting.

**12.3.2.4 Signal Encoding.** Five distinct symbols can be transmitted on the line: CD0, CD1, CVL, CVH, and IDL. Of these, CVL and CVH are transmitted only as part of the collision presence reporting pattern CP.

**12.3.2.4.1 Data Transmission Rate.** The data transmission rate (BR) is 1 Mb/s  $\pm$  0.01%. A bit time (BT) is therefore nominally 1  $\mu$ s.

**12.3.2.4.2 Data Symbol Encoding.** Manchester encoding is used for the transmission of packets. Manchester encoding is a binary signaling mechanism that combines data and clock into bit cells. Each bit cell is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit cell. During the first half of the bit cell, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit cell, the encoded signal is the uncomplemented value of the bit being encoded. Thus, a CD0 is encoded as a bit cell in which the first half is HI and the second half is LO. A CD1 is encoded as a bit cell in which the first half is LO and the second half is HI. Examples of Manchester waveforms are shown in Fig 12-10. The zero crossings of an ideal Manchester waveform occur on precise half-bit-cell boundaries. The zero crossings of real waveforms may include timing jitter that causes deviation from these "idealized zero crossings."

**12.3.2.4.3 Collision Presence Encoding.** Two signals, CVL and CVH, that are transmitted only as part of the collision presence reporting pattern, CP, violate the normal Manchester encoding rule requiring a transition in the middle of each symbol. A CVH is encoded as a transition from LO to HI at the beginning of the bit cell, HI for the entire bit cell, and transition from HI to LO at the end of the bit cell. A CVL is encoded as a transition from HI to LO at the beginning of the bit cell, LO for the entire bit cell, and transition from LO to HI at the end of the bit cell.

The Collision Presence reporting signal, CP, is a special sequence that differs from any legitimate Manchester-encoded signal. CP is encoded as a repeating sequence of 1 bit time LO, 1/2 bit time HI, 1 bit time LO, 1 bit time HI, 1/2 bit time LO, and 1 bit time HI. This may also be interpreted as repetitions of the five-symbol sequence CVL, CD0, CD1, CD0, CVH. Should a transmitter's or receiver's timing be shifted by 1/2 bit time, then the same sequence will be interpretable as repetitions of CD1, CVL, CVH, CD1, CD0. In either case, the presence of non-Manchester symbols distinguishes the sequence from data. Examples of

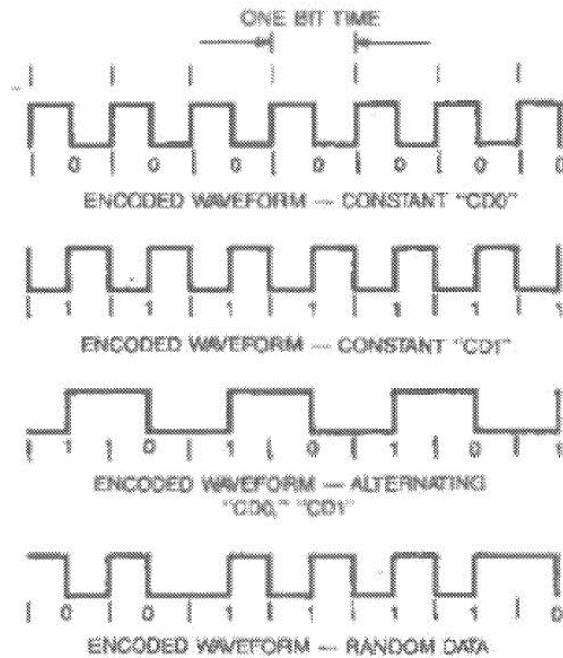


Fig 12-10  
 Examples of Manchester Waveforms

Collision Presence waveforms are shown in Fig 12-11. See 12.8.2.2.5 and 12.4.3.2 for further details on the detection and generation of CP.

NOTE: CP is the minimal length sequence that meets the following design criteria:

- (1) The sequence should not look like legitimate Manchester encoded data even if the receiver does not lock onto the correct bit-cell boundaries.
- (2) The sequence should maintain overall dc balance. That is, it should be HI 50% of the time and LO the other 50%.
- (3) The signal should occupy the same part of the frequency spectrum as normal data. That is, transitions should occur every half or whole bit time so that the fundamental signaling frequencies of BR/2 and NR are maintained. Furthermore, allowing more than one bit time to pass without a transition would introduce ambiguity with the idle line condition (IDL).

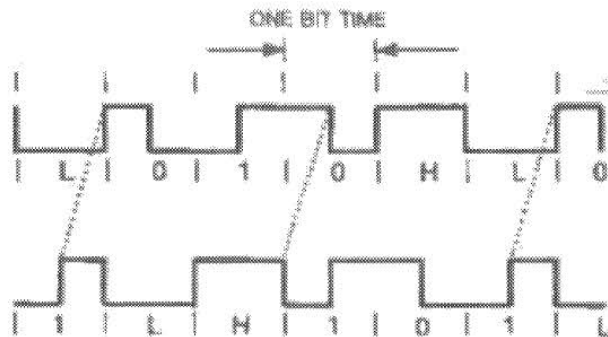
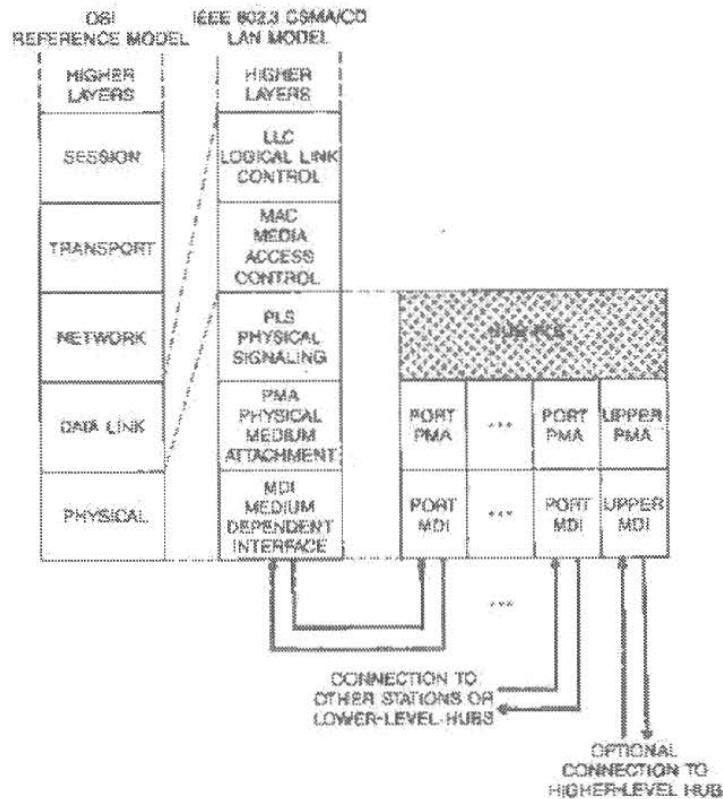


Fig 12-11  
 Examples of Collision Presence Waveforms

**12.3.2.4.4 Idle Line Encoding.** The line condition IDL is also used as an encoded signal. An IDL always starts with a HI signal level. Since IDL always starts with a HI signal, an additional transition will be added to the data stream if the last bit sent was a zero. This transition cannot be confused with clocked data (CD0 or CD1) since the transition will occur at the start of a bit cell. There will be no transition in the middle of the bit cell. The HI signal level, as sent by a transmitter, shall be maintained for a minimum of 2 bit times.

## 12.4 Hub Specification

**12.4.1 Overview.** This section defines the logical characteristics of the hub used in 1BASE5. The relationship of this specification to the entire standard is shown in Fig 12-12.



**Fig 12-12**  
Hub Relationship to the OSI Reference Model  
and the IEEE 802.3 CSMA/CD LAN Model

### 12.4.1.1 Summary of Major Concepts

- (1) A hub consists of a Hub PLS sublayer and a number of instances of the PMA sublayer.
- (2) One instance of the PMA sublayer, the "upper PMA," provides a connection to a higher-level hub. This PMA is not required for the header hub.
- (3) Each of the remaining instances of the PMA sublayer, called "port PMAs," provides a connection to a DTE or a lower-level hub.

- (4) The Hub PLS transfers data in two directions: upward from the port PMA's, to the upper PMA and downward from the upper PMA to the port PMA's.
- (5) The upward and downward "sides" of the hub operate independently and simultaneously.

**12.4.1.2 Application Perspective.** The hub is a physical layer entity that performs two functions:

- (1) It retransmits incoming signals with amplitude and timing restored.
- (2) It detects collisions between any two or more ports and reports knowledge of the collision by transmitting a special collision presence reporting pattern.

**12.4.2 Hub Structure.** Each hub is functionally divided into two parts: the upward side and the downward side. The upward side is responsible for combining the transmissions from DTEs and hubs lower in the network into a single transmission to the next level up. The downward side is responsible for distributing the combined signal (which is wrapped around from the upward side of the header hub) to each of the DTEs and hubs below. Except as specified in 12.4.3.2.3 and 12.4.2.6, the two sides function independently.

There is an upward input channel and a corresponding downward output channel for each DTE or hub immediately below the hub. Although there is no electrical connection between the two lines, they do share a connector and cable (see 12.6 and 12.7) and are collectively known as a hub port. Each port is accessed through an instance of the PMA sublayer referred to as a "port PMA."

The one output channel from the upward side and the one input channel to the downward side of a hub are similarly paired and, for all but the header hub, are connected to a port of the next-higher-level hub. They are accessed through an instance of the PMA sublayer referred to as the "upper PMA."

NOTE: A hub that includes *n* hub ports should be called an *n*-port hub, even though it may have an extra jack for the upper PMA. The latter connection should never be counted as a port, despite common engineering usage, because it does not meet the specific definition of a 10BASE5 hub port given above.

**12.4.2.1 Upward Side.** The primary function of the upward side of a hub is to propagate signals from each of its inputs to its single output. If more than one input is active, then the Collision Presence signal CP is transmitted instead. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

**12.4.2.2 Downward Side.** The primary function of the downward side of a hub is to repeat signals from its one input to each of its outputs. In addition, the signals are retimed to restore the transitions to half-bit-time boundaries; see 12.4.3.2.5 for the details of retiming.

**12.4.3 Hub PLS Functional Specification.** This section provides a detailed model for the Hub PLS sublayer.

**12.4.3.1 Hub PLS to PMA Interface.** The interface between the Hub PLS and the PMA is the same as that specified in 12.3.2.1 for use between the DTE PLS and the PMA except that the *output* message from the Hub PLS to the PMA is used to transmit CVL and CVH in addition to CD0 and CD1.

**12.4.3.2 Hub PLS Functions.** The Hub PLS sublayer functions consist of three asynchronous functions. These functions are Upward Transfer, Jabber, and Downward Transfer. All three functions are started immediately following PowerOn; an independent copy of the Jabber function is started for each port PMA. These functions are depicted in the state diagrams shown in Fig 12-13 through Fig 12-15, using the notation described in 1.2.1.

**12.4.3.2.1 State Diagram Variables.** The variables used in the state diagrams and the corresponding descriptions are the following:

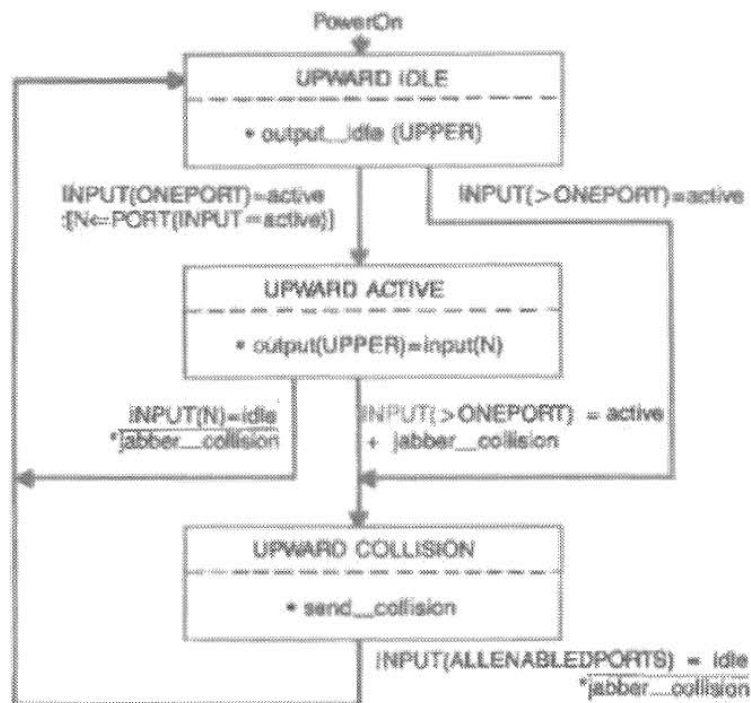
- (1) *Port Designators:* Instances of the PMA sublayer are referred to by index. PMA information is obtained by replacing the X in the desired function with the index of the PMA of interest. Furthermore, PMA's may be referenced by several special designators used as indices:

X                                      Generic port PMA designator. When X is used in a state diagram its value indicates the particular instance of a generic function.

UPPER	Indicates the upper PMA.
ALLPORTS	Indicates that all port PMAs are to be considered. All port PMAs must meet a test condition in order for that test to pass.
ALLENABLEDPORTS	Indicates that all port PMAs that are not disabled by the Jabber Function are to be considered. All such port PMAs must meet a test condition in order for that test to pass.
ONEPORT	Indicates that all port PMAs that are not disabled by the Jabber Function are to be considered. One, but not more than one, such port PMA must meet a test condition in order for that test to pass.
>ONEPORT	Indicates that all port PMAs that are not disabled by the Jabber Function are to be considered. Two or more such port PMAs must meet a test condition in order for that test to pass.
N	Defined by the PORT function on exiting from the UPWARD IDLE state of Fig 12-13. It indicates which port PMA caused the exit from the UPWARD IDLE state.
(2) <i>Port Functions:</i>	
PORT(TestCondition)	Returns the index of a port PMA passing the indicated test condition. If multiple port PMAs meet the test condition, the PORT function will return one and only one of the acceptable values.
(3) <i>Input Variables:</i>	
INPUT(X)	Indicates the state of activity on the designated PMA input channel. It may be either "idle" or "active." The former indicates that <i>input_idle</i> is asserted; the latter indicates that it is not asserted.
input(X)	Used to receive an <i>input</i> message (see 12.3.2.1) from the designated PMA input channel.
probation_alternative	Used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Fig 12-14 when an active port becomes idle. The implementor of a hub may treat the variable as either true or false.
(4) <i>Output Variables:</i>	
output(X)	Used to send an <i>output</i> message (see 12.3.2.1 and 12.4.3.1) to the designated PMA output channel.
output_idle(X)	Used to send an <i>output_idle</i> message (see 12.3.2.1) on the designated PMA output channel.
(5) <i>Inter Process Flags:</i>	
send_collision	Used by the Upward Signal Transfer Function to indicate a series of <i>output</i> messages to the upper PMA sublayer, the effect of which is to transmit the CP signal, as described in 12.3.2.4.2, 12.3.2.4.3, and 12.4.3.2.7.
jabber_collision	Used by the various instances of the Jabber Function to signal the Upward Signal Transfer Function that CP should be generated.
disable_input(X)	Used to disable the designated PMA input channel. The input is re-enabled when <i>disable_input(X)</i> is no longer asserted. Only the Upward Signal Transfer Function is affected by the disabling of a port (via the ALLENABLEDPORTS, ONEPORT, and >ONEPORT designators).

jabberTime1	Used by the Jabber Function (see 12.4.3.2.3) to detect excessively long transmissions. It is started by "start_jabberTime1." "jabberTime1_done" is satisfied when the timer has expired.
jabberTime2	Used by the Jabber Function (see 12.4.3.2.3) to determine when to disable ports due to excessively long transmissions. It is started by "start_jabberTime2." "jabberTime2_done" is satisfied when the timer has expired.

**12.4.3.2.2 Upward Signal Transfer Function.** The Upward Signal Transfer Function combines signals from the various port inputs and passes them on to the upper output. It also detects and reports collisions as appropriate. The state diagram of Fig 12-13 depicts its operation.



**Fig 12-13**  
**Hub PLS Upward Transfer Function**

Signals are propagated upward according to the following rules, except as controlled by the Jabber Function (see 12.4.3.2.3):

- (1) If IDL is present on all port inputs, then transmit IDL.
- (2) If IDL is present on all but one of the port inputs, then repeat the signal received from that one line. If that one signal is CP, then a hub may generate its own CP signal instead of repeating the received CP signal.
- (3) If two or more inputs are active (non-IDL) at the same time, then transmit CP and continue transmitting CP until all inputs indicate IDL again.

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

**12.4.3.2.5 Jabber Function.** The Jabber Function detects abnormally long transmissions and takes appropriate action to abort them. The state diagram of Fig 12-14 depicts its operation.

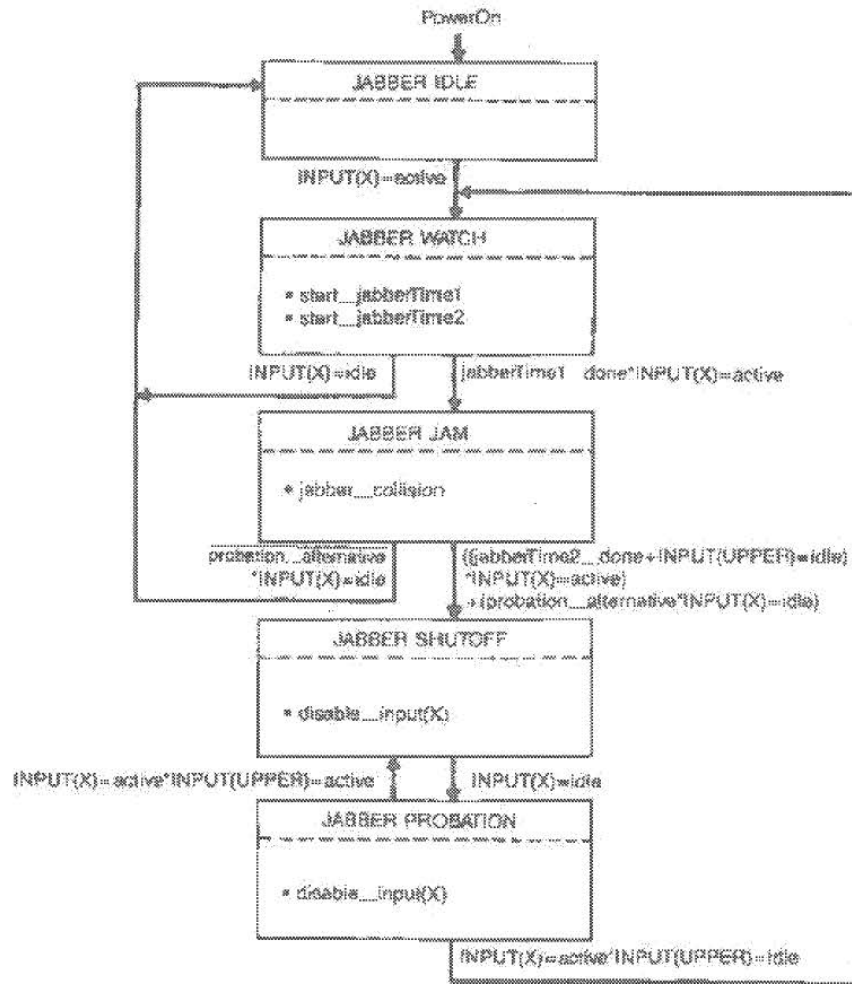


Fig 12-14  
Hub PLS Jabber Function for Port X

Two timers are used by the Jabber Function. They may be implemented either as local timers for each instance of the Jabber Function or as global timers shared by all instances. Furthermore, because the two timers are always started concurrently, an implementation may share circuitry between the two.

The first timer is started by "start\_jabberTime1" and asserts "jabberTime1\_done" after 25 to 50 ms since starting. If implemented as a single global timer, assertion of start\_jabberTime1 by any instance of the Jabber Function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance.

Similarly, the second timer is started by "start\_jabberTime2" and asserts "jabberTime2\_done" after 51 to 100 ms since starting. If implemented as a single global timer, assertion of start\_jabberTime2 by any instance of the Jabber Function with any other instance(s) still waiting for that timer shall not restart the timer, thereby shortening the waiting period for the latest instance. Furthermore, if this second timer is implemented as a single global timer, then assertion of start\_jabberTime1 by any instance of the Jabber Function with any other instance(s) still waiting for just the second timer (in the JABBER JAM state) shall

be treated as if the first timer expires immediately (asserting `jabberTime1_done`) for the latest instance, thereby causing that instance to join the other instance(s) waiting for the second timer.

Hardware within the upward side of a hub shall provide a *window* of 25 to 50 ms, during which time a normal packet or CP sequence may be propagated upward. If any port input (or, as an alternative implementation, the hub's combined upward signal) exceeds this duration without becoming idle, then the hub shall switch to transmitting CP until 51 to 100 ms after the beginning of the window and then, if that input is still active, disable that input (or all nonidle inputs) until it once again becomes active while the downward side is idle.

The "probation\_alternative" input variable is used to distinguish between the two allowed alternatives for exiting the JABBER JAM state of Fig 12-14 when an active port becomes idle. The implementor of a hub may treat the variable as either true or false. If true, the port will enter the JABBER PROBATION state (via the JABBER SHUTOFF state); if false, the port will instead return to the JABBER IDLE state.

**12.4.3.2.4 Downward Signal Transfer Function.** The Downward Signal Function repeats signals from the upper input to the various port outputs. The state diagram of Fig 12-15 depicts its operation.

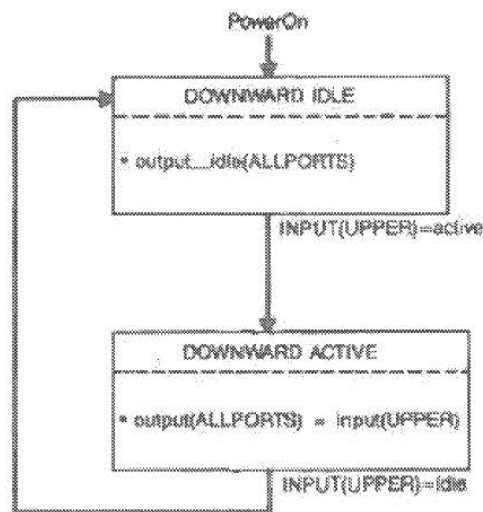


Fig 12-15  
Hub PLS Downward Transfer Function

The downward side of a hub may detect the Collision Presence signal at the upper input and generate its own CP signal to be transmitted at the port outputs (in place of repeating the received CP signal).

Whenever the hub finishes transmitting CP, it shall then transmit IDL, including the extended HI period.

**12.4.3.2.5 Retiming (Jitter Removal).** Each side of each hub shall retime any clocked signals that it propagates so that the transitions occur on half-bit-time boundaries, thereby avoiding accumulation of excessive jitter. Such retiming shall preserve the sequence of CD0, CD1, CVL, and CVH symbols being propagated.

If an ambiguity exists in the incoming bit cells due to excessive noise or jitter, then the appropriate side of the hub may either switch to generating CP or replace the erroneous bit cell with an arbitrary combination of half or whole bit cells.

Retiming also accounts for differences (if any) in clock rates between that used to send bit cells to the hub and that used to send them out from the hub. Excessive differences in clock rates (caused by clocks not meeting 12.3.2.4.1) and excessively long packets (caused by exceeding `maxFrameSize`) may each cause the capacity of the retiming function to be exceeded. In such circumstances, the appropriate side of the hub may either switch to transmitting CP or add or delete half or whole bit cells as needed.



Whenever bit cells are added, deleted, or replaced, the hub shall maintain synchronization of the outgoing bit cells to a half or whole bit cell boundary. Furthermore, it shall not generate periods of more than one bit time without a transition.

**12.4.3.2.6 Header Hub Wrap-Around.** For each particular network configuration, one hub operates as the header hub and all others as intermediate hubs. It is suggested, but not required, that hub implementations be capable of being used for either purpose. Methods for switching between these two modes are beyond the scope of this standard.

For an intermediate hub, the upper output shall be connected to a port input of the next higher-level hub and the upper input shall be connected to a port output of a higher-level hub.

For the header hub, the upper output shall be connected to the upper input. This wraparound may appropriately bypass parts of the PMA specification so long as the resulting implementation is functionally equivalent to one with a wired connection. For example, signals internal to the hub need not be translated to the corresponding external levels and then translated back to internal levels. Similarly, it shall not be necessary to retime the wrapped signal twice, once in the upward side and then again in the downward side of the same header hub; a single retiming is permissible.

**12.4.3.2.7 Collision Presence Startup.** When a hub starts generating CP (as specified in 12.4.3.2.2 through 12.4.3.2.5) it shall synchronize the startup to a half or whole bit-cell boundary of any immediately preceding signal. If it was sending IDL immediately before the CP, no synchronization or preamble is required.

A hub may start transmission of CP at any point in the sequence that does not result in periods of more than one bit time without a transition during the switch from passing on data to sending CP. Depending on the preceding signal, it may start with L010H, 010HL, 10HL0, 0HL01, or HL010. Because startup may be synchronized to any half-bit-cell boundary, a hub may also transmit the shifted version of CP starting with 1LH10, LH101, H101L, 101LH, or 01LH1.

**12.4.3.3 Reliability.** Hubs shall be designed to provide a mean time between failure (MTBF) of at least 45 000 hours of operation. Hubs, including the associated connectors and other passive components, should be designed to minimize the probability that a particular failure results in total network failure. Furthermore, the port electronics of each hub should be designed so as to minimize the probability that the failure of one port prevents communication by equipment attached to the other ports.

## 12.5 Physical Medium Attachment (PMA) Specification

**12.5.1 Overview.** This section defines the Physical Medium Attachment (PMA) sublayer for 1BASE5. The relationship of this specification to the entire standard is shown in Fig 12-16. The PMA sublayer connects the PLS sublayer to the Medium Dependent Interface (MDI).

**12.5.2 PLS-PMA Interface.** The interface between the PLS and the PMA sublayers is specified in 13.3.2.1 for DTEs and in 12.4.3.1 for hubs.

### 12.5.3 Signal Characteristics

**12.5.3.1 Transmitter Characteristics.** Transmitters should operate properly when loaded with any cable meeting the requirements of 12.7. To approximate the boundary conditions of such loading, two specific test loads are specified. Transmitters shall meet all requirements of this section when connected to both the "light" (115  $\Omega$ ) load shown in Fig 12-17 and the "heavy" (approximately 80  $\Omega$ ) load shown in Fig 12-18. It is expected that transmitters that perform correctly with these two loads will also perform acceptably under intermediate loading conditions.

**12.5.3.1.1 Differential Output Voltage.** For simplicity of explanation, the text and figures of this section describe the differential output voltage in terms of voltage magnitudes. The requirements of this section apply to the negative pulses as well as the positive ones.

Beginning with the second bit of the preamble (or CP, if no preamble is present), pulses of duration  $BT/2$  shall meet the conditions of Fig 12-19. Pulses of duration  $BT$  shall meet the conditions of Fig 12-20. After the zero-crossing, the output shall exceed the voltage of a signal rising from the zero-crossing to 2.0 V with

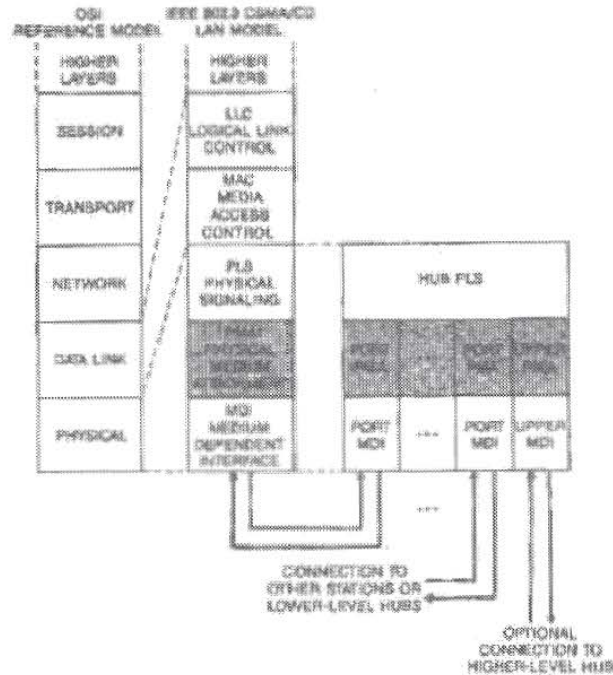


Fig 12-16  
Physical Medium Attachment, Relationship to the OSI Reference Model  
and the IEEE 802.3 CSMA/CD LAN Model



Fig 12-17  
Simulated Light Load

a slope of magnitude 20 mV/ns. The output shall remain above 2.0 V until 100 ns before the next, zero-crossing. The peak output voltage shall not exceed 3.65 V. While falling from 2.0 V to the zero-crossing, the signal shall exceed the voltage of a signal falling from 2.0 V to the zero-crossing with a slope of magnitude 20 mV/ns.

For pulses of duration  $BT$ , the average voltage that appears from 100 ns after the zero-crossing through  $BT/2$  shall be between 0.95 and 1.8 times the average voltage that appears from time  $BT/2$  through 100 ns before the following zero-crossing. Similarly, for pulses of duration  $BT$ , the peak voltage that appears from 100 ns after the zero-crossing through  $BT/2$  shall be between 0.95 and 1.8 times the peak voltage that appears from time  $BT/2$  through 100 ns before the following zero-crossing.

NOTE: The purpose of the above restrictions on average and peak voltages is to avoid transmitter waveforms that peak excessively during the second half of signals of duration  $BT$ , resulting in excessive jitter at the receiver. Some equalization to produce slight droop in the second half of signals of duration  $BT$ , on the other hand, may help decrease jitter at the far end of long cables.

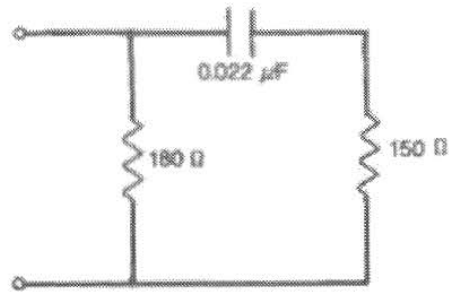


Fig 12-18  
Simulated Heavy Load

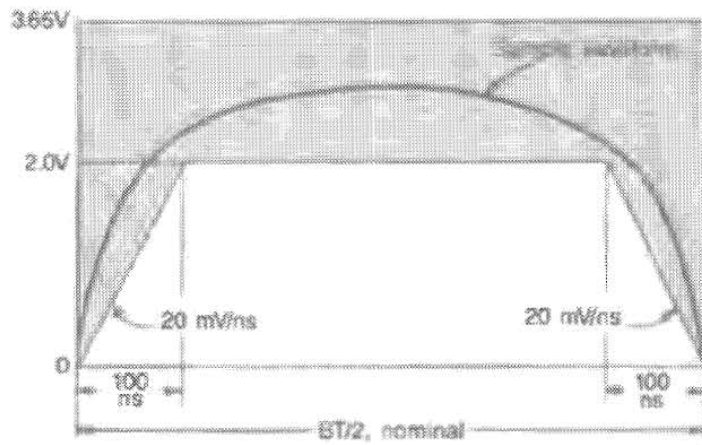


Fig 12-19  
Differential Output Voltage, Nominal Duration BT/2

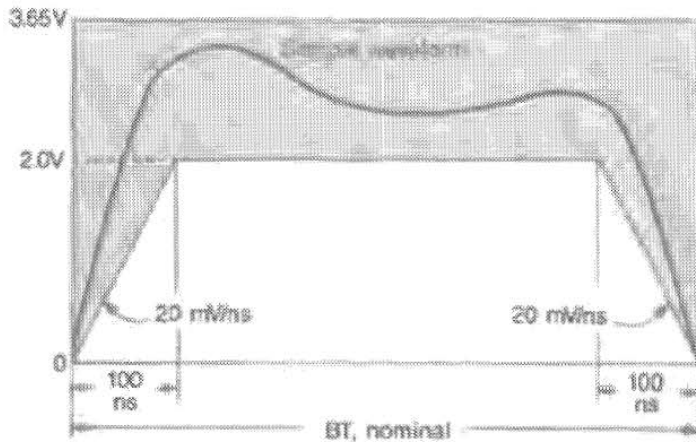


Fig 12-20  
Differential Output Voltage, Duration BT

The amplitude of the power spectrum at the output of the transmitter for all possible sequences of signals shall not exceed that produced by an idealized transmitter sending corresponding rectangular waveforms with magnitude 365 V at any frequency.

When a transmitter enters the idle state, it shall maintain a minimum differential output voltage of 2.0 V from 100 ns through 2BT after the last low-to-high transition, as illustrated in Fig 12-21. The differential output voltage shall then fall to 1.1 V within 3BT after that same low-to-high transition. Starting when the differential output voltage first reaches 1.1 V, the magnitude of the output voltage driven into the test loads indicated in Figs 12-22 and 12-23 shall then remain within the limits indicated in Fig 12-21 until the transmitter leaves the idle state.

The transmitter output at the start of idle may exhibit overshoot, ringing, slow voltage decay, or a combination thereof due to the following factors:

- (1) Change in transmitter source impedance between the active and idle states
- (2) Difference in the magnitudes of the differential output voltage between the high and low output states ( $\Delta V_{OD}$ )
- (3) Waveform asymmetry at the transmitter ( $\Delta T$ )
- (4) Transmitter and receiver (transformer) inductance (L)

NOTE: The contribution to the undershoot from each of these can be computed with the following equations:

$$V_{\Delta V_{OD}} = \pm \Delta V_{OD} \cdot R_{OFF} / 2R_{ON}$$

$$V_{\Delta T} = (\Delta T / 1000 \text{ ns}) \cdot V_P \cdot R_{OFF} / R_{ON}$$

$$V_L = V_P \cdot \left( 1 - e^{-4.76 \mu\text{s}(L/R_{ON})} \right) \cdot R_{OFF} / R_{ON}$$

where:

$$R_{OFF} = R_{SRC-OFF} \parallel R_L$$

$$R_{ON} = R_{SRC-ON} \parallel R_L$$

$R_{SRC-OFF}$  = source impedance ( $\Omega$ ) when the driver is off

$R_{SRC-ON}$  = source impedance ( $\Omega$ ) when the driver is on

$R_L$  = load impedance ( $\Omega$ )

$L_P$  = combined inductance ( $\mu\text{H}$ ) of the transmitter and receiver transformers

$\Delta V_{OD}$  = difference (V) in magnitude of the HI and LO output voltages

$\Delta T$  = asymmetry of the waveform equals the difference between the average HI and average LO pulse widths (ns) at the transmitter

$V_P$  = maximum output voltage (V) during the start of IDLE

NOTE: The waveform shown in Fig 12-21 and the equations in the preceding note apply to a transmitter connected to the test loads of Figs 12-22 and 12-23. An actual receiver may present a more complex termination impedance and so the undershoot or overshoot may exceed that encountered with the test loads.

**12.5.3.1.2 Output Timing Jitter.** The transmitted signal zero-crossings shall deviate from the idealized zero-crossings by no more than  $\pm 10$  ns.

**12.5.3.1.3 Transmitter Impedance Balance.** The longitudinal to metallic impedance balance of the transmitter, defined as  $20 \log_{10}(E_{\text{ext}}/E_{\text{diff}})$ , where  $E_{\text{ext}}$  is an externally applied ac voltage, as shown in Fig 12-24, shall exceed 44 dB at all frequencies up to and including 4BR in the idle and nonidle states.

NOTE: It may be difficult to measure the transmitter impedance balance in the nonidle state. A frequency-selective wavemeter or other measurement technique may be required. Furthermore, the balance of the test equipment (such as the matching of the 400  $\Omega$  resistors) must exceed that required of the transmitter.

**12.5.3.1.4 Common-Mode Output Voltage.** The magnitude of the total common-mode output voltage of the transmitter,  $E_{\text{cm}}$ , measured as shown in Fig 12-25, shall not exceed 300 mV.

NOTE: The implementor should consider any applicable local, national, or international regulations and standards concerning HF emission. Driving unshielded twisted pairs with high-frequency common-mode voltages may result in interference to other equipment.

**12.5.3.1.5 Common-Mode Tolerance.** Transmitters shall meet the requirements of 12.5.3.1.1 and 12.5.3.1.2 even in the presence of common-mode sinusoidal voltage,  $E_{\text{cm}}$  (as shown in Fig 12-26), of  $\pm 20$  V peak at frequencies from 40 kHz through 6BR.

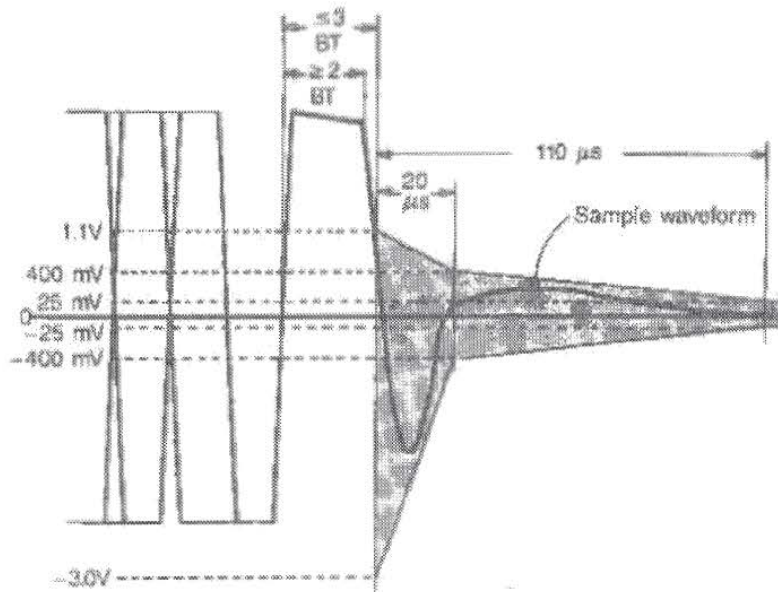


Fig 12-21  
Transmitter Waveform for Idle

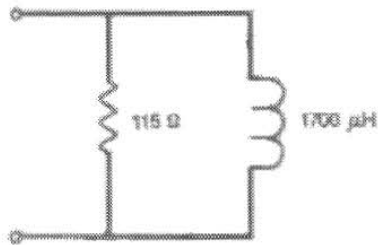


Fig 12-22  
Start-of-Idle Test Load #1

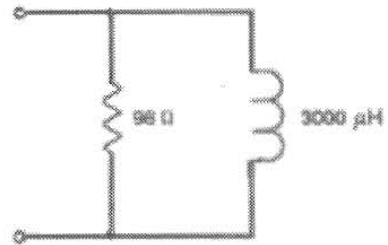


Fig 12-23  
Start-of-Idle Test Load #2

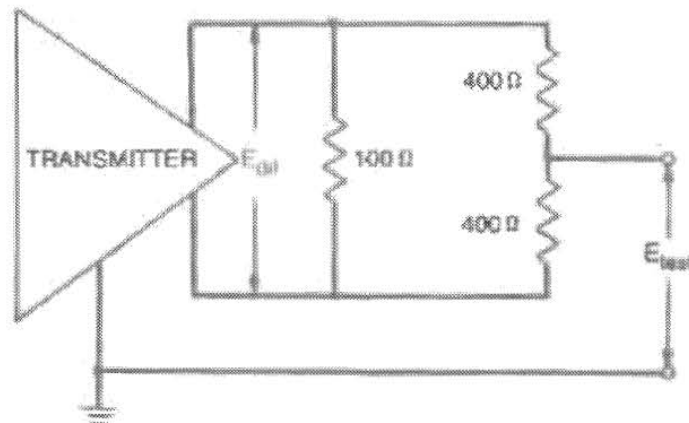


Fig 12-24  
Transmitter Impedance Balance

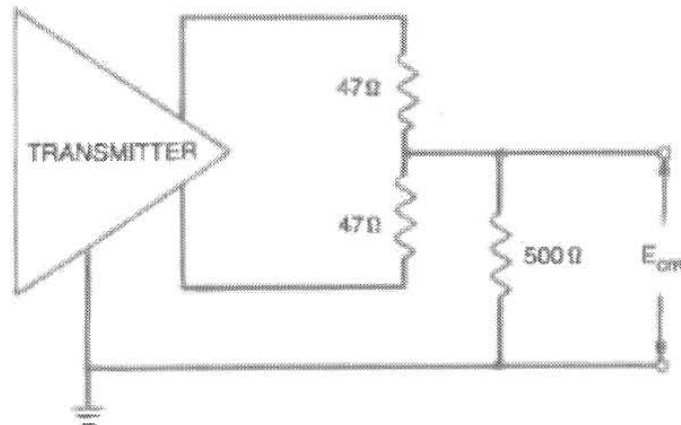


Fig 12-25  
Common-Mode Output Voltage

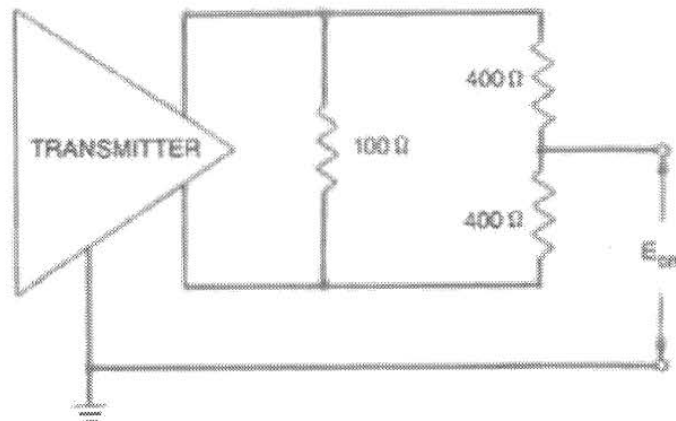


Fig 12-26  
Transmitter Common-Mode Tolerance

**12.5.3.1.6 Transmitter Fault Tolerance.** Transmitters, both when idle and when nonidle, shall tolerate the application of short circuits across their outputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, both when idle and when nonidle, shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Fig 12-27. The shape of the impulse shall be 0.3/50  $\mu$ s (300 ns virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 (see Reference [11]).

NOTE: Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that section are mandatory.

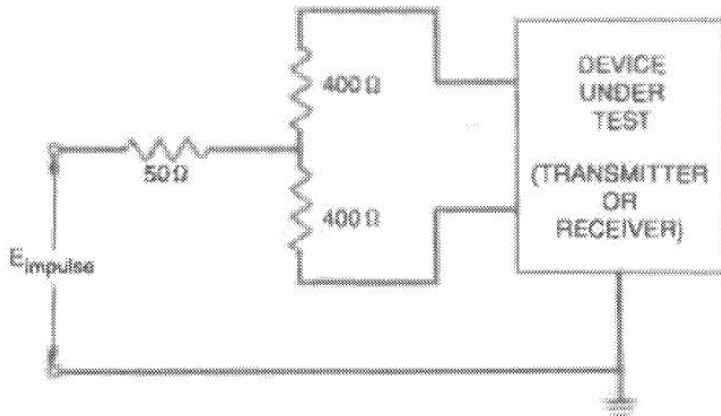


Fig 12-27  
Common-Mode Impulse Test

12.5.3.2 Receiver Characteristics

**12.5.3.2.1 Differential Input Voltage.** The receiver shall operate properly when a signal meeting the minimum magnitude requirements of Fig 12-28 is received. When less than 300 mV, the magnitude of the voltage will exceed that of a straight line through the nearest zero-crossing with slope of magnitude 9 mV/ns. That is, the average slow rate near each zero-crossing will exceed 9 mV/ns. The magnitude of the voltage will also remain at or above 1.0 V for some period lasting at least 150 ns (650 ns for pulses of duration BT) that starts within 250 ns of the preceding zero-crossing and its peak will be at least 1.1 V.

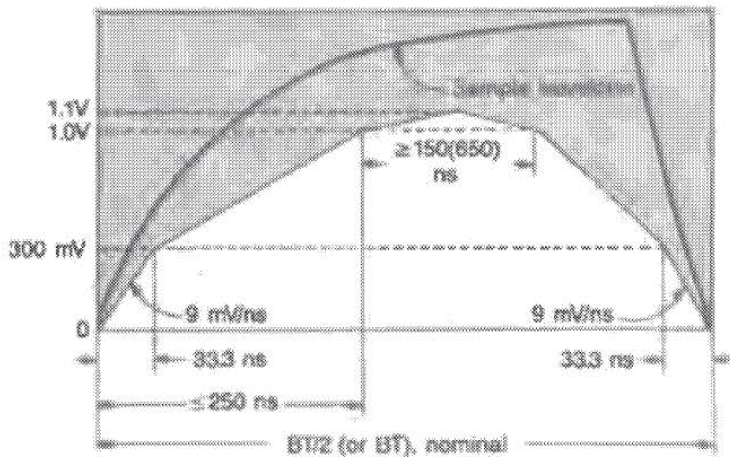


Fig 12-28  
Receiver Signal Envelope

**12.5.3.2.2 Input Timing Jitter.** Receivers shall operate properly with zero-crossing jitter of up to  $\pm 32$  ns from the ideal.

**12.5.3.2.3 Idle Input Behavior.** The IDL condition shall be detected within 1.5 bit times of the last low-to-high transition at the receiver.

NOTES: (1) It is necessary to distinguish CVH from IDL.

(2) System jitter considerations make it impractical to detect IDL (end-of-cable, end-of-transmission delimiter) any sooner than 1.5 bit times. The specific implementation of the clock recovery mechanism, or equivalent, determines the lower bound on the actual IDL detection time. Adequate margin should be provided between the lower bound and 1.5 bit times.

The receiver shall take precautions to ensure that the HI-to-silence transition of the start of IDL is not falsely interpreted as a silence-to-nonidle transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, cable, and receiver, including those discussed in 12.5.3.1.1.

To this end, a receiver in a hub shall treat its input as if it were idle for between 20 and 30  $\mu$ s after detecting IDL. The timing of this "protection" period for the port PMAs may use a single timer that is started when all ports have become idle or disabled by the Jabber Function. Receivers in DTEs may include a similar protection period of up to 30  $\mu$ s.

NOTE: The protection period is required in hubs because erroneously interpreting the start-of-idle as a new transmission will result in propagation of the error to DTEs, despite any precautions taken in those DTEs. The protection period is optional in DTEs because any implementation error in a DTE will affect only that particular DTE.

**12.5.3.2.4 Differential Input Impedance.** The (complex) differential input impedance of the receiver,  $Z_{\text{receiver}}$ , shall be such that the reflection attenuation, defined as  $20 \log_{10} (|Z_{\text{receiver}} + Z_{\text{cable}}| / |Z_{\text{receiver}} - Z_{\text{cable}}|)$ , where  $Z_{\text{cable}}$  is the differential characteristic impedance of the attached cable, exceeds 16 dB over the range BR/2 through 2BR for all cables meeting the requirements of 12.7.2.

**12.5.3.2.5 Common-Mode Rejection.** Receivers shall assume the proper output state for any differential input signal,  $E_{\text{diff}}$ , that results in a signal,  $E_{\text{diff}}$ , that meets 12.5.3.2.1 and 12.5.3.2.2, even in the presence of common-mode sinusoidal voltages,  $E_{\text{cm}}$ , (as shown in Fig 12-29), of  $\pm 20$  V peak at frequencies from 40 kHz through 6BR.

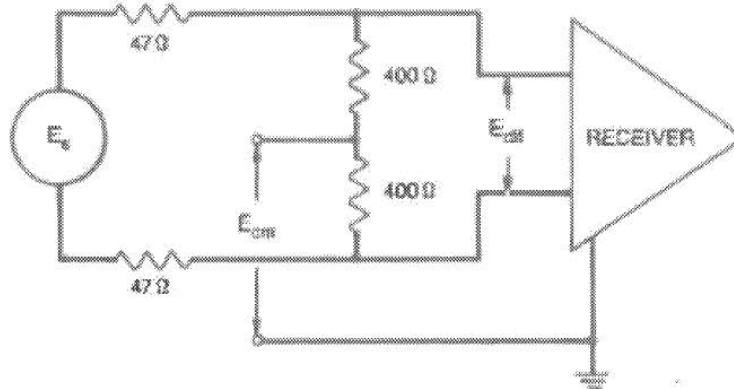


Fig 12-29  
Receiver Common-Mode Rejection

**12.5.3.2.6 Noise Immunity.** Receivers shall meet the following limits on average error rates when the noise described in 12.7.4 is added to the signals described in 12.5.3.2.1 and 12.5.3.2.2:

- (1) When nonidle, the receiver error rate shall not exceed one error in  $10^8$  bits.
- (2) When idle, a receiver used in a DTE shall not falsely detect carrier more than one in 100 s.
- (3) When idle, a receiver used in a hub shall not falsely detect carrier more than once in 1500 s.

NOTE: Receivers whose inputs include a 2-4 MHz, 3-pole, low-pass, Butterworth filter and a 360 mV squelch level will meet this last requirement for idle-mode noise immunity yet still perform properly with the weakest signal allowed by 12.5.3.2.1.



**12.5.3.2.7 Receiver Fault Tolerance.** Receivers shall tolerate the application of short circuits across their inputs for an indefinite period of time without damage and shall resume normal operation after such faults are removed.

Receivers shall withstand, without damage, a 1000 V common-mode impulse of either polarity, applied as indicated in Fig 12-27. The shape of the impulse shall be 0.3/50  $\mu$ s (300 ns virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 (see Reference [11]).

NOTE: Tolerance of, and recovery from, the application of the telephony voltages described in 12.10.2 is optional, but the safety requirements of that section are mandatory.

## 12.6 Medium Dependent Interface (MDI) Specification

**12.6.1 Line Interface Connector.** 8-pin connectors meeting the requirements of Section 3 and Figs 1 through 5 of ISO/DIS 8877 (see Reference [16]) shall be used as the compatibility interface between the PMA and the medium. The use of other types of connectors, if any, within a PMA or within the medium, although not explicitly prohibited, is outside the scope of this standard.

**12.6.2 Connector Contact Assignments.** The contacts of the connectors, as depicted in Figs 12-30 and 12-31, shall correspond to signaling circuits as indicated below:

Contact	Signal
1	Upward Data+ (positive for HI signal)
2	Upward Data- (negative for HI signal)
3	Downward Data+ (positive for HI signal)
4	not used by 1BASE5
5	not used by 1BASE5
6	Downward Data- (negative for HI signal)
7	reserved
8	reserved

For DTEs and the upper MDI of hubs, contacts 1 and 2 are used for transmitting and contacts 3 and 6 are used for receiving. For the port MDIs of hubs, however, contacts 1 and 2 are used for receiving and contacts 3 and 6 are used for transmitting.

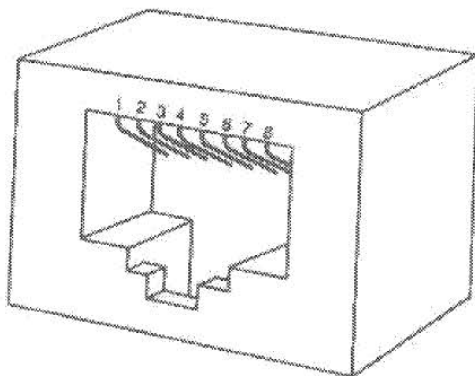


Fig 12-30  
DTE and Hub Connector

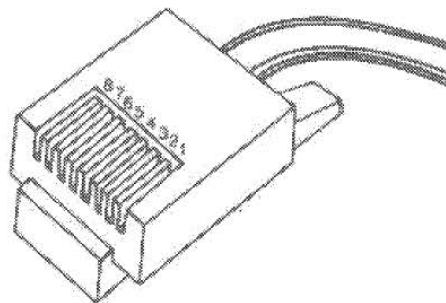


Fig 12-31  
Cable Connector

**12.6.3 Labeling.** To distinguish 1BASE5 connectors from those used for other purposes, it is recommended that appropriate labels be affixed to wall outlets and other connectors. This is particularly important in environments in which the specified 8-contact connectors are used for more than one purpose.

## 12.7 Cable Medium Characteristics

**12.7.1 Overview.** A significant number of BASE5 networks are expected to utilize in-place building wiring. In this environment, DTEs connect to wall outlets using twisted pair telephone cord. The wall outlets, in turn, connect to wiring closets, where hubs could be located, using standard telephone wiring. This wiring typically consists of 0.4–0.6 mm diameter (26–22 gauge) unshielded twisted pairs.

**12.7.2 Transmission Parameters.** Each wire pair used to interconnect DTEs and hubs shall meet the requirements of 12.9.3 and also have the following characteristics.

**12.7.2.1 Attenuation.** Total cable attenuation between a transmitter and the corresponding receiver shall be no more than 6.5 dB at all frequencies between BR/2 and BR, 9.2 dB at frequencies between BR and 2BR, and 13.8 dB at frequencies between 2BR and 4BR.

**12.7.2.2 Differential Characteristic Impedance.** The magnitude of the differential characteristic impedance at frequency BR,  $Z_{BR}$ , of each wire pair used shall be between 60  $\Omega$  and 115  $\Omega$ . In addition, the magnitude and phase angle of the characteristic impedance at each of the following frequencies shall be within the corresponding ranges indicated:

Frequency	Magnitude		Phase Angle	
	Minimum	Maximum	Minimum	Maximum
BR/4	$Z_{BR}$	$Z_{BR} + 7 \Omega$	$-10^\circ$	$0^\circ$
BR/2	$Z_{BR}$	$Z_{BR} + 5 \Omega$	$-8^\circ$	$0^\circ$
BR	$Z_{BR}$	$Z_{BR}$	$-6^\circ$	$0^\circ$
2BR	$Z_{BR} - 4 \Omega$	$Z_{BR}$	$-4^\circ$	$0^\circ$
4BR	$Z_{BR} - 5 \Omega$	$Z_{BR}$	$-3^\circ$	$0^\circ$

**12.7.2.3 Medium Timing Jitter.** Intersymbol interference and reflections due to impedance mismatches between the sections of a cable segment can introduce jitter in the timing of the zero-crossings. A cable segment terminated in 96  $\Omega$  shall add no more than  $\pm 17$  ns, referenced to the transmit clock, of edge jitter when driven with a rectangular signal of magnitude 2.5 V through a source impedance 22  $\Omega$ . The driving signal shall be a Manchester-encoded pseudo-random sequence of data with a repetition period of at least 511 bits.

NOTES: (1) The reflections caused by splicing two cable sections that have different characteristic impedances (but that each meet the requirements of 12.7.2.2) will not contribute significantly to timing jitter if the splice is within 10 m of either end of the segment.

(2) Branches off a wire pair (often referred to as "bridged taps" or "stubs") will generally cause excessive jitter and so should be avoided.

(3) Jitter can be measured at the receiving end of a segment using an oscilloscope. The oscilloscope is triggered on zero-crossings; the deviation of subsequent zero-crossings from multiples of BT2 is then observed. The deviation of each zero-crossing must not exceed  $\pm 34$  ns.

**12.7.2.4 Dispersion.** Each wire pair shall produce an output signal that meets the zero-crossing edge rate described in 12.5.3.2.1 when driven with a 1 MHz trapezoidal signal of magnitude 3.0 V (that is, 4.0 V peak-to-peak) with edge rate 20 mV/ns.

**12.7.3 Coupling Parameters.** To avoid excessive coupling of signals between pairs of a cable, the crosstalk and imbalance must be limited.

Crosstalk attenuation is specified with the far end of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 96  $\Omega$ .

**12.7.3.1 Pair-to-Pair Crosstalk.** The near-end, differential, crosstalk attenuation between each wire pair and each other pair in the same cable shall be at least 45 dB frequencies up to BR and at least  $45 - 15 \log_{10}(f/BR)$  dB for each frequency  $f$  between BR and 4BR.

**12.7.3.2 Multiple-Disturber Crosstalk.** The near-end, differential, crosstalk attenuation between multiple disturbing wire pairs and a disturbed pair in the same cable shall be at least 38.5 dB at frequency  $BR$  and at least  $38.5 - 15 \log_{10}(f/BR)$  dB for each frequency  $f$  between  $BR$  and  $4BR$ .

When two or more disturbers are present in a common cable sheath, the multiple-disturber, near-end, crosstalk attenuation (MDNEXT) into each pair, measured in dB, may be determined using the following equations:

$$H_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \cos \theta_{ij}$$

$$V_j = \sum_{i \neq j} 10^{(-X_{ij}/20)} \sin \theta_{ij}$$

$$\text{MDNEXT}_j = 10 \log_{10}(H_j^2 + V_j^2)$$

where:

$i$  iterates over each disturbing pair

$j$  is the disturbed pair

$X_{ij}$  is the magnitude of the near-end, differential, crosstalk attenuation from pair  $i$  to pair  $j$

$\theta_{ij}$  is the phase angle of the near-end, differential, crosstalk attenuation from pair  $i$  to pair  $j$

If only the probability distribution of  $X_{ij}$  is known, then the distribution of MDNEXT can be determined using Monte Carlo methods with that  $X_{ij}$  distribution and a phase angle uniformly distributed between 0 and  $2\pi$  rad.

NOTE: See Appendix A3 for example computations of MDNEXT distributions.

**12.7.3.3 Balance.** The longitudinal to metallic balance of the cable, defined as  $20 \log_{10}(E_{\text{long}}/2E_x)$ , where  $E_{\text{long}}$  is an externally applied voltage, as shown in Fig 12-32, shall exceed 44 dB at all frequencies up to  $4BR$ .

NOTE: The balance of the test equipment (such as the balance of the transformer and the matching of the 300  $\Omega$  resistors) must exceed that required of the cable.

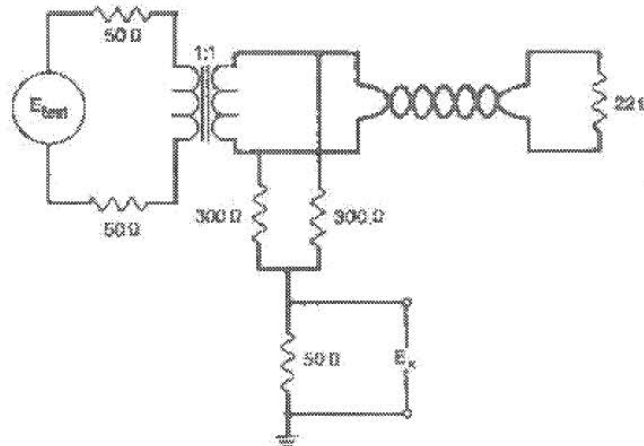


Fig 12-32  
Cable Balance Test

**12.7.4 Noise Environment.** Links used with 1BASE5 shall provide a noise environment no worse than that described below. The total noise environment generally results from two primary contributions: self-crosstalk from other 1BASE5 wire pairs and externally induced impulse noise, typically from telephone ringing and dialing signals, and office machinery. For the purposes of this standard, it can be assumed that the two components contribute independently and so the total error rate can be appropriately split between the two.

**12.7.4.1 Impulse Noise.** The noise voltage on wire pairs terminated at both ends in 96  $\Omega$ , as measured through the following specified filters, shall not exceed the corresponding threshold voltages more than 9 times per 1800 s interval. Following the start of any particular impulse that is counted, any additional impulses shall be ignored (that is, not counted) for a period of 100  $\mu$ s. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-Off Frequency	Threshold
2 MHz	170 mV
4 MHz	275 mV
10 MHz	560 mV

The impulse noise occurrence rate changes inversely by one decade for each 7 dB change in the threshold voltage. That is, if the noise occurrence rate is 9 counts per 1800 s at a particular threshold voltage, then a rate of 9 counts per 18 000 s will occur at a threshold 7 dB above that voltage. If a count rate of  $N$  counts per 1800 s is measured on a specific cable and filter at the specified voltage threshold, the media noise margin is  $7 \log_{10}(9/N)$  dB.

**12.7.4.2 Crosstalk.** The level of crosstalk noise on a pair depends on the level of the disturbing signal(s) and the crosstalk attenuation from the pair(s) carrying the signal(s). With the maximum transmit level specified in 12.5.3.1, the sinusoidal crosstalk attenuations specified in 12.7.3.1 and 12.7.3.2, and multiple, synchronized, random Manchester disturbers, the peak self-crosstalk (that is, crosstalk from other 1BASE5 signals) noise levels, as measured through the following specified filters, shall be less than or equal to the levels indicated below. Each filter is a 2-pole Butterworth low-pass filter with the indicated cut-off (3 dB point) frequency.

Cut-Off Frequency	Level
2 MHz	105 mV
4 MHz	160 mV

## 12.8 Special Link Specification

**12.8.1 Overview.** Some 1BASE5 networks may require extension beyond the limits imposed by 12.7 or, due to the installation environment, may require special media such as optical fiber, high-grade cable, or even free-space transmission. The detailed design of special links that replace standard links for use in such circumstances is beyond the scope of this standard, but the end-to-end characteristics are specified. It shall be the responsibility of the supplier to ensure the proper operation of special links with other 1BASE5 equipment.

**12.8.2 Transmission Characteristics.** Special links shall meet the overall attenuation, jitter, and dispersion specifications of 12.7.2.1, 12.7.2.3, and 12.7.2.4, respectively. Total noise introduced due to crosstalk or other sources shall not exceed that allowed for standard media, as specified in 12.7.4. To the extent that it affects operability with 1BASE5 transmitters and receivers, special links shall also meet the impedance and balance requirements of 12.7.2.2 and 12.7.3. The delay and preamble loss allowed for special links is specified in 12.9.4.

**12.8.3 Permitted Configurations.** No more than one special link is permitted in the path between any DTE and the header hub. That is, special links may be installed in parallel but not in series.

**NOTE:** Special links may be combined with other 1BASE5 components, such as hubs. Such combinations are subject to the performance specifications of this standard only as visible at their external interfaces. For example, explicit MDIs are not required internal to such combinations.

## 12.9 Timing

**12.9.1 Overview.** The successful interconnection of multivendor system components mandates that delay and bit loss be allocated fairly and realistically among the various system elements. The balance of this section defines the upper limits of delay and bit loss allocated to each component. These values allow proper operation with the worst-case system configuration of five levels of hubs, special links, maximum-length cable segments throughout the network, and colliding DTEs at extremes of the network.

**12.9.2 DTE Timing.** DTE Initial Transmit Delay is the time from the first full transition (due to the first OUTPUT\_UNIT of preamble) from the MAC to the first full transition (after startup bit loss, if any) at the MDI. This delay shall not exceed 8BT. The start bit loss shall not exceed 1 bit.

DTEs shall correctly receive frames that are preceded by 13 or more bits of preamble plus 8 bits of <sfid>.

There is a delay between the reception of signal at the PMA input of a DTE and operation of the deferral process in the MAC. Therefore, there is a window in which a DTE may fail to defer to a transmission even after it has arrived at the input. The DTE Deference Delay is the time from the receipt of the first transition of the preamble at the MDI until the last moment that the DTE might start transmitting at the MDI. This delay includes the following components:

- (1) The delay from the first input transition at the MDI to CARRIER\_ON at the PLS-MAC interface
- (2) The delay through the MAC processes from CARRIER\_ON to the last moment that a new transmission would miss being deferred
- (3) The delay from the first OUTPUT\_UNIT at the MAC-PLS interface to the first output transition at the MDI

The DTE Deference Delay shall be no more than 21BT.

The DTE Collision Shutdown Delay is the time from the first CVL or CVH arriving at the MDI of a transmitting DTE until that DTE transmits IDL at that interface. This time shall be no more than 26BT + jamSize=58BT. This limit shall not start until after the <sfid> has been transmitted.

**12.9.3 Medium Timing.** The Medium Transit Delay is the time from when a signal enters the medium until that signal leaves the medium. This delay shall not exceed 4BT.

**12.9.4 Special Link Timing.** The Special Link Transit Delay is the time from when a signal enters a special link until that signal leaves the special link. This delay shall not exceed 15BT. The preamble leaving a special link shall be no more than 2 bit cells longer than the preamble sent to that special link and no more than 1 bit cell shorter than the preamble sent to that special link. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

**12.9.5 Hub Timing.** Hub Startup Delay is the time from when the first bit cell of the preamble arrives at a hub until the first bit cell (also preamble) leaves that hub. This time shall be no greater than 12BT. The preamble sent by a hub shall be no more than 1 bit cell longer than the preamble sent to that hub or more than 4 bit cells shorter than the preamble sent to that hub. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

Hub Idle Collision Startup Delay applies to any case in which CP arrives preceded by fewer (or no) bit times of preamble than the Hub Startup Delay. The time from arrival of the first bit cell (either preamble or CP) until the first bit cell leaves the hub shall be no greater than 12BT.

Hub Transit Delay is the time from the arrival of any bit cell at a hub to the transmission of the corresponding bit cell from the hub. This delay shall not exceed 9BT, excluding the cumulative effects of clock tolerance.

The transit (propagation) delay between the upward and downward sides of the Header Hub shall be negligible.

Hub Delay Stretch/Shrink is the increase or decrease in a hub's transit delay due to the effects of differing clock rates. The clock rate tolerance of 0.01% specified in 12.3.2.4.1 and the maximum frame size of 1518 octets specified in 4.4.2.2 yield a maximum stretch or shrink of  $(56 + 8 + 1518 \cdot 8) \cdot 0.01\% \cdot 2 < 3BT$ , both at any given hub and through an entire network.

Hub Collision Detect Delay is the time required for a hub to detect multiple incoming signals and initiate transmission of CP. The time until transmission of the first CVH or CVL shall be no greater than 21BT.

Hub Active Collision Startup Delay is the time from the arrival of the first CVH or CVL of a CP pattern at a hub that is repeating bit cells until transmission of the first CVH or CVL from the hub. This delay shall be no greater than 12BT in either the upward or downward direction.

Hub Collision Shutdown Delay is the time from IDL arriving at a hub that is passing on or generating CP until that hub starts transmitting IDL. This delay shall be limited to 9BT. The limit is relaxed to 25BT, however, for the upward side of a hub that is generating CP. This extra allowance is made to avoid requiring implementation of a separate detection mechanism in each port of the hub.

**12.10 Safety.** Implementors are urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. EIA CB8-1981 (see Annex [12]) provides additional guidance concerning many relevant regulatory requirements.

Sound installation practice, as defined by applicable codes and regulations, shall be followed. ECMA-97 (see Annex [11]) describes safety requirements for local area networks.

**12.10.1 Isolation.** Each PMA/MDI interface lead shall be isolated from frame ground. This electrical separation shall withstand at least one of the following electrical strength tests:

- (1) 1500 V (rms) at 50 to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].
- (2) 2250 V (dc) for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 (see Reference [8]).
- (3) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50  $\mu$ s (1.2  $\mu$ s virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 (see Reference [11]).

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950 (see Reference [8]), during the test. The resistance after the test shall be at least 2 M $\Omega$ , measured at 500 V (dc).

**12.10.2 Telephony Voltages.** The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1BASE5 equipment. Other than voice signals (which are very low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard that constrains them, the following maximums generally apply:

- (1) Battery voltage to an on-hook telephone line is about -56 V (dc) applied to the line through a balanced 400  $\Omega$  source impedance. This voltage is used to power the telephone instrument and detect the off-hook condition. Source inductance can cause large spikes on disconnect.
- (2) Battery voltage to an off-hook telephone line is also about -56 V (dc) applied to the line through a balanced 400  $\Omega$  source impedance, but most of the voltage appears across the source impedance because the telephone instrument's impedance is relatively much lower.
- (3) Ringing voltage is a composite signal. The first portion can be up to 175 V peak at 20 to 66 Hz, limited by a 100  $\Omega$  source resistance or a 400 to 600  $\Omega$  source inductive impedance. The second portion is -56 V (dc) limited by a 300 to 600  $\Omega$  source impedance. Large spikes can occur at the start and end of each ring.

Although 1BASE5 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE: Wiring errors may impose telephony voltages differentially across the 1BASE5 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, however, receivers will generally appear to the telephone system as off-hook telephones. Full ring voltages, therefore, will be applied for only short periods of time. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to low resistance of the transformer coil.

### 13. System Considerations for Multisegment 10 Mb/s Baseband Networks

**13.1 Overview.** This section provides information on building multisegment 10 Mb/s baseband networks within a single collision domain. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two Data Terminal Equipments (DTEs) to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. This section applies only to networks that contain 10BASE-T segments.

NOTE: Information on 10BASE-T is included to begin the process of developing this section. It is intended that 3.6.1 and 10.7.1 be merged into this section in the future and that any new 10BASE segments be added to this section.

**13.2 Definitions.** Terminology used in Section 13 is defined here:

**collision domain.** A single CSMA/CD network. If two or more Media Access Control (MAC) sublayers are within the same collision domain and both transmit at the same time, a collision will occur. MAC sublayers separated by a repeater are within the same collision domain. MAC sublayers separated by a bridge are within different collision domains.

**link segment.** The point-to-point full duplex medium connection between two and only two Medium-Dependent Interfaces (MDIs).

**segment.** The medium connection, including connectors, between MDIs in a CSMA/CD LAN.

**13.3 Transmission System Model.** The physical size of a 10BASE-T network, or mixed-media network containing 10BASE-T link segments, is constrained by the limits of individual network components. These limits include the following:

- (1) Cable length and its associated propagation time delay.
- (2) Delay of repeater units (start-up and steady-state).
- (3) Delay of MAUs (start-up and steady-state).
- (4) Interpacket gap shrinkage.
- (5) Delays within the DTE associated with the CSMA/CD access method.

Table 13-1 summarizes the delays for the various network media segments:

**Table 13-1**  
**Delays for Network Media Segments**

Media Segment Type	Maximum Number of MAUs per Segment	Maximum Segment Length (m)	Minimum Medium Propagation Velocity*	Maximum Medium Delay per Segment (ns)
Coaxial	10BASE5	500	0.77 c	2165
	10BASE2	185	0.65 c	950
Link	FOIRL	1000	0.60 c	5000
	10BASE-T	100 <sup>†</sup>	0.59 c	1000
AUI <sup>‡</sup>	1 DTE/1 MAU	50	0.65 c	257

\*c =  $3 \times 10^8$  m/s

<sup>†</sup>Actual maximum segment length depends on cable characteristics; see 14.1.1.3.

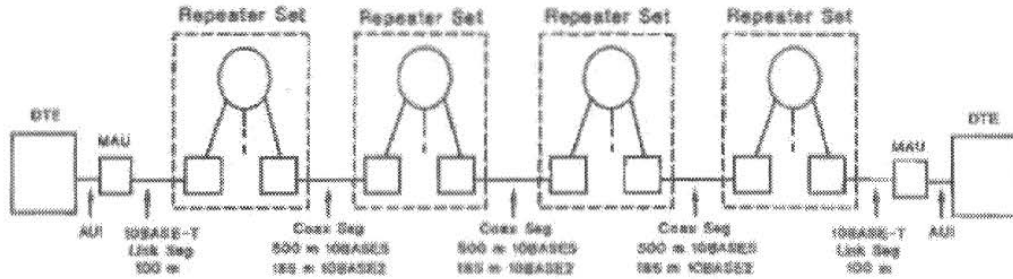
<sup>‡</sup>AUI is not a segment.

In addition, Table 14-1 summarizes the delays for the 10BASE-T MAU; Section 8, the delays for the 10BASE5 MAU; Section 10, the delays for the 10BASE2 MAU; and Section 9, the delays of the fiber optic inter-repeater link (FOIRL) and the repeater.

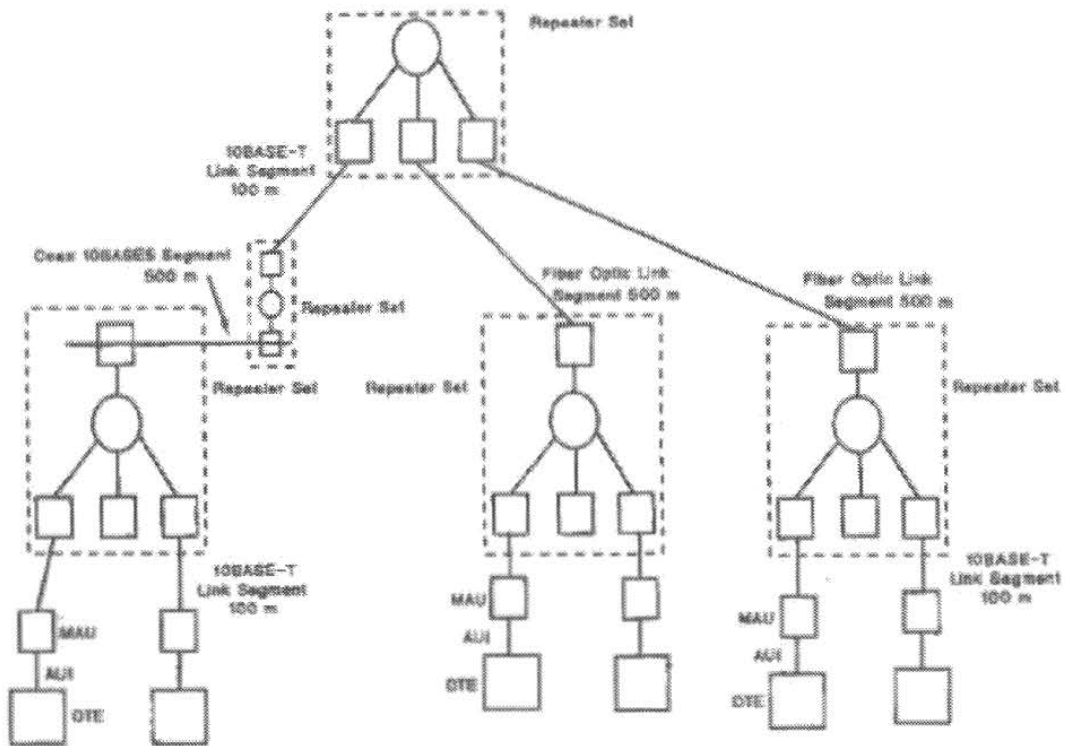
The following network topology constraints apply for 10BASE-T networks as well as mixed-media networks containing 10BASE-T link segments:

- (1) Repeater sets are required for all segment interconnection.
- (2) MAUs that are part of repeater sets count toward the maximum number of MAUs on a segment.
- (3) The transmission path permitted between any two DTEs may consist of up to five segments, four repeater sets (including optional AUIs), two MAUs, and two AUIs.
- (4) When a network path consists of four repeater sets and five segments, up to three of the segments may be coaxial and the remainder must be link segments (Figs 13-1 and 13-2). When five segments are present, each FOIRL link segment should not exceed 500 m.
- (5) When a network path consists of three repeater sets and four segments, the maximum allowable length of the FOIRL segments is 1000 m each, as specified in 9.9 (Fig 13-3).





**Fig 13-1**  
**Maximum Transmission Path with Three Coaxial Cable Segments**



**Fig 13-2**  
**Example of Maximum Transmission Path Using Coaxial Cable Segments, 10BASE-T Link Segments, and Fiber Optic Link Segments**

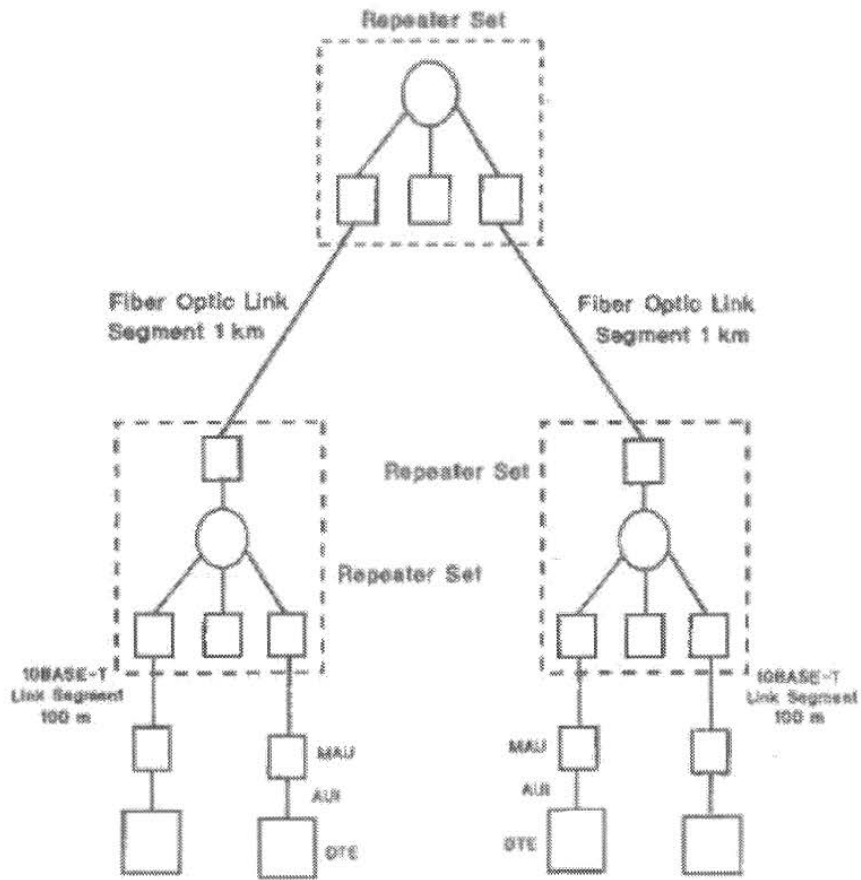


Fig 13-3  
Example of Maximum Transmission Path with Three Repeater Sets,  
Four Link Segments (Two are 100 m 10BASE-T and Two are 1 km Fiber)

## 14. Twisted-Pair Medium Attachment Unit (MAU) and Baseband Medium, Type 10BASE-T

### 14.1 Scope

**14.1.1 Overview.** Section 14 defines the functional, electrical, and mechanical characteristics of the Type 10BASE-T MAU and one specific medium for use with that MAU. The relationship of this specification to the entire ISO/IEC 8802-3 CSMA/CD Local Area Network Specification is shown in Fig 14.1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Sections 1 through 7 and Section 9 of this standard.

**14.1.1.1 Medium Attachment Unit (MAU).** The MAU has the following general characteristics:

- (1) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Section 14.
- (2) Supports message traffic at a data rate of 10 Mb/s.
- (3) Provides for operating over 0 m to at least 100 m (328 ft) of twisted pair without the use of a repeater.
- (4) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
- (5) Supports network configurations using the CSMA/CD access method defined in ISO/IEC 8802-3:1993 with baseband signaling.
- (6) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
- (7) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.

**14.1.1.2 Repeater Unit.** The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-T networks with more than two DTEs (see Figs 13-1 and 13-2). The repeater unit is defined in Section 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Section 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs, as defined in 9.4.1. Repeater sets with 10BASE-T MAUs are required to provide the auto-partition/reconnection algorithm on these ports, as specified in 9.6.6.2.

**14.1.1.3 Twisted-Pair Media.** The medium for 10BASE-T is twisted-pair wire. The performance specifications of the simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

**14.1.2 Definitions.** This section defines the terminology specific to Type 10BASE-T MAUs and their application to repeater units.

**bit time (BT).** The duration of one bit symbol (1/BR).

**collision.** A condition that results from concurrent transmissions from multiple signal sources.

**common-mode voltage.** The instantaneous algebraic average of two signals applied to a balanced circuit, both signals referred to a common reference. Also called longitudinal voltage.

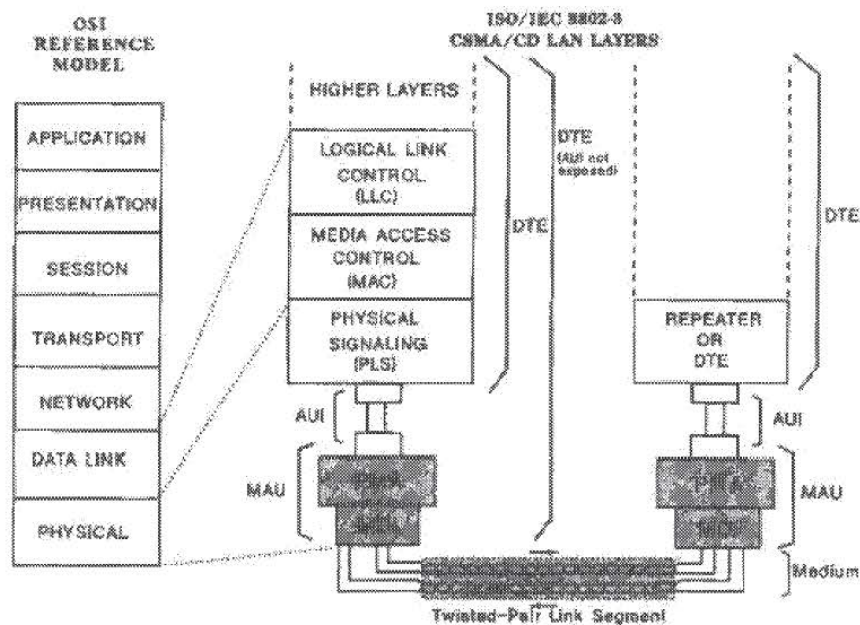


Fig 14-1  
10BASE-T Relationship to the ISO Open Systems Interconnection (OSI)  
Reference Model and the IEEE 802.3 CSMA/CD LAN Model

**cross connect.** A group of connection points often wall- or rack-mounted in a wiring closet, used to mechanically terminate and interconnect twisted-pair building wiring.

**differential-mode voltage.** The instantaneous algebraic difference between two signals applied to a balanced circuit, both signals referred to a common reference. Also called metallic voltage.

**Medium-Dependent Interface (MDI).** The mechanical and electrical interface between the twisted-pair link segment and the MAU.

**Physical Medium Attachment (PMA) sublayer.** The portion of the MAU that contains the functional circuitry.

**Physical Signaling (PLS) sublayer.** The portion of the Physical Layer, contained within the DTE, that provides the logical and functional coupling between the MAU and the Data Link Layer.

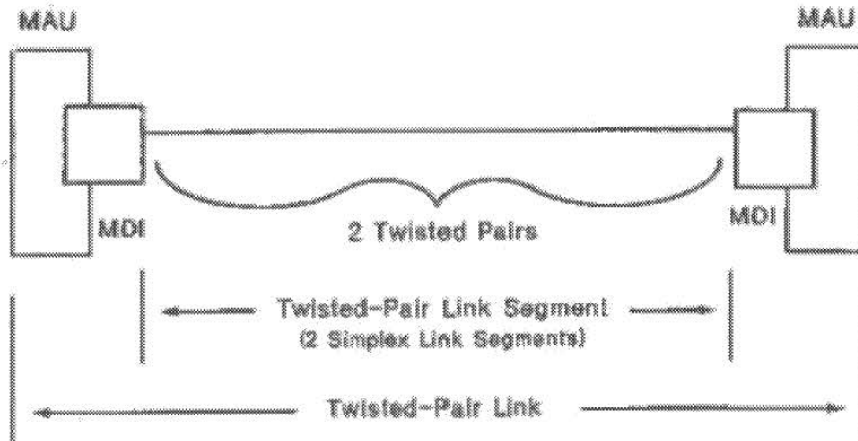
**simplex link segment.** A two-wire path between two MAUs including the terminating connectors, consisting of one or more twisted pairs joined serially with appropriate connection devices, for example, patch fields and wall plates (see Fig 14-2).

**twisted pair.** Two continuous insulated conductors helically twisted around one another (see Fig 14-2).

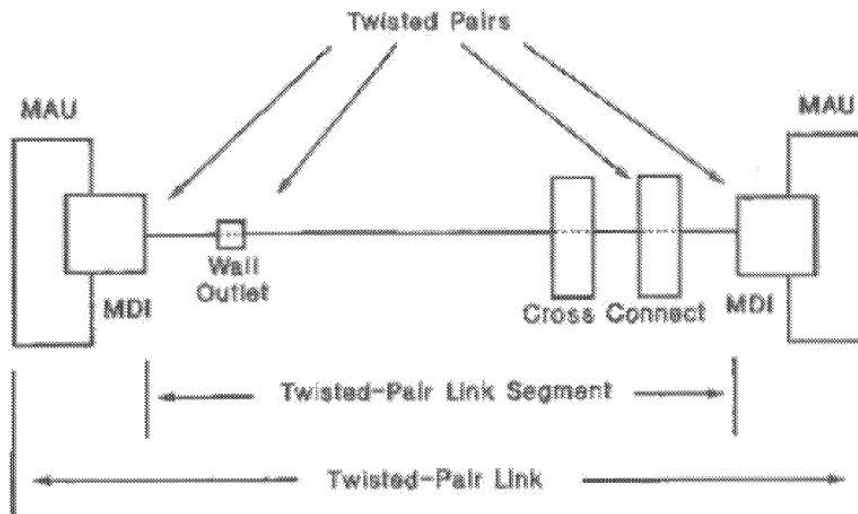
**twisted-pair cable.** A group of twisted pairs within a single protective sheath.

**twisted-pair cable binder group.** A group of twisted pairs within a cable that are bound together. Large telephone cables have multiple binder groups with high interbinder group near-end crosstalk loss.

**twisted-pair link.** A twisted-pair link segment and its two attached MAUs (see Fig 14-2).



(a)



(b)

Fig 14-2  
Twisted-Pair Link

twisted-pair link segment (duplex link segment). Two simplex link segments for connecting two MAUs (see Fig 14-2).

**14.1.3 Application Perspective.** This section states the broad objectives and assumptions underlying the specifications defined throughout Section 14.

#### 14.1.3.1 Objectives

- (1) Provide the physical means for communication between LAN Data Link Layer Entities.
- (2) Ensure compatibility of independently developed physical and electrical interfaces.
- (3) Provide a communication channel with a mean bit error rate, at the physical layer service interface of less than one part in  $10^6$ .
- (4) Provide for ease of installation and service.
- (5) Ensure that fairness of DTE access is not compromised.
- (6) Provide for low-cost networks, as related to both equipment and cabling.
- (7) Make use of telephone twisted-pair building wiring and telephony wiring practices.

**14.1.3.2 Compatibility Considerations.** All implementations of the twisted-pair link shall be compatible at the MDI. The MAU and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI (when implemented) specifications are met.

**14.1.3.3 Mode of Operation.** The 10BASE-T MAU is capable of operating in *normal* mode only (see 7.1.4). The MAU shall not operate in *monitor* mode.

When normal mode is in operation, the MAU functions as a direct connection between the medium and the DTE or repeater. Data from the DTE or repeater is output to one of the simplex link segments of the link segment, and data received on the other simplex link segment is input to the DTE or repeater.

**14.1.4 Relationship to PLS and AUI.** A close relationship exists between Section 14 and Section 7. Section 14 specifies the physical medium parameters and the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Section 7 by means of the AUI. 10BASE-T MAUs support a subset of the AUI services specified in Section 7. 10BASE-T MAUs do not support the optional isolate function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of both Section 14 and Section 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Section 14 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-T MAU does not require the implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present and MAU operation is defined in terms of them.

**14.2 MAU Functional Specifications.** The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the twisted-pair link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the twisted-pair link segment:

- (1) **Transmit function.** Provides the ability to transfer Manchester-encoded data from the DO circuit to the TD circuit. While not sending Manchester-encoded data on the TD circuit, the MAU sends an idle signal, TP\_IDL, on the TD circuit.
- (2) **Receive function.** Provides the ability to transfer Manchester-encoded data from the RD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, the MAU sends an idle signal, IDL, on the DI circuit.
- (3) **Loopback function.** Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the TD circuit.
- (4) **Collision Presence function.** Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the RD and DO circuits and to report such an occurrence as a collision.
- (5) **signal\_quality\_error Message (SQE) Test function.** Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal\_quality\_error* message can be sent by the MAU.
- (6) **Jabber function.** Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.

- (7) **Link Integrity Test function.** Provides the ability to protect the network from the consequences of failure of the simplex link attached to the RD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.

**14.2.1 MAU Functions.** The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions. The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function.

**14.2.1.1 Transmit Function Requirements.** The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD- lead.

At the start of a packet transmission, no more than 2 bits may be received from the DO circuit and not transmitted on the TD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with the differential voltage specified in 14.3.1.2.1 and with no more jitter than is specified in 14.3.1.2.3. The second bit transmitted on the TD circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6  $\mu$ s or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 BT.

Whenever data is not being transmitted on the TD circuit, an idle signal, TP\_IDL, shall be transmitted on the TD circuit. TP\_IDL is a start of idle, as defined in 14.3.1.2.1, followed by a repeating sequence of a 16 ms  $\pm$  8 ms period of silence (the time where the differential voltage remains at 0 mV  $\pm$  50 mV) and a link test pulse (see 14.3.1.2.1). Following a packet and start of idle, the repeating sequence shall start with a period of silence.

Transmission of TP\_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

**14.2.1.2 Receive Function Requirements.** The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD- lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

At the start of a packet reception from the RD circuit, no more than 5 bits may be received on the RD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1. The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6  $\mu$ s or less, the start-up delay of the first packet shall not exceed that of the second packet by more than 2 BT.

**14.2.1.3 Loopback Function Requirements.** When the MAU is transmitting on the TD circuit and is not receiving *RD\_input* messages (14.2.2.4) on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start of packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 14.3.1.3.1 (that is, 13.5 ns plus 1.5 ns). The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

**14.2.1.4 Collision Presence Function Requirements.** The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the RD circuit while in the Link Test Pass state. While a collision is detected, a CSO signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be

presented to the CI circuit no more than 9 BT after the occurrence of a collision. The signal shall be deasserted within 9 BT after the DO circuit or the RD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 BT.

When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

**14.2.1.5 *signal\_quality\_error* Message (SQE) Test Function Requirements.** The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time 'SQE\_test' beginning a time 'SQE\_test\_wait' after the last positive transition of a packet on the DO circuit. The value of 'SQE\_test' shall be  $10 \text{ BT} \pm 5 \text{ BT}$  and the value of 'SQE\_test\_wait' shall be between  $0. \mu\text{s}$  and  $1.6 \mu\text{s}$ . This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the TD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

**14.2.1.6 Jabber Function Requirements.** The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Fig 14-5). The MAU shall provide a window 'xmit\_max' during which time the Transmit function may continuously transmit *TD\_output* messages to the TD circuit. The value of 'xmit\_max' shall be between 20 ms and 150 ms. If a transmission exceeds this duration, the Jabber function shall inhibit the Loopback function and the transmission of *TD\_output* messages by the Transmit function, and shall send the CS0 signal on the CI circuit. This shall continue until *output\_idle* has been continuously present on the DO circuit for a time 'unjab'. The value of 'unjab' shall be  $0.5 \text{ ms} \pm 0.25 \text{ s}$ .

It is permissible to activate the Jabber function when the TD circuit transmitter is sending *TD\_output* messages for longer than 'xmit\_max'.

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.5.5.

**14.2.1.7 Link Integrity Test Function Requirements.** In order to protect the network from the consequences of a simplex link segment failure, the MAU shall monitor the RD circuit for *RD\_input* and link test pulse activity. If neither *RD\_input* nor a link test pulse is received for a time 'link\_loss', the MAU shall enter the Link Test Fail state and cause the *input\_idle* message to be sent on the DI circuit and the *TD\_idle* message to be sent on the TD circuit (Fig 14-6). The value of 'link\_loss' shall be between 50 ms and 150 ms. When *RD\_input* or a number 'lc\_max' of consecutive link test pulses is received on the RD circuit, the MAU shall exit the Link Test Fail state. The value of 'lc\_max' shall be between 2 and 10 inclusive.

Only link test pulses that occur within time 'link\_test\_max' of each other shall be considered consecutive. The value of 'link\_test\_max' shall be between 25 ms and 150 ms. In addition, detected pulses that occur within a time 'link\_test\_min' of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of 'link\_test\_min' shall be between 2 ms and 7 ms. Re-enabling shall be deferred until the signals on the RD and DO circuits become idle. The MAU shall not detect a link test pulse as *RD\_input*. Additionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the RD circuit becomes idle and the Jabber function has disabled transmission on the TD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At PowerOn, in place of entering the Link Test Pass state as shown in Fig 14-6, a MAU may optionally enter the Link Test Fail Reset state.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

**14.2.2 PMA Interface Messages.** The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater



unit to PMA communication. These and the messages between the PMAs over the MDI are summarized below.

**14.2.2.1 PLS to PMA Messages.** The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU:

Message	Circuit	Signal	Meaning
<i>output</i>	DO	CD1,CD0	Output information
<i>output_idle</i>	DO	IDL	No data to be output

**14.2.2.2 PMA to PLS Messages.** The following messages are sent by the MAU to the PLS in the DTE or repeater:

Message	Circuit	Signal	Meaning
<i>input</i>	DI	CD1,CD0	Input information
<i>input_idle</i>	DI	IDL	No information to input
<i>mau_available</i>	CI	IDL	MAU is available for output
<i>signal_quality_error</i>	CI	CS0	Error detected by MAU

Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required. Considerable jitter may be present (see 14.3.1.3.1).

#### 14.2.2.3 PMA to Twisted-Pair Link Segment Messages

Message	Circuit	Signal	Meaning
<i>TD_output</i>	TD	CD1,CD0	Output information
<i>TD_idle</i>	TD	TP_IDL	No information to output

The encoding for TP\_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI. Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required.

#### 14.2.2.4 Twisted-Pair Link Segment to PMA Messages

Message	Circuit	Signal	Meaning
<i>RD_input</i>	RD	CD1,CD0	Input information
<i>RD_idle</i>	RD	TP_IDL	No information to input

The encoding for TP\_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI.

**14.2.2.5 Interface Message Time References.** Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. The following describes the point where each message starts:

Message	Reference
<i>output</i>	leading bit cell boundary (BCB) of first valid CD1 or CD0
<i>output_idle</i>	last positive-going transition prior to start of IDL
<i>input</i>	leading BCB of first valid CD1 or CD0
<i>input_idle</i>	last positive-going transition prior to start of IDL
<i>signal_quality_error</i>	first transition of valid amplitude
<i>mau_available</i>	last positive-going transition prior to start of IDL
<i>TD_output</i>	leading BCB of first valid CD1 or CD0
<i>TD_idle</i>	last positive-going transition prior to start of TP_IDL
<i>RD_output</i>	leading BCB of first valid CD1 or CD0
<i>RD_idle</i>	last positive-going transition prior to start of TP_IDL

**14.2.3 MAU State Diagrams.** The state diagrams of Figs 14-3, 14-4, 14-5, and 14-6 depict the full set of allowed MAU state functions relative to the circuits of the AUI and NDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following sections.

**14.2.3.1 State Diagram Variables.** Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable *xmit* has the value 'disable' whenever the Jabber function or the Link Integrity Test function is in a state that asserts *xmit=disable*. The variable has the default value 'enable' all other times.

The variables used in the state diagrams are defined as follows:

**DI.** Controls the signal sent by the MAU on the DI circuit.

Values: *idle*; MAU is sending *input\_idle*, IDL (default).  
DO; MAU sends the signal received on the DO circuit.  
*lpbk = disable* overrides this and causes *input\_idle* to be sent.  
RD; MAU sends the signal received on the RD circuit.  
*rcv = disable* overrides this and causes *input\_idle* to be sent.

**CI.** Controls the signal sent by the MAU on the CI circuit.

Values: *idle*; MAU sends *max\_available*, IDL (default).  
SQE; MAU sends *signal\_quality\_error*, CS0.

**DO.** Status of the signal received by the MAU on the DO circuit.

Values: *idle*; MAU is receiving *output\_idle*, IDL.  
*active*; MAU is receiving *output*, CD0 or CD1.

**TD.** Controls the signal sent by the MAU on the TD circuit.

Values: *idle*; MAU sends *TD\_idle*, TP\_IDL (default).  
DO; MAU sends the signal received on the DO circuit.  
*xmit = disable* overrides this and causes *TD\_idle* to be sent.

**RD.** Status of the signal received by the MAU on the RD circuit.

Values: *idle*; MAU is receiving silence or a link test pulse.  
*active*; MAU is detecting signals which meet the requirements of 14.3.1.3.2.

**link\_test\_rcv.** Status of the link test signal received by the MAU on the RD circuit.

Values: *false*; MAU is not detecting a link test pulse.  
*true*; MAU is detecting a link test pulse.

**link\_count.** Count of the number of consecutive link test pulses received while in the Link Fail state.

Values: non-negative integers.

**lc\_max.** The number of consecutive link test pulses required before exit from the Link Fail state.

Values: positive integer between 2 and 10 inclusive.

**rcv.** Controls the path from the RD circuit to the DI circuit.

Values: *enable*; receive is enabled (default).  
*disable*; the output to the DI circuit is *input\_idle* when DI=RD.

**lpbk.** Controls the path from the DO circuit to the DI circuit.

Values: *enable*; loopback is enabled (default).  
*disable*; the output to the DI circuit is *input\_idle* when DI=DO.

**xmit.** Controls the path from the DO circuit to the TD circuit.

Values: *enable*; transmit is enabled (default).  
*disable*; transmit is disabled and the signal sent on the TD circuit is TP\_IDL.

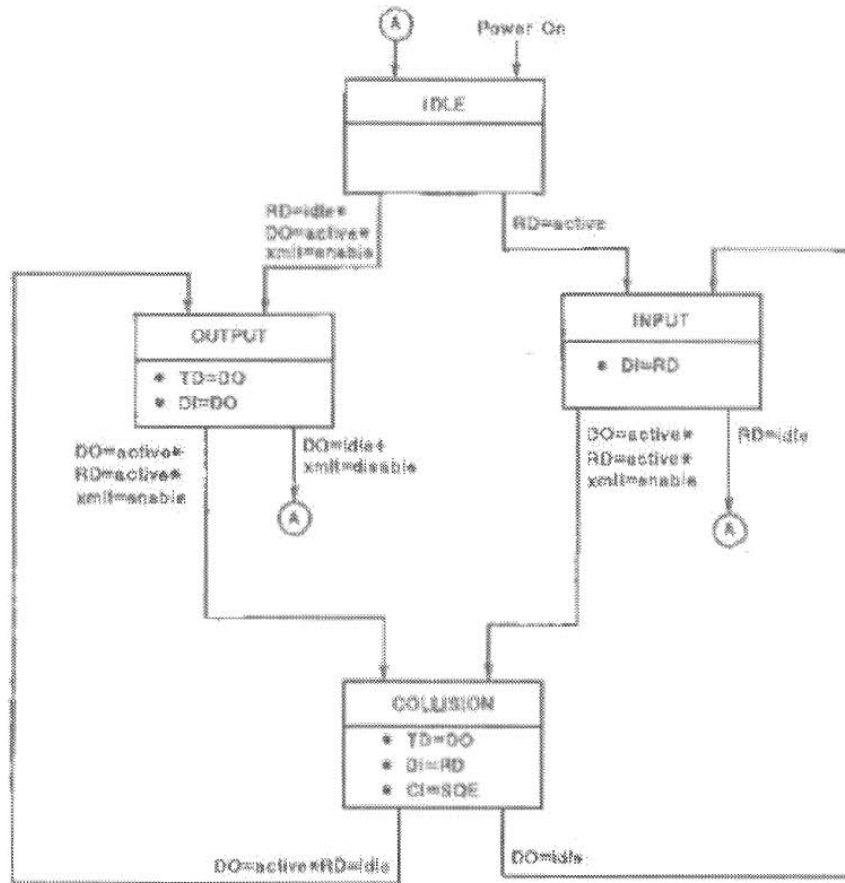


Fig 14-3  
MAU Transmit, Receive, Loopback, and Collision Presence Functions State Diagram

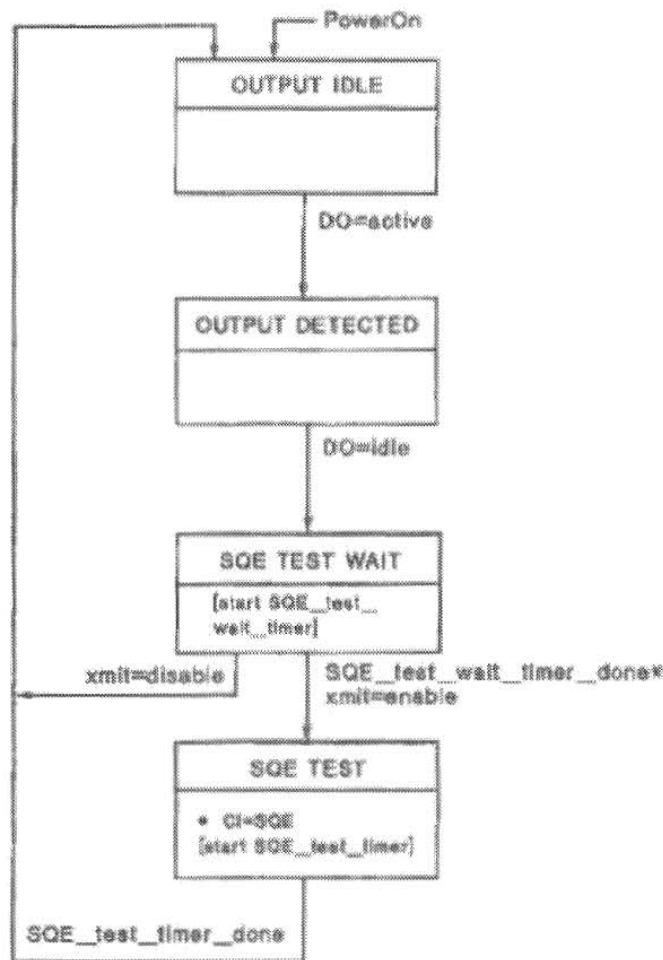


Fig 14-4  
*signal\_quality\_error* Message Test Function State Diagram

**14.2.3.2 State Diagram Timers.** All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where 'start x\_timer' is asserted. Time 'x' after the timer has been started, 'x\_timer\_done' is asserted and remains asserted until the timer is reset. At all other times, 'x\_timer\_not\_done' is asserted.

When entering a state where 'start x\_timer' is asserted, the timer is reset and restarted even if the entered state is the same as the exited state; for example, when in the Link Test Pass state of the Link Integrity Test function state diagram, the 'link\_loss\_timer' and the 'link\_test\_min\_timer' are reset each time the term 'RD = active + (link\_test\_rcv=true + link\_test\_min\_timer\_done)' is satisfied.

**link\_loss\_timer.** Timer for longest time input activity can be missing before the MAU determines that a link fail condition exists (14.2.1.7).

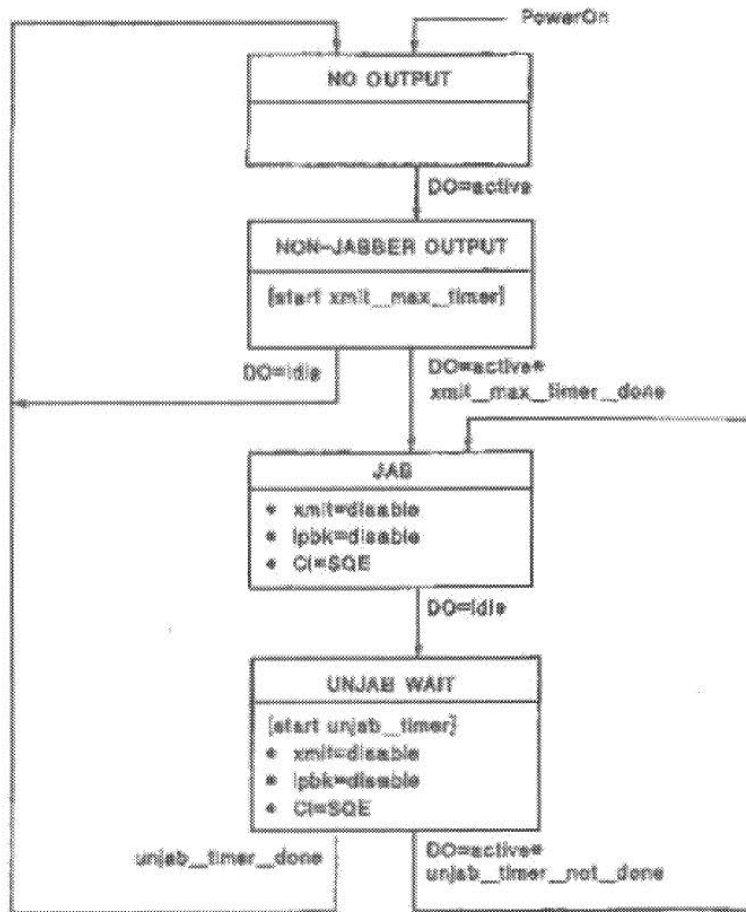


Fig 14-5  
Jabber Function State Diagram

**link\_test\_min\_timer.** Timer for the minimum time between valid link test pulses (14.2.1.7).

**link\_test\_max\_timer.** Timer for maximum time input activity can be missing before Link Fail state is exited (14.2.1.7).

**SQE\_test\_timer.** Timer for the duration of the CSQ signal used for the SQE Test function (14.2.1.5).

**SQE\_test\_wait\_timer.** Timer for the delay from end of packet to the start of the CSQ signal used for the SQE Test function (14.2.1.5).

**xmit\_max\_timer.** Timer for excessively long transmit time (14.2.1.6).

**unjab\_timer.** Timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (14.2.1.6).

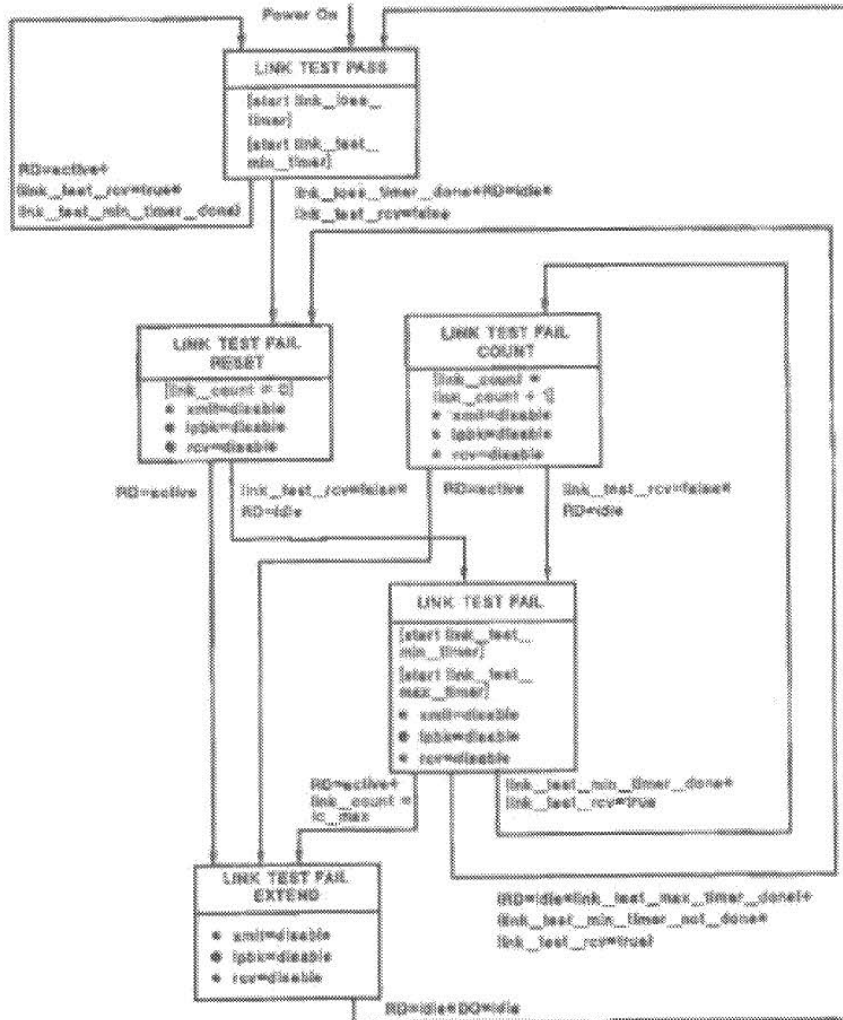


Fig 14-6  
Link Integrity Test Function State Diagram

**14.3 MAU Electrical Specifications.** This section defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Section 7 when the AUI is implemented.

Additional information relative to conformance testing is given in A4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

### 14.3.1 MAU-to-MDI Interface Characteristics

**14.3.1.1 Isolation Requirement.** The MAU shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI loads including those not used by 10BASE-T. This electrical separation shall withstand at least one of the following electrical strength tests.

- (1) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].
- (2) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].
- (3) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50  $\mu$ s (1.2  $\mu$ s virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 [11].

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950 [8], during the test. The resistance after the test shall be at least 2 M $\Omega$ , measured at 500 Vdc.

**14.3.1.2 Transmitter Specifications.** The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this section.

Where a load is not specified, the transmitter shall meet requirements of this section when connected to a 100  $\Omega$  resistive load. The use of 100  $\Omega$  terminations simplifies the measurement process when using 50  $\Omega$  measurement equipment as 50  $\Omega$  to 100  $\Omega$  impedance matching transformers are readily available.

Some tests in this section require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Fig 14-7 with component tolerances as follows: Resistors,  $\pm 1\%$ ; capacitors,  $\pm 5\%$ ; inductors,  $\pm 10\%$ . Component tolerance specifications shall be met from 5.0 MHz to 16 MHz. For all measurements, the TD circuit shall be connected through a balun to Section 1 and the signal measured across a load connected to Section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100  $\Omega$  resistive load and the TD circuit.

The insertion loss of the twisted-pair model when measured with a 100  $\Omega$  source and 100  $\Omega$  load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.

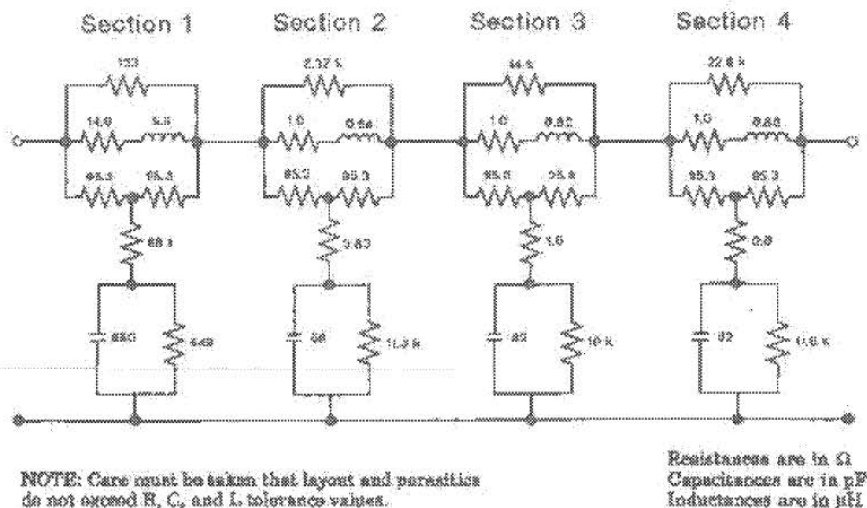


Fig 14-7  
Twisted-Pair Model

**14.3.1.2.1 Differential Output Voltage.** Some of the text and figures of this section describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

The peak differential voltage on the TD circuit when terminated with a 100  $\Omega$  resistive load shall be between 2.2 V and 2.8 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE: The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal  $V_o$ , is defined at the output of the twisted-pair model as shown in Fig 14-8. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Fig 14-9 for all data sequences. Voltage and time coordinates for inflection points on Fig 14-9 are given in Table 14-1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Fig 14-9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in A4.3.1. Time  $t = 0$  on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100  $\Omega$  and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

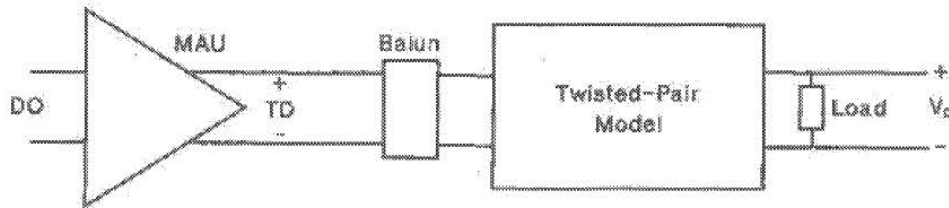


Fig 14-8  
Differential Output Voltage Test

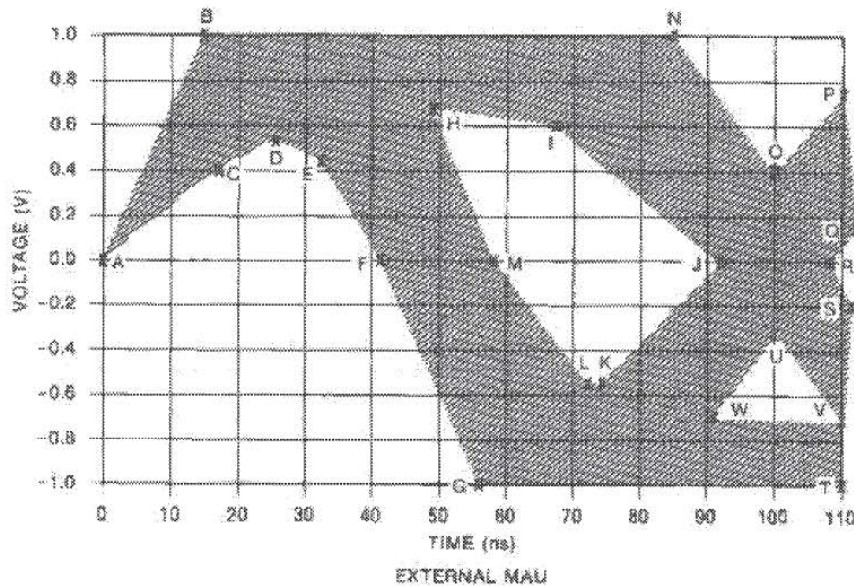


Fig 14-9  
Voltage Template



Table 14-1  
Voltage Template Values for Fig 14-9

Reference	Time (ns)		Voltage (V)
	External MAU	Internal MAU	
A	0	0	0
B	15	15	1.0
C	15	15	0.4
D	25	25	0.55
E	32	32	0.46
F	42	36	0
G	57	57	-1.0
H	48	48	0.7
I	67	67	0.6
J	82	88	0
K	74	74	-0.66
L	73	73	-0.66
M	98	91	0
N	86	95	1.0
O	100	100	0.4
P	110	110	0.75
Q	111	111	0.15
R	108	111	0
S	111	111	-0.15
T	110	110	-1.0
U	100	100	-0.3
V	116	110	-0.7
W	90	90	-0.7

This test shall be repeated with the template inverted about the time axis. In that case,  $t = 0$  on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See A4.3.3 for modification of the template to test jitter.)

The TP\_IDL shall always start with a positive waveform when a waveform conforming to Fig 7-12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Fig 14-10. Once the differential voltage has gone more negative than -50 mV, it shall not exceed +50 mV. The template requirements of Fig 14-10 shall be met when measured across each of the test loads defined in Fig 14-11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figs 14-7 and 14-8.

The link test pulse shall be a single positive (TD+ lead positive with respect to TD- lead) pulse, which falls within the shaded area of Fig 14-12. Once the differential output voltage has become more negative than -50 mV, it shall remain less than +50 mV. The template requirements of Fig 14-12 shall be met when measured across each of the test loads defined in Fig 14-11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figs 14-7 and 14-8.

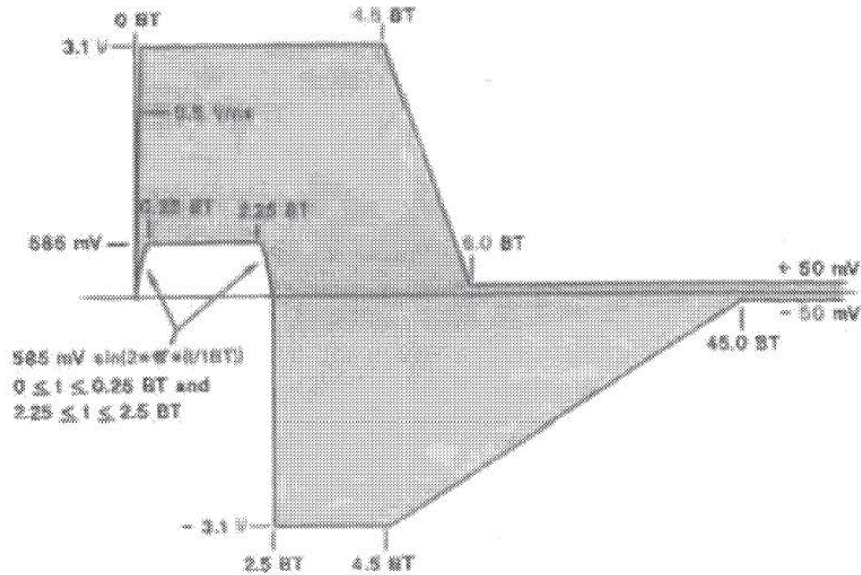
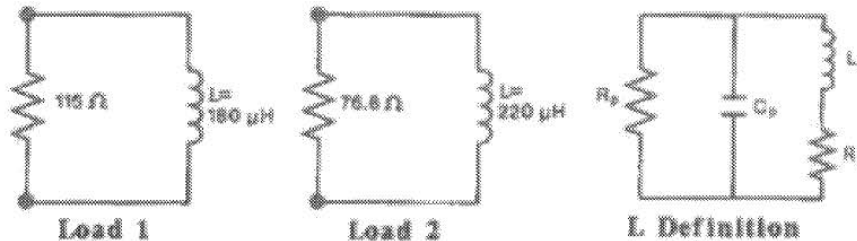


Fig 14-10  
Transmitter Waveform for Start of TP\_IDL



All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$$L_s = L \pm 1\% \quad R_p > 2 \text{ k}\Omega$$

$$C_p = 12 \text{ pF} \pm 20\% \quad R_s \leq 0.5 \Omega$$

Fig 14-11  
Start-of-TP\_IDL Test Load

**14.3.1.2.2 Transmitter Differential Output Impedance.** The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of 5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP\_IDL.

**14.3.1.2.3 Output Timing Jitter.** The transmitter output jitter is measured at the output of the twisted-pair model terminated in a 100 Ω load, as shown in Fig 14-8. The jitter added to the signal on the DO circuit as it propagates through the MAU and the twisted-pair model shall be no more than  $\pm 3.5$  ns.

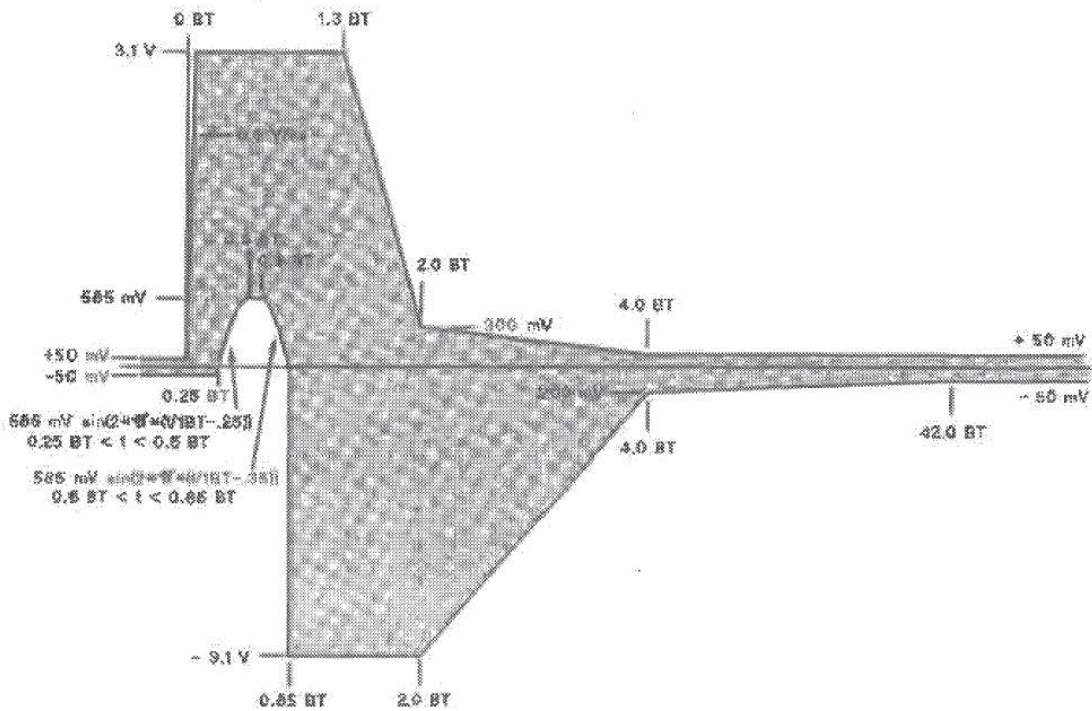


Fig 14-12  
Transmitter Waveform for Link Test Pulse

Additionally, the MAU shall add no more than  $\pm 8$  ns of jitter to the signal received on the DC circuit when the TD circuit is directly driving a 100  $\Omega$  resistive load.

**14.3.1.2.4 Transmitter Impedance Balance.** The common-mode to differential-mode impedance balance of the TD circuit shall exceed  $20 - 17 \log_{10}(f/10)$  dB (where  $f$  is the frequency in MHz) over the frequency range 1.0 MHz to 20 MHz. This balance is defined as  $20 \log_{10}(E_{cm}/E_{diff})$ , where  $E_{cm}$  is an externally applied sine wave voltage as shown in Fig 14-13.

NOTE: The balance of the test equipment (such as the matching of the 147  $\Omega$  resistors) must exceed that required of the transmitter.

**14.3.1.2.5 Common-Mode Output Voltage.** The magnitude of the total common-mode output voltage of the transmitter,  $E_{cm}$ , measured as shown in Fig 14-14, shall be less than 50 mV peak.

NOTE: This specification is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment.

**14.3.1.2.6 Transmitter Common-Mode Rejection.** The application of  $E_{cm}$ , as shown in Fig 14-13, shall not change the differential voltage at the TD circuit,  $E_{diff}$ , by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of  $E_{cm}$  shall be no more than 1.0 ns.  $E_{cm}$  shall be a 15 V peak 10.1 MHz sine wave.

**14.3.1.2.7 Transmitter Fault Tolerance.** Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at  $E_{cm}$  of either polarity (as indicated in Fig 14-15). The shape of the impulse shall be 0.9/50  $\mu$ s (300 ns virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 [11].

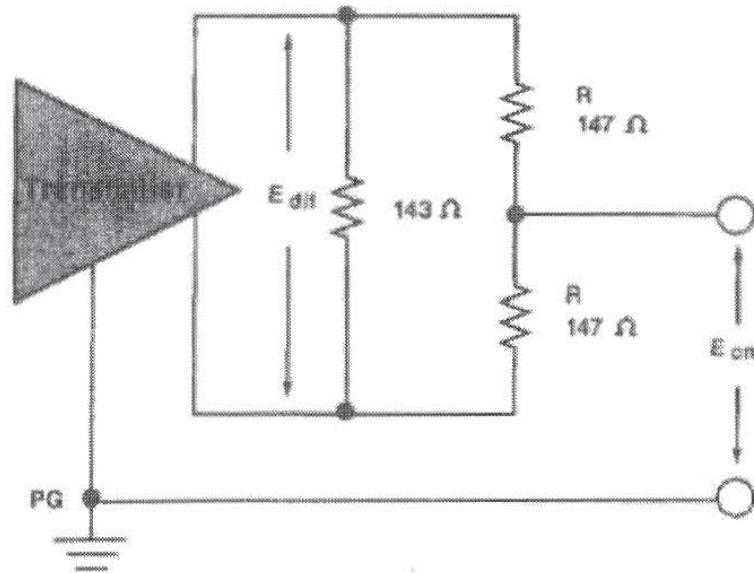


Fig 14-13  
Transmitter Impedance Balance and Common-Mode Rejection Test Circuit

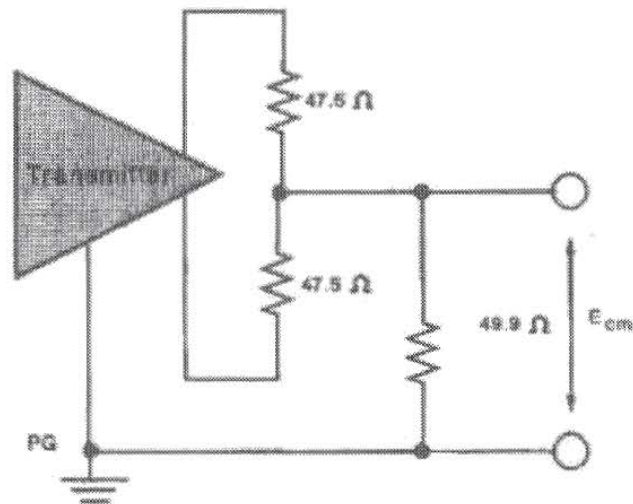


Fig 14-14  
Common-Mode Output Voltage Test Circuit

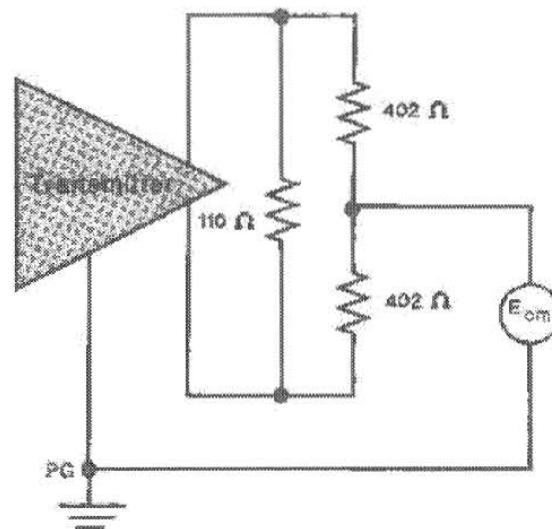


Fig 14-15  
Transmitter Fault Tolerance Test Circuit

**14.3.1.3 Receiver Specifications.** The MAU shall provide the Receive function specified in 14.2.1.2 in accordance with the electrical specifications of this section.

**14.3.1.3.1 Receiver Differential Input Signals.** Differential signals received on the RD circuit that are within the envelope of Fig 14-16 and 14-17, and have a maximum zero crossing jitter up to  $\pm 13.5$  ns from the ideal shall be sent to the DI circuit. The 13.5 ns includes jitter caused by an encoder, AUI cable and transmitting MAU, the twisted pair, and noise. Additionally, the MAU receiver shall add no more than  $\pm 1.5$  ns jitter to the receive signal before sending the signal to the DI circuit.

**14.3.1.3.2 Receiver Differential Noise Immunity.** The receiver, when presented with Manchester-encoded data meeting the requirements of 14.3.1.3.1, shall send this data to the DI circuit with a bit loss of no more than that specified in 14.2.1.2. In addition, the receiver, when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Fig 14-12, shall accept it as a link test pulse.

The receiver, while in the Idle state, shall reject as *RD\_input* the following signals:

- (1) All signals that when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cutoff at 15 MHz (refer to A4.2).
- (2) All continuous sinusoidal signals of amplitude less than 6.2 V peak-to-peak and frequency less than 2 MHz.
- (3) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-to-peak where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in (1) above.

**14.3.1.3.3 Idle Input Behavior.** The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver. The receiver shall take precautions to ensure that the high-to-silence transition of the start of idle is not falsely interpreted as a silence-to-non-idle transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, link segment, and receiver.

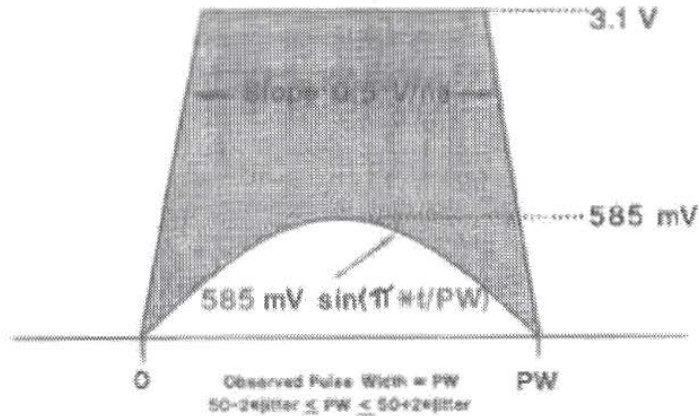


Fig 14-16  
 Receiver Differential Input Voltage—Narrow Pulse

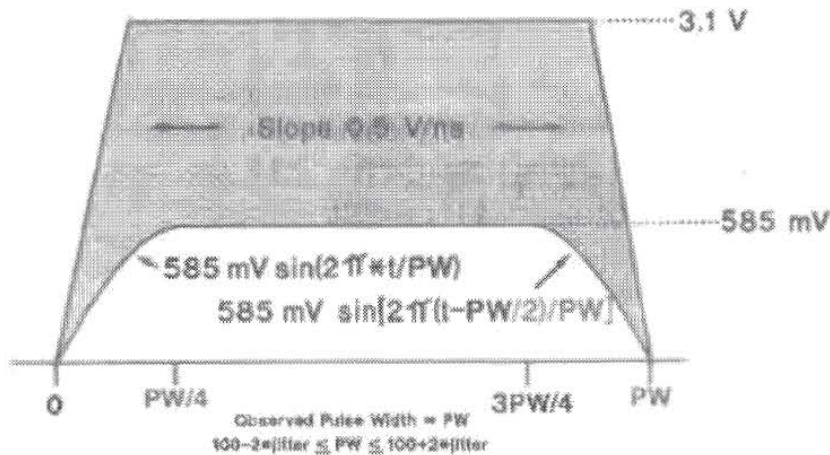


Fig 14-17  
 Receiver Differential Input Voltage—Wide Pulse

**14.3.1.3.4 Receiver Differential Input Impedance.** The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz. The return loss shall be maintained when the MAU is powered.

**14.3.1.3.5 Common-Mode Rejection.** Receivers shall assume the proper state on DI for any differential input signal  $E_d$  that results in a signal  $E_{diff}$  that meets 14.3.1.3.1 even in the presence of common-mode voltages  $E_{cm}$  (applied as shown in Fig 14-18).  $E_{cm}$  shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%). Additionally,  $E_{cm}$  shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more than 4.0 ns of edge jitter to  $E_d$  before sending the signal on the DI circuit.

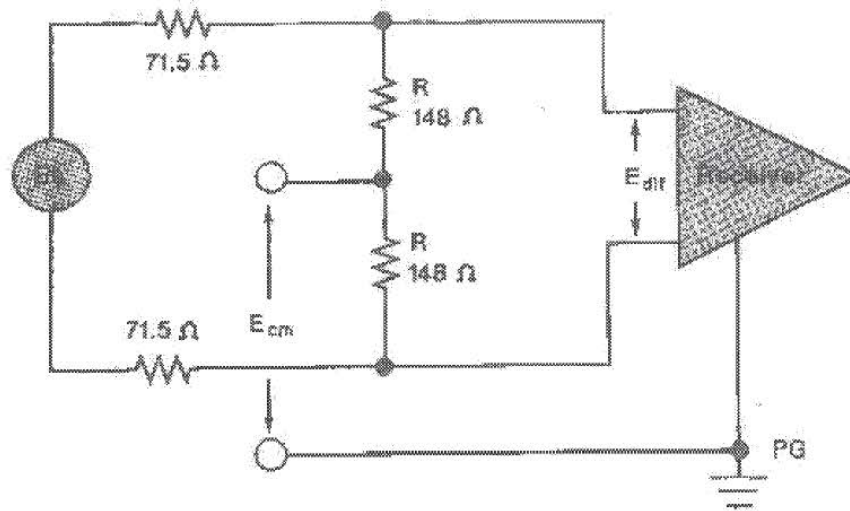


Fig 14-18  
Receiver Common-Mode Rejection Test Circuit

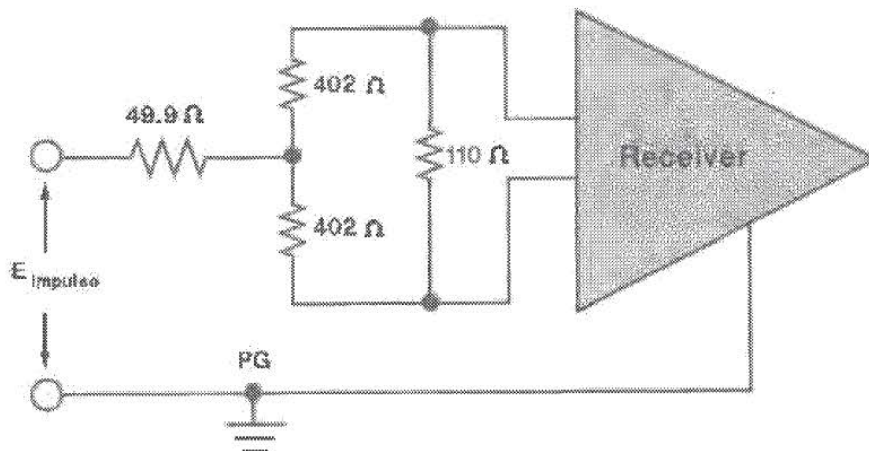


Fig 14-19  
Common-Mode Impulse Test Circuit

**14.3.1.3.6 Receiver Fault Tolerance.** The receiver shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ( $E_{impulse}$  as indicated in Fig 14-19). The shape of the impulse shall be 0.2/50  $\mu$ s (300 ns virtual front time, 50  $\mu$ s virtual time of half value), as defined in IEC Publication 60 [11].

**14.3.2 MAU-to-AUI Specification.** When a MAU contains a physical AUI connector, the following specifications shall be met.

**14.3.2.1 MAU-AUI Electrical Characteristics.** The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in

7.4 and 7.5. Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than  $\pm 160$  mV differential.

**14.3.2.2 MAU-AUI Mechanical Connection.** The MAU shall be provided with a 15-pin male connector as specified in 7.6.

**14.3.2.3 Power Consumption.** Following PowerOn, the surge current drawn by the MAU shall be such that  $I_p \times T_w$  is less than or equal to  $2 \times 10^{-3}$  ampere-seconds, where  $I_p$  is the peak surge current and  $T_w$  is the time during which the current exceeds the larger of 0.5 A or  $0.5 \times I_p$ . After the 100 ms following PowerOn, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

**14.4 Characteristics of the Simplex Link Segment.** Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100  $\Omega$ .

**14.4.1 Overview.** The medium for 10BASE-T is twisted-pair wiring. Since a significant number of 10BASE-T networks are expected to be installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

NOTE: EIA/TIA 568 (1991) [A19] provides specifications for media and installation practices suitable for use with this standard.

**14.4.2 Transmission Parameters.** Each simplex link segment shall have the following characteristics. All characteristics specified apply to the total simplex link segment unless otherwise noted. These characteristics are generally met by 100 m of unshielded twisted-pair cable composed of 0.5 mm [24 AWG] twisted pairs.

**14.4.2.1 Insertion Loss.** The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE: Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

**14.4.2.2 Differential Characteristic Impedance.** The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link segment shall be between 85  $\Omega$  and 111  $\Omega$  for all frequencies between 5.0 MHz and 10 MHz. Since characteristic impedance tends to decrease with increasing frequency, the above requirement is generally implied by the condition that the magnitude of the characteristic impedance over the frequency band 1 MHz to 16 MHz is  $100 \Omega \pm 15 \Omega$ . Also, the magnitude of the input impedance averaged over the 5.0 MHz to 10 MHz frequency band of a simplex link segment terminated in 100  $\Omega$  shall be between 85  $\Omega$  and 111  $\Omega$ .

**14.4.2.3 Medium Timing Jitter.** Intersymbol interference and reflections due to impedance mismatches between tandem twisted pairs of a twisted-pair link segment and effects of connection devices can introduce jitter to the CDI and CDO signals received on the RD circuit. No more than  $\pm 5.0$  ns of jitter shall be introduced to a test signal by a simplex link segment. The test signal shall have a peak amplitude of 3.0 V and 10% to 90% rise and fall times of 12 ns. The content of the test signal shall be a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

NOTE: Branches off a twisted pair (often referred to as "bridged taps" or "stubs") will generally cause excessive jitter and so should be avoided.



**14.4.2.4 Delay.** The maximum propagation delay of twisted pair shall be 5.7 ns/m (minimum velocity of  $0.585 \times c$ ). The maximum propagation delay of a link segment shall not exceed 1000 ns.

**14.4.3 Coupling Parameters.** To avoid excessive coupling of signals between twisted pairs of a twisted-pair cable, the crosstalk must be limited. Crosstalk loss is specified for the twisted pairs in a twisted-pair cable or twisted-pair cable binder group that are used as 10BASE-T twisted-pair links. Crosstalk loss is specified with the far ends of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 100  $\Omega$ . Drivers of disturbing pairs shall have a source impedance of 100  $\Omega$ .

**14.4.3.1 Differential Near-End Crosstalk (NEXT) Loss.** The NEXT loss between any two twisted pairs of a twisted-pair cable is dependent upon the geometry of the twisted-pair cable. Since the proximity of any two twisted pairs is influenced by the size of the twisted-pair cable, the NEXT loss is affected by twisted-pair cable size.

**14.4.3.1.1 Twenty-Five-Pair Cable and Twenty-Five-Pair Binder Groups.** The NEXT loss between any two twisted pairs in a twenty-five-pair twisted-pair cable or binder group used for 10BASE-T applications shall be at least  $30 - 15 \log_{10}(f/10)$  dB (where  $f$  is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

**14.4.3.1.2 Four-Pair Cable.** The NEXT loss between any two twisted pairs in a four-pair twisted-pair cable used for 10BASE-T applications shall be at least  $26 - 15 \log_{10}(f/10)$  dB (where  $f$  is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

**14.4.3.1.3 Other Cables.** The NEXT loss requirement for all other twisted-pair cables shall be the multiple-disturber NEXT loss of 14.4.3.2.

**14.4.3.2 Multiple-Disturber NEXT (MDNEXT) Loss.** When a twisted-pair cable or twisted-pair cable binder group contains twisted pairs from multiple 10BASE-T twisted-pair link segments, the multiple-disturber crosstalk loss is dependent upon the specific selection of disturbing and disturbed pairs. For each 10BASE-T receive pair, MDNEXT is measured by having the remaining near-end transmit pairs (excluding the transmit pair associated with the receive pair under test) driven with identical and synchronized sine wave signals. MDNEXT may then be determined from the signal level observed on the receive pair under test. By examining all pair combinations with a fixed number of disturbers, a cumulative distribution of MDNEXT is obtained at each frequency of interest. The one percentile of this cumulative distribution shall be at least  $23 - 15 \log_{10}(f/10)$  (where  $f$  is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. When the number of possible combinations allowed by a cable is fewer than 100, the MDNEXT loss for all combinations shall be at least  $23 - 15 \log_{10}(f/10)$  (where  $f$  is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. Refer to 12.7.3.2 and Appendix A3 for a tutorial and method for estimating the MDNEXT loss for a complete n-pair cable.

**14.4.4 Noise Environment.** The noise level on the link segments shall be such that the objective error rate is met. The noise environment consists generally of two primary contributors: crosstalk from other 10BASE-T circuits; and externally induced impulse noise, typically from telephone ringing and dialing signals, and other office and building equipment.

**14.4.4.1 Impulse Noise.** The average rate of occurrence of impulses greater than 264 mV shall be less than or equal to 0.2/s as measured at the output of the following specified filter. Following the start of any particular impulse that is counted, any additional impulse shall be ignored for a period of 1  $\mu$ s. The simplex link segment shall be terminated at the far end in 100  $\Omega$ . The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to A4.2).

NOTE: Typically, the impulse noise occurrence rate changes inversely by one decade for each 5 dB to 9 dB change in the threshold voltage. If a count rate of  $N$  counts/s is measured on a specific twisted pair and filter at the specified voltage threshold, the median noise margin is approximately  $7 \log_{10}(0.2/N)$  dB. Impulse noise may be a burst phenomenon and should be measured over an extended period of time.

**14.4.4.2 Crosstalk Noise.** The level of crosstalk noise on a simplex link segment depends on the level of the disturbing signal(s) and the crosstalk loss between the pair(s) carrying the signal(s) and the dis-

turbed pair. With the maximum transmit level (14.3.1.2), the sinusoidal crosstalk loss (14.4.3.2), and multiple, random Manchester-encoded disturbers, the peak self-crosstalk noise levels as measured at the output of the following specified filter shall be less than or equal to 264 mV. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to A4.2).

**14.5 MDI Specification.** This section defines the MDI for the twisted-pair link segment. The link topology requires a crossover function between PMAs. Implementation and location of this crossover is also defined in this section.

**14.5.1 MDI Connectors.** Eight-pin connectors meeting the requirements of Section 3 and Figures 1-5 ISO 8877 [20] shall be used as the mechanical interface to the twisted-pair link segment. The plug connector shall be used on the twisted-pair link segment and the jack on the MAU. These connectors are depicted (for informational use only) in Figs 14-20 and 14-21. The following table shows the assignment of signals connector contacts.

<u>CONTACT</u>	<u>MDI SIGNAL</u>
1	TD+
2	TD-
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD-
7	Not used by 10BASE-T
8	Not used by 10BASE-T

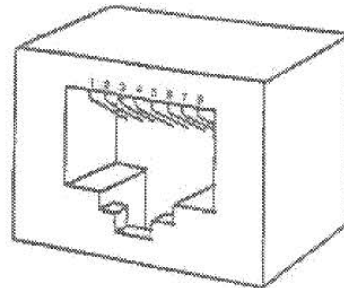


Fig 14-20  
MAU MDI Connect

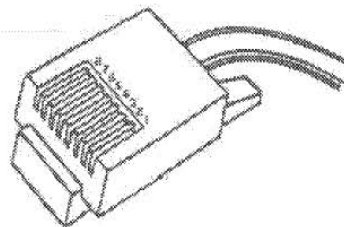


Fig 14-21  
Twisted-Pair Link Segment Connector

**14.5.2 Crossover Function.** A crossover function shall be implemented in every twisted-pair link. The crossover function connects the transmitter of one MAU to the receiver of the MAU at the other end of the twisted-pair link. Crossover functions may be implemented internally to a MAU or elsewhere in the twisted-pair link. For MAUs that do not implement the crossover function, the signal names of 14.5.1 refer to their own internal circuits. For MAUs that do implement the crossover function, the signal names refer to the remote MAU of the twisted-pair link. Additionally, the MDI connector for a MAU that implements the crossover function shall be marked with the graphical symbol "X". Internal and external crossover functions are shown in Fig 14-22.

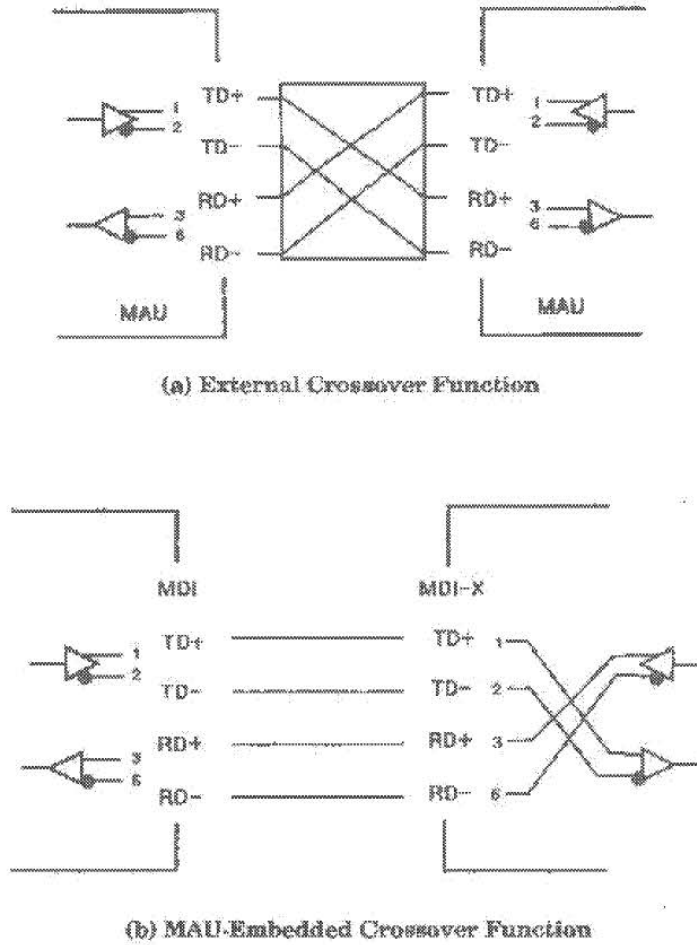


Fig 14-22  
Crossover Function

When a twisted-pair link connects a DTE to a repeater, it is recommended that the crossover be implemented in the MAU local to the repeater. If both MAUs of a twisted-pair link contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the MAUs. When both MAUs contain internal crossovers, it is further recommended in networks in which the topology identifier (either a central backbone segment or a central hub) that the MAU furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

**14.6 System Considerations.** The repeater unit specified in Section 9 forms the central unit for interconnecting 10BASE-T twisted-pair links in networks of more than two nodes. It also provides the means for connecting 10BASE-T twisted-pair links to other 10 Mb/s baseband segments. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Section 13.

#### 14.7 Environmental Specifications

**14.7.1 General Safety.** All equipment meeting this standard shall conform to one of the following IEC Publications: 380 [5], 435 [6], or 950 [8].

NOTE: For ISO/IEC 8802-3 : 1993, conformance shall be to IEC 950 [8].

**14.7.2 Network Safety.** This section sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this section are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

- (1) Direct contact between LAN components and power, lighting, or communications circuits.
- (2) Static charge buildup on LAN cables and components.
- (3) High-energy transients coupled onto the LAN cable system.
- (4) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 14.3.1.1.

**14.7.2.1 Installation.** Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

**14.7.2.2 Grounding.** Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

<p><b>WARNING:</b> It is assumed that the equipment to which the MAU is attached is properly earthed, and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.</p>
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**14.7.2.3 Installation and Maintenance Guidelines.** During installation and maintenance of the cable plant, care shall be taken to ensure that uninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

**14.7.2.4 Telephony Voltages.** The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400  $\Omega$  source impedance.

Ring voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100  $\Omega$  source resistance. The dc component is 56 Vdc with a 300  $\Omega$  to 600  $\Omega$  source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE: Wiring errors may impose telephony voltages differentially across 10BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

### 14.7.3 Environment

**14.7.3.1 Electromagnetic Emission.** The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

**14.7.3.2 Temperature and Humidity.** The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the MAU the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the twisted-pair link segment, the distance and operating environmental conditions over which the specifications of 14.4 will be met.

**14.8 MAU Labeling.** It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

- (1) Data rate capability in Mb/s,
- (2) Power level in terms of maximum current drain (for external MAUs),
- (3) Any applicable safety warnings.

See also 14.5.2.

**14.9 Timing Summary.** Table 14-2 summarizes the timing requirements for the 10BASE-T twisted-pair link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced sections.

**Table 14-2**  
**Maximum Timing Parameters**

Symbol	Function	Bit Loss <sup>1</sup>	Invalid Bits <sup>1</sup>	Steady-State Propagation Delay <sup>1</sup>	Start-up Delay <sup>1</sup>		Specified in
					Maximum	Variability <sup>2</sup>	
M1	<i>RD_input</i> to <i>input</i> on DI	5.0	1.0	2.0	8.0	2.0	14.2.1.2
M2	<i>output</i> on DO to <i>TD_output</i>	2.0	1.0	2.0	6.0	2.0	14.2.1.1
M3	<i>RD_input</i> * <i>output</i> to <i>signal_quality_error</i>	—	—	—	9.0	—	14.2.1.4
M4	<i>RD_idle</i> + <i>output_idle</i> (end of collision) to <i>max_available</i>	—	—	—	9.0	—	14.2.1.4
M5	<i>RD_input</i> * <i>output</i> to <i>input</i> on DI from circuit RD	—	—	—	9.0	—	14.2.1.4
M6	<i>RD_idle</i> * <i>output</i> to <i>input</i> on DI from circuit DO	—	—	—	9.0	—	14.2.1.4
M7	<i>output_idle</i> on DO to <i>signal_quality_error</i>	—	—	—	0 < x < 10	—	14.2.1.5
M8	<i>signal_quality_error</i> duration for SQE test	—	—	—	5 < x < 15	—	14.2.1.5
M9	<i>output</i> on DO to <i>input</i> on DI	5.0	1.0	1.0	7.0	—	14.2.1.3
T1	twisted-pair propagation	0	0	30.00	10.00	—	14.4.2.4
A1	ATN cable propagation (30 m)	0	0	3.57	3.57	—	7.4.3.7

<sup>1</sup>All Times in BT.

<sup>2</sup>For an explanation of the meaning of variability, see 14.2.11 and 14.2.12.

## Annex Additional Reference Material

(This Annex is not a part of this International Standard but is a part of ANSI/IEEE Std 802.3, 1993.)

- [A1] ANSI/EIA 364A-1987, Standard Test Procedures for Low-Frequency (Below 3 MHz) Electrical Connector Test Procedure.<sup>14</sup>
- [A2] ANSI/IEEE Std 770X3.97-1983, IEEE Standard Pascal Computer Programming Language.<sup>15</sup>
- [A3] Material from this reference is now incorporated into the base standard.
- [A4] Material from this reference is now incorporated into the base standard.
- [A5] ANSI/NFPA 70-1987, National Electrical Code.<sup>16</sup>
- [A6] ANSI/UL 94-1985, Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.<sup>17</sup>
- [A7] ANSI/UL 114-1982, Safety Standard for Office Appliances and Business Equipment.
- [A8] ANSI/UL 478-1979, Safety Standard for Electronic Data-Processing Units and Systems.
- [A9] ECMA-97 (1985), Local Area Networks Safety Requirements.<sup>18</sup>
- [A10] EIA CB8-1981, Components Bulletin (Cat 4) List of Approved Agencies, US and Other Countries, Impacting Electronic Components and Equipment.
- [A11] FCC Docket 20780-1980 (Part 15), Technical Standards for Computing Equipment, Amendment of Part 15 to redefine and clarify the rules governing restricted radiation devices and low-power communication devices, Reconsidered First Report and Order, April 1980.<sup>19</sup>
- [A12] MIL-C-17F-1983, General Specification for Cables, Radio Frequency, Flexible and Semirigid.<sup>20</sup>
- [A13] MIL-C-24308B-1983, General Specifications for Connector, Electric, Rectangular, Miniature Polarized Shell, Rack and Panel.
- [A14] UL Subject No 758: UL VW-1, Description of Appliance Wiring Material.<sup>21</sup>
- [A15] AMP, Inc., Departmental Publication 5525, Design Guide to Coaxial Taps. Harrisburg, PA 17105.
- [A16] AMP, Inc., Instruction Sheet 6814, Active Tap Installation. Harrisburg, PA 17105.

<sup>14</sup>All ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, New York, NY 10036, USA; EIA publications are available from the Standards Sales Department, Electronic Industries Association, 1001 Eye Street, NW, Washington, DC 20004, USA.

<sup>15</sup>IEEE publications are available from the Service Center, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08856-1331, USA.

<sup>16</sup>NFPA publications are available from Publications Sales, National Fire Protection Association, Batterymarch Park, Quincy, MA 02269-9101, USA.

<sup>17</sup>UL publications are available from Publications Sales, Underwriters Laboratories, Inc., 333 Pfingston Rd., Northbrook, IL 60062, USA.

<sup>18</sup>ECMA publications are available from European Computer Manufacturers Association, 115 Rue du Rhône, 1204 Geneva, Switzerland.

<sup>19</sup>FCC publications are available from the Federal Communications Commission, Washington, DC 20542, USA.

<sup>20</sup>MIL publications are available from US Navy Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120, USA.

<sup>21</sup>Information on this subject is available from Underwriters Laboratories, Inc., 1286 Walt Whitman Road, Melville, NY 11747, USA.

[A17] Brinch Hansen, P. *The Architecture of Concurrent Programs*. Englewood Cliffs, NJ: Prentice Hall, 1977.

[A18] Hammond, J.L., Brown, J.E., and Liu, S.S. *Development of a Transmission Error Model and Error Control Model*. Technical Report RADC-TR-76-138. Rome: Air Development Center (1975).

[A19] EIA/TIA 568 (1991), *Commercial Building Wiring Standard*.



## Appendixes

(These Appendixes are not a part of this International Standard or of ANSI/IEEE Std 802.3, 1993 Edition.)

### Appendix A System Guidelines

#### A1. Baseband System Guidelines and Concepts

**A1.1 Overall System Objectives.** The CSMA/CD Access Method, supported by baseband technology, depends on a variety of analog system components at and below the physical level of the OSI Reference Model. These components provide basic interconnection facilities for the CSMA/CD access mechanism itself and are defined throughout Sections 6, 7, and 8.

Overall performance of the analog baseband medium and related physical layer capabilities depends on an optimal and known set of analog capabilities within each of these critical system elements: the coaxial trunk cable, MAUs, branch cables, DTEs, and repeater units. These system elements affect the integrity with which the serial data bit stream analog signals are carried between open systems. There are at least three critical parameters of interest: bits lost in the transmission system, signal delays, and phase jitter. It is important that these be apportioned properly among the affected system elements.

The successful interconnection of multivendor system components mandates that the values for bits lost, signal delays, and phase jitter be allocated fairly and realistically among the various system elements. The balance of Appendix A identifies the upper limits of values to be placed on the subject parameters. These values are based on the maximal system configuration (for example, four repeater units, 2.5 km trunk coaxial cable medium).

**A1.2 Analog System Components and Parameter Values.** The values given in the following table are in terms of bits and are stated as maximum values except for values given within ranges.

The initial monogram under each component entry refers to the system component as identified in Fig A1. System parameters are stated in terms of the intralayer or interlayer messages sent within a station. Specific delays are called out as = delay.

The repeater concepts described throughout this section are considered to be an acceptable set of specifications for a multirepeated system. It is noted that the exact parametric values specified for the repeater environment are subject to minor refinement.

Component and Parameter	Start Up Delay	Lost In to Lost Out Delay	Start Up Loss
<b>MEDIUM</b>			
Trunk Coaxial Cable			
C1 Propagation	0.0	21.65	0.0
<b>POINT TO POINT LINK</b>			
P1 Propagation	0.0	25.54	0.0
A1 Propagation	0.0	2.57	0.0
<b>MEDIUM ACCESS UNIT</b>			
M1 DATA IN ASSERT → INPUT	6.0	0.5	5.0
M2 OUTPUT → DATA OUT ASSERT	3.0	0.5	2.0
M3 DATA IN COLLISION → SQE ASSERT	17.0	—	—
M4 COLLISION DEASSERT → SQE DEASSERT	20.0	—	—
M5 OUTPUT IDLE → SQE ASSERT	8 < x < 16	—	—
M6 SQE TEST ASSERT → SQE DEASSERT	5 < x < 15	—	—

Component and Parameter	Start Up Delay	Last In to Last Out Delay	Start Up Loss
<b>DTE</b>			
D1 INPUT → INPUT UNIT	18.0	---	18.0
D2 OUTPUT UNIT → OUTPUT	---	3.0	---
D3 INPUT → CARRIER STATUS = CARRIER ON	3.0	---	---
D4 INPUT IDLE → CARRIER STATUS = OFF	$3.0 < x \leq 6.0$	---	---
D5 SQE ASSERT → CARRIER STATUS = ON	3.0	---	---
D6 SQE DEASSERT → CARRIER STATUS = OFF	$3.0 < x \leq 6.0$	---	---
D7 SQE ASSERT → SIGNAL STATUS = ERROR	3.0	---	---
D8 SQE DEASSERT → SIGNAL STATUS = NO ERROR	$3.0 < x \leq 6.0$	---	---
D9 CARRIER STATUS = OFF → OUTPUT UNIT	$96 \leq x \leq 100$	---	---
D10 INPUT → OUTPUT	8.0	---	---
D11 SIGNAL STATUS = ERROR → JAM OUTPUT	16.0	---	---
D12 JAM OUTPUT DURATION	=32.0	---	---
<b>REPEATER UNIT</b>			
R1 INPUT 1,2 → OUTPUT 2,1	7.5	---	$23 < x < 34$
R2 INPUT IDLE 1,2 → OUTPUT IDLE 2,1	---	12.5	---
R3 INPUT 1,2 → CARRIER STATUS = ON	3.0	---	---
R4 SQE → SOURCED OUTPUT	6.5	---	---
R5 JAM OUTPUT → OUTPUT IDLE	=96.0	---	---

Figure A1 indicates the maximal system configuration and identifies the various system component parameters considered critical in determining analog system performance.

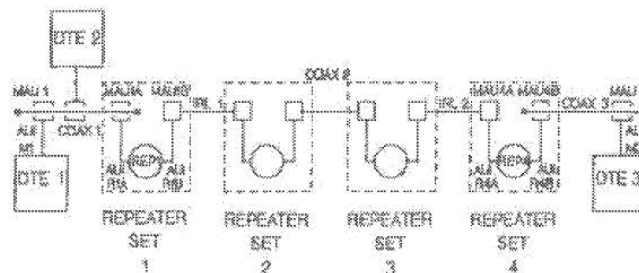


Fig A1  
Maximal System Configuration Bit Budget Apportionments

**A1.3 Minimum Frame Length Determination.** The following table indicates the system elements that make up the minimum frame length calculation based on the worst-case numbers as outlined in the bit budget of A1.2. The compilation in the following table is based on the following scenario:

- (1) DTE 1 transmits to an adjacent DTE 2 on coaxial segment 1.
- (2) DTE 3 transmission collides with DTE 1 transmission.
- (3) DTE 3 is assumed to be the worst-case distance from DTE 1 and its transmission just misses deferring to the DTE 1 message.
- (4) The collision fragment travels back down the network to inform DTE 1 that a collision has occurred on its message.

The frame length is constrained by two parameters:

- (a) The message from DTE 1 shall be long enough so that it is still sending when the collision is detected.
- (b) The message from DTE 1 shall be short enough such that DTE 2 can throw out the message on the basis of being too short.

Component and Function	Direction	Table Entry	Delay	Total Delay
<b>DTE 1 STARTS TO PUT OUT FIRST BIT</b>				
DTE 1	FWD	D2	3.0	3.0
AUI M1	FWD	A1	2.57	5.57
MAU1	FWD	M2	3.0	8.5
COAX1	FWD	C1	21.65	30.2
<b>REPEATER SET 1</b>				
MAU 1A	FWD	M1	3.0	36.2
AUI 1A	FWD	A1	2.57	38.8
REP 1	FWD	R1	7.5	46.3
AUI 1B	FWD	A1	2.57	48.9
MAU 1B	FWD	M2	3.0	51.9
<b>REPEATER SET TOTAL</b>			<b>21.64</b>	
IRL 1	FWD	P1	25.64	77.5
REPEATER SET 2	FWD		21.6	99.1
COAX 2	FWD	C1	21.65	120.8
REPEATER SET 3	FWD		21.6	142.4
IRL 2	FWD	P1	25.64	168.1
REPEATER SET 4	FWD		21.6	189.7
COAX 3	FWD	C1	21.65	211.4
MAU 3	FWD	M1	5.0	217.4
AUI 3	FWD	A1	2.57	219.9
DTE 3 PUTS OUT A BIT	REV	D10	3.0	227.9
AUI 3	REV	A1	2.57	230.5
MAU 3	REV	M2	3.0	233.5
COAX 3	REV	C1	21.65	255.1
<b>REPEATER SET 4</b>				
MAU 4B	REV	M3	17.0	272.1
AUI 4B	REV	A1	2.57	274.7
REP 4	REV	R4	6.0	281.2
AUI 4A	REV	A1	2.57	283.8
MAU 4A	REV	M2	3.0	286.8
<b>REPEATER SET TOTAL</b>			<b>31.64</b>	
IRL 2	REV	P1	25.64	312.4
REPEATER SET 3	REV		31.64	344.1
COAX 2	REV	C1	21.65	365.7
REPEATER 2	REV		31.64	397.4
IRL 1	REV	P1	25.64	423.0
REPEATER SET 1	REV		31.64	454.6
COAX 1	REV	C1	21.65	476.3
MAU 1	REV	M3	17.0	493.3
AUI M1	REV	A1	2.57	495.9
DTE 1	REV	D7	3.0	498.9

The above table provides the scenario that enables DTE 1 to determine a collision is taking place. DTE 1 shall transmit for at least 499 bit times. To determine how much longer DTE 2 will continue to receive bits, assume that DTE 1 is the last transmitter to provide bits to the DTE 2 MAU. DTE 2 then sees the following:

Component and Function	Direction	Table Entry	Delay	Total Delay
DTE 1	FWD	D11	18.0	514.9
DTE 1	FWD	D12	32.0	547.9
AUI M1	FWD	A1	2.57	649.4

If Repeater Set 1 is the last system component to provide bits to DTE 2, then DTE 2 will see the following:

Component and Function	Direction	Table Entry	Delay	Total Delay
<b>REPEATER SET 1 (1st JAM BIT)</b>				
REP 1	REV	R5	64.0	564.6
COAX 1	REV	C1	21.65	572.3

The Repeater Set is the last transmitter to provide a bit to DTE 2. The DTE 2 MAU starts seeing bits at time 8.6, which means that DTE 2 sees 563.7 bits (572.3 - 8.6). DTE 2 sees a minimum of 61 preamble bits and 8 SFD bits. The preamble and SFD bits can be deleted from the 563.7 total because they are not counted in minimum frame length.

The minimum frame length determination from the above scenario is then 564.7 - 69.0 = 494.7 bits. The 10 Mb/s system value for minimum frame length has been set at 512 bits.

**A1.4 System Jitter Budgets.** The typical jitter budget expected for the baseband system is apportioned in the following manner:

Encoder	0.5 ns
AUI Cable	1.0 ns (transmit end)
MAU Transmit	5.0 ns
Trunk Coax	7.0 ns
MAU Receive	-1.0 ns (with compensation)
AUI Cable	1.0 ns (receive end)
SNR on COAX	5.0 ns (SNR = 5:1)
SNR on AUI	0.5 ns (SNR = 5:1, transmit end)
SNR on AUI	0.5 ns (SNR = 5:1, receive end)
	<b>16.5 ns</b>

The 16 ns jitter budget leaves adequate design margin for implementation-dependent considerations.

**A1.4.1 Nominal Jitter Values.** The jitter budget values given above are not expected to accommodate all step changes in phase jitter due to system parameter variations within one or a few bit times.

**A1.4.2 Decoder Evaluation.** The phase decoder in the PLS sublayer should correctly decode a Manchester-encoded signal whose data transition point (center of a bit cell) has a peak-to-peak jitter of no more than 36 ns ( $\pm 18$  ns deviation from the bit cell center). See Figs A2 and A3 for test method.

Evaluation of decoder performance may be simulated and tested by application of three distinct waveforms representing worst-case and normal conditions. The waveforms contain Manchester-encoded bits whose center transitions represent the extremes of maximum skew. A 5 MHz (repetition rate) pulse train whose pulse width is either 64 ns or 136 ns simulates the two worst-case jitter conditions. The data output from the decoder should remain stable for each of the three test patterns and shifts between these extremes where there is a low rate of change in center transition skew. Note that the actual transmission system is not expected to permit sudden drastic changes in the steady-state edge deviation during the reception of any given frame. The above evaluation process is not intended to guarantee proper decoder performance under all operating conditions.

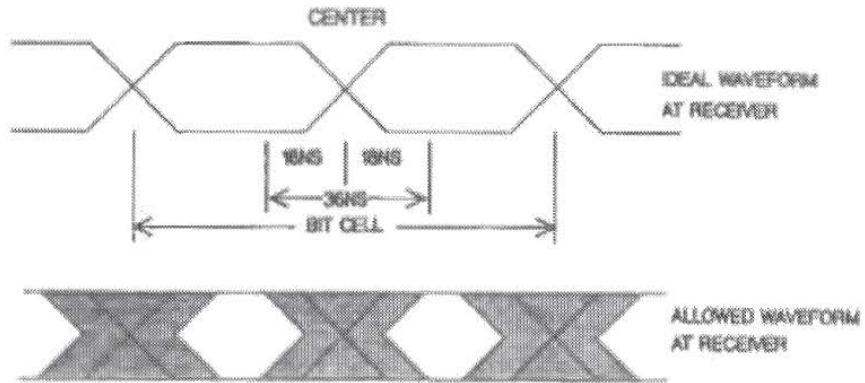


Fig A2  
Typical Signal Waveforms

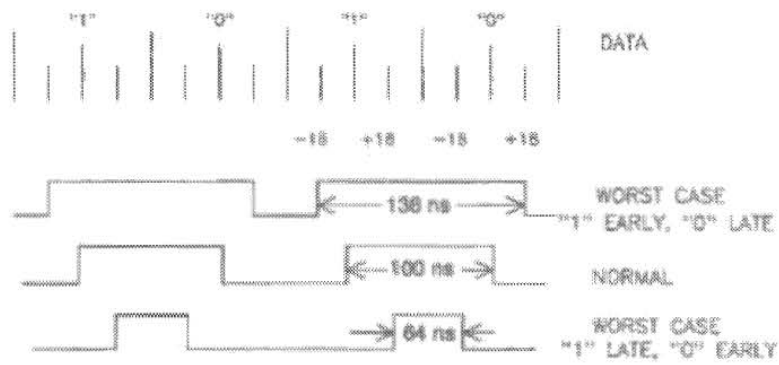


Fig A3  
Worst-Case Signal Waveform Variations

## A2. System Parameters and Budgets for 1BASE5

**A2.1 Delay Budget.** The successful interconnection of multivendor system components mandates that the values for bits lost and signal delays be allocated fairly and realistically among the various system elements. The following table summarizes and indicates the derivation of some of the delays specified in 12.9. The breakdowns shown for the parameters are illustrative only; implementors are free to make other allocations of delay *within* a device so long as the specifications of 12.9 are not violated.

Component	Delay (BT)
DTE Initial Transmit Delay (see 12.9.2)	3
DTE Deference Delay (see 12.9.2)	21
unsquelch	3
Carrier detect	5
MAC detects carrier and defers	10
DTE Initial Transmit Delay	3
DTE Collision Shutdown Delay (see 12.9.2)	58
detect CP and report SIGNAL_ERROR	10
detect SIGNAL_ERROR and start jamming	16
jamSize	32
Medium Transit Delay (see 12.9.3)	4
Special Link Transit Delay (see 12.9.4)	15
Hub Startup Delay (see 12.9.5)	12
unsquelch	4
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Idle Collision Startup Delay (see 12.9.5) (same as Hub Startup Delay)	12
Hub Transit Delay (see 12.9.5)	9
half fill FIFO	6
analogue of DTE Initial Transmit Delay	3
Hub Delay Stretch/Shrink (see 12.9.5) ( $(\text{preamble} + \langle \text{sfd} \rangle + \text{maxFrameSize}) \cdot 0.01\% \cdot 2$ )	3
Hub Collision Detect Delay (see 12.9.5)	21
unsquelch	3
detect collision	6
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3
Hub Active Collision Startup Delay (see 12.9.5)	12
Hub Transit Delay	9
First CVL or CVH may be preceded by CD0s and CD1s	3

Component	Delay (RT)
Hub Collision Shutdown Delay (downward) (see 12.9.5) (same as Hub Transit Delay)	9
Hub Collision Shutdown Delay (upward) (see 12.9.5)	25
detect loss of carrier	20
clear FIFO, if necessary	2
analogue of DTE Initial Transmit Delay	3

**A2.2 Minimum Frame Length Determination.** The minimum frame length for IBASES is determined using the values specified in 4.4.2.2 and 12.9, applied to the following (worst) case:

- (1) DTE 1, connected to Hub 1 at a network extremity, transmits a message upward toward Hub 5.
- (2) There is a special link in the path between Hub 1 and Hub 5.
- (3) DTE 2, also connected to Hub 1, transmits, just missing deferring to the downward signal from DTE 1 that was wrapped around at Hub 5.
- (4) DTE 3, also connected to Hub 1, receives the transmission from DTE 1.
- (5) Hub 1 generates CP, which travels up and then back down the network to inform DTE 1 and DTE 2 that a collision has occurred on their messages.
- (6) DTE 1 and DTE 2 continue to transmit until they have received CP, reacted to it, and completed their jams.
- (7) DTE 3 continues to receive until the end of CP.

The minimum frame length must allow both of the following conditions to be met:

- (1) DTE 1 is still sending when CP is received and recognized.
- (2) DTE 3 can discard the message fragment it receives because it is too short.

Event	Bits	Total
<b>DTE 1 → DTE 2</b>		
DTE Initial Transmit Delay	3	3
8 · Medium Transit Delay	32	35
2 · Special Link Transit Delay	30	65
10 · Hub Startup Delay	120	185
DTE Deference Delay	21	206
<b>DTE 2 → HUB 1 CP</b>		
Medium Transit Delay	4	210
Hub Collision Detect Delay	21	231
<b>HUB 1 CP → HUB 5 CP</b>		
3 · Medium Transit Delay	12	243
Special Link Transit Delay	15	258
4 · max(Hub Startup Delay, Hub Active Collision Startup Delay, Hub Idle Collision Startup Delay)	48	306
<b>HUB 5 CP → DTE 1 receives CP</b>		
5 · Hub Active Collision Startup Delay	60	366
4 · Medium Transit Delay	16	382
Special Link Transit Delay	15	397
<b>DTE 1 receives CP → DTE 1 stops transmitting</b>		
DTE Collision Shutdown Delay	58	455

COMPUTATION OF MINIMUM FRAME SIZE original preamble + <sfid>	-64	391 = data bits transmitted
5 · (Hub Collision Shutdown Delay (upward) -Hub Transit Delay)	80	471
5 · (Hub Collision Shutdown Delay (downward) -Hub Transit Delay)	0	471
Tiny fraction of Hub Delay Stretch/Shrink	0	471 = data bits received

The minimum frame length must exceed both the maximum number of bits sent before recognizing CP (391 - jamsiz = 359) and the maximum collision fragment size (471), as computed above. The 1BASE5 system value for minimum frame length has been set at 512 bits, which exceeds both of these values with a margin for error.

**A2.3 Jitter Budget.** The total edge jitter of the signals on each link must be limited to allow proper decoding at the receiver. The following budget has been used to allocate jitter to the indicated components that contribute to the total jitter on each link:

Component	Jitter
Transmitter skew	±10 ns
Cable intersymbol interference	9
Cable reflections	8
Reflections due to receiver termination mismatch	5
Total	±32 ns

The cable intersymbol interference and reflection allowances form the basis for the limit specified in 12.7.2.3; the reflection component is sufficient to allow a single 20 Ω impedance mismatch anywhere along a cable segment. The receiver-mismatch allowance is derived from the reflection attenuation specified in 12.5.3.2.4. The total forms the basis for the specification in 12.5.3.2.2.

The remainder of the jitter that can be tolerated by the Manchester decoder in a receiver is reserved to allow for distortion of the signal due to noise, receiver threshold offset, receiver skew, and receiver sampling timing error.

A simple clocked receiver/decoder with an 8 MHz sampling rate (the worst case allowed for in the design of this standard), can achieve proper decoding with up to ± 125 ns of jitter between two edges, which is equivalent to ±62.5 ns on each edge. Other receiver designs may tolerate more edge jitter. For example, a 6 MHz sampling rate would allow up to ±83.33 ns of jitter on each edge and a 16 MHz sampling rate allows up to ±31.25 ns of jitter.

It may be necessary to use a low-pass filter as part of the receiver to reduce the noise level seen by that receiver (see 12.7.4 for a description of the noise environment). A filter that reduces the noise may also have an effect on the amplitude and edge rate of the received signal. The filtered signal's edge rate near the zero-crossing is used in the critical translation from mV of noise and receiver offset into ns of jitter.

An example receiver design using an 8 MHz sampling rate and a 2 MHz Butterworth input filter might be based on the following jitter budget:

Component	Jitter
Input jitter (from above)	±32 ns
Noise and receiver threshold offset	19.5
Receiver skew (analog)	4
Receiver skew (digital)	7
Total	±62.5 ns



The two primary contributors to noise in a 1BASE5 cable are self-crosstalk and impulse noise (see 12.7.4). Because it is unlikely that both will be present at their 1% worst-case levels on any particular cable, the required bit error rate attributable to each source can be set at half of the one in  $10^4$  error rate required by 12.5.3.2.6.

Crosstalk noise is specified to be no more than 105 mV (peak) through a 2 MHz filter (see 12.7.4.2). Because crosstalk is present for the entire transmission of a packet, some crosstalk will coincide with the most sensitive part of the received signal. Therefore, the receiver must operate without error in the presence of this 105 mV of noise.

Impulse noise has a peak amplitude of 170 mV for  $\leq 0.005$  counts/s through the 2 MHz filter (see 12.7.4.1). This threshold does not directly correlate to jitter, however, because the derivation of the 62.5 ns jitter tolerance for an 8 MHz clock assumed worst-case sampling error. Assuming a random phasing of the sampling clock to the received signals, it can be shown that the 170 mV of noise is equivalent to a level of 85 mV with a worst-phase clock.

Jitter due to noise should be computed using the larger of the above two levels. The 105 mV for crosstalk noise, therefore, should be added to 50 mV for receiver threshold offset and the result should be divided by the edge rate of the filtered signal near the zero-crossing (7.9 mV/ns for the 2 MHz filter), yielding the 19.5 ns indicated above.

### A3. Example Crosstalk Computation for Multiple Disturbers

A method for computing multiple-disturber, near end, crosstalk attenuation (MDNEXT) into each 1BASE5 pair is specified in 12.7.3.2. This appendix provides example computations of MDNEXT using that method when only the distribution of  $X_j$  is known.

The single-disturber probability distribution curve (labelled "1") shown in Fig A4 is based on actual measurement of 25-pair, 24-gauge, unshielded, twisted pair cable. The remaining probability distribution curves (labelled with the number of disturbing pairs) were computed using Monte Carlo simulation. To compute each sample MDNEXT<sub>j</sub> for N disturbers, N values of crosstalk attenuation ( $X_i$ ) were chosen from the single-disturber distribution and N values of crosstalk phase ( $\theta_i$ ) were chosen from a uniform distribution between 0 and  $2\pi$  rad. These values were then used with the following equations to compute MDNEXT<sub>j</sub>:

$$H_j = \sum_{1 \leq i \leq N} 10^{(-X_i/20)} \cos \theta_i$$

$$V_j = \sum_{1 \leq i \leq N} 10^{(-X_i/20)} \sin \theta_i$$

$$\text{MDNEXT}_j = 10 \log_{10} (H_j^2 + V_j^2)$$

Iterating this process several hundred times, each time producing a single MDNEXT<sub>j</sub> sample, resulted in distributions for MDNEXT that are summarized in the following table and Fig A4:

Disturbers	Iterations	MDNEXT: Mean	Std. Dev.	99%
1		61.2 dB	7.0 dB	48.6 dB
2	500	57.2	6.2	46.4
3	500	55.1	5.8	45.2
6	500	52.0	5.7	42.5
13	1000	49.5	5.4	39.1
18	500	47.1	5.3	37.8
24	500	45.9	5.9	36.2

Because two pairs are used for each 1BASE5 connection, the entries in this table for 18 and 24 disturbers are not applicable for normal installation of 25-pair cables. Furthermore, telephone cables with larger

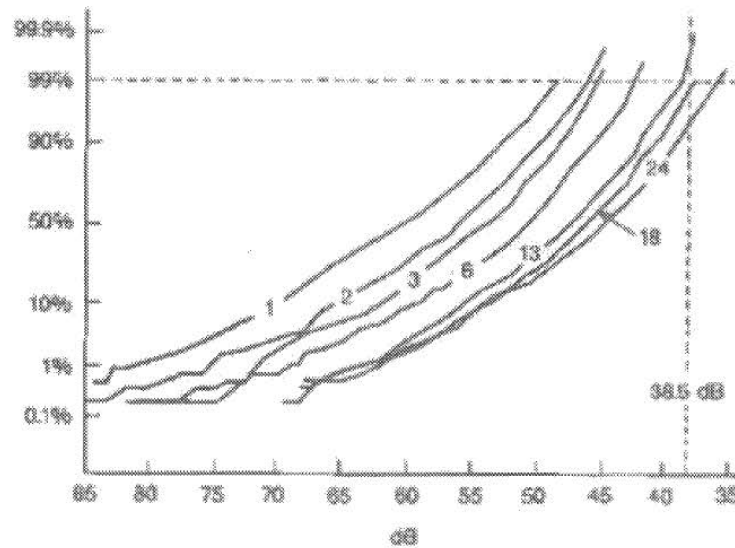


Fig A4  
MDNEXT Cumulative Probability Distribution

numbers of pairs are often constructed using sub-bundles of 25 pairs each and so might yield similar results (for example, the curves for 13 or fewer disturbers would be the most applicable ones).

The calculation method of this Appendix, though not the numeric values, applies to 10BASE-T.

#### A4. 10BASE-T

**A4.1 System Jitter Budget.** The jitter budget for 10BASE-T is apportioned as follows:

Jitter budget	Maximum-Length Twisted-Pair Link	Short-Length Twisted-Pair Link
	(jitter expressed in ns)	
Encoder	0.5	0.5
AUI cable (including SNR (D) pair)	1.5	1.5
MAU transmitter	2.0	2.0
Twisted-pair medium with equalization	1.5	0.0
Noise jitter on twisted-pair medium	8.0	2.5
MAU receiver	1.5	1.5
AUI cable (including SNR (D) pair)	1.5	1.5
Total	16.5	15.5

NOTE: Total transmit jitter for the combination of the MAU transmitter and link segment (A.4.1.2.3) is 33.5 ns and 28.0 ns for maximum- and short-length twisted-pair link segments, respectively. It is the sum of the entries for MAU transmitter and twisted-pair medium with equalization. The individual components cannot be easily observed on MAUs. Short-length segment is defined as a short, non-zero-length twisted-pair link. A short- rather than a zero-length segment is used in the calculation since a zero-length segment will have no significant noise and is a less severe case.

**A4.2 Filter Characteristics.** The implementation of the 3-pole, low-pass Butterworth filter should have the following characteristics:

3 dB cutoff frequency	15 MHz
Insertion loss (5 MHz to 10 MHz)	≤1.0 dB
30 MHz attenuation	≥17.5 dB
Input impedance (5 MHz to 10 MHz)	100 Ω
Return loss with 100 Ω load (5 MHz to 10 MHz)	≥20 dB

This filter is only used for the tests described in 14.3.1.3.2, 14.4.4.1, and 14.4.4.2. A buffer may be needed to achieve the above return loss when using an LC implementation of this filter.

**A4.3 Notes for Conformance Testing.** The following notes are provided to assist in developing the conformance test.

**A4.3.1 Notes for 14.3.1.2.1 on Differential Output Voltage.** For testing harmonics measured on the TD circuit when the DO circuit is driven by an all-ones Manchester-encoded signal, it is acceptable to use a pattern of maximum length packets whose data field is all ones.

For testing of the maximum and minimum output signal to the template in Fig 14-9, the recommended measurement procedure is described as follows. An oscilloscope set for a zero voltage trigger with a positive slope is allowed to accumulate an eye pattern that must be within the template. Acquisition must be long enough to ensure that all data variations have been observed. When using packetized data, the TP\_IDLE and the first transmitted bit should be excluded from this measurement. Also, the interpacket interval may be adjusted so that transition-to-idle transient effects are excluded. When testing with the inverted template, the slope of the scope trigger should be negative.

**A4.3.2 Note for 14.3.1.2.2 on Transmitter Differential Output Impedance.** The return loss (RL) is defined as follows:

$$RL = 20 \log_{10} \frac{|Z_{\text{transmitter}} + Z_{\text{cable}}|}{|Z_{\text{transmitter}} - Z_{\text{cable}}|}$$

and also

$$RL = 20 \log_{10} \frac{|V_i|}{|V_r|}$$

where

$Z_{\text{transmitter}}$  is the impedance of the transmitter

$Z_{\text{cable}}$  is the impedance of the cable

$V_i$  is the differential voltage incident upon the transmitter

$V_r$  is the differential voltage reflected from the transmitter

- (1) A transmitter with a purely resistive source impedance of  $96 \Omega \pm 20\%$  will satisfy this requirement.
- (2) The requirement of 14.3.1.2.2 is equivalent to the following two constraints:
  - (a) The return loss when measured with an  $85 \Omega$  resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
  - (b) The return loss when measured with a  $111 \Omega$  resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

**A4.3.3 Note for 14.3.1.2.3 on Output Timing Jitter.** Adherence to the template of 14.3.1.2.1 with a jitterless source driving DO and the zero crossings constrained to 46.5 ns to 53.5 ns and 96.5 ns to 103.5 ns is sufficient to demonstrate compliance with the 3.5 ns jitter requirement. When measuring an integrated MAU, the zero crossing time interval should be constrained to 44.5 ns to 55.5 ns and 94.5 ns to 105.5 ns due to the additional allocation for encoder and AUI jitter. This test is simpler to perform than the test which follows, but failure of this test does not demonstrate noncompliance.

When triggering on one edge of the transmitted signal and observing another edge, the observed jitter measures the difference between the jitter of the triggering edge and the observed edge. When the two

edges are separated such that the jitter of the edges is independent and clock drift is insignificant, the observed jitter is twice that of a single edge.

Therefore, a test that demonstrates compliance or noncompliance is as follows: Observe the zero crossings 8 BT and 8.5 BT from the triggering zero crossing while transmitting a pseudo-random data sequence of at least 511 bits. An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time intervals  $8.0 \text{ BT} \pm 7 \text{ ns}$  and  $8.5 \text{ BT} \pm 7 \text{ ns}$ . An integrated MAU is compliant when all zero crossings fall within the time intervals  $8.0 \text{ BT} \pm 11 \text{ ns}$  and  $8.5 \text{ BT} \pm 11 \text{ ns}$ .

When using packetized data, the TP\_IDL and the first transmitted bit should be excluded from these measurements.

**A4.3.4 General Note on Common-Mode Tests.** When performing tests specified as balanced or common-mode, the balance of the test equipment (such as matching resistors) must exceed that required by the test.

**A4.3.5 Note for 14.3.1.3.4 on Receiver Differential Input Impedance.** The return loss (RL) is defined as follows:

$$RL = 20 \log_{10} \frac{|Z_{\text{receiver}} + Z_{\text{cable}}|}{|Z_{\text{receiver}} - Z_{\text{cable}}|}$$

and also

$$RL = 20 \log_{10} \frac{|V_r|}{|V_i|}$$

where

$Z_{\text{receiver}}$  is the impedance of the receiver

$Z_{\text{cable}}$  is the impedance of the cable

$V_i$  is the differential voltage incident upon the receiver

$V_r$  is the differential voltage reflected from the receiver

- (1) A receiver with a resistive input impedance of  $96 \Omega \pm 20\%$  will satisfy this requirement.
- (2) The requirement of 14.3.1.3.4 is equivalent to the following two constraints:
  - (a) The return loss when measured with an  $85 \Omega$  resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
  - (b) The return loss when measured with a  $111 \Omega$  resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

**A4.3.6 Note for 14.3.1.3.3 on Receiver Idle Input Behavior.** For conformance testing of receivers, the start of idle shall conform to the template shown in Fig 14-10. Additionally, the magnitude of the voltage-time integral of the undershoot (measured from the negative zero crossing that ends the positive idle pulse to the time when the differential signal settles to  $0.0 \text{ mV} \pm 50 \text{ mV}$ ) shall be no greater than 1.2 times the voltage-time integral of the positive idle pulse (measured from the last positive zero crossing to the negative zero crossing).

**A4.3.7 Note for 14.3.1.3.5 on Receiver Common-Mode Rejection.** For a stand-alone MAU, the receiver common-mode test may be performed with a jitterless  $E_s$ , so that the DI circuit should have no more than 4.0 ns of edge jitter.

For an integrated MAU, the common-mode test is performed with an  $E_s$  that has zero crossing jitter up to 11 ns from the ideal.

## Appendix B State Diagram, MAC Sublayer

### B1. Introduction

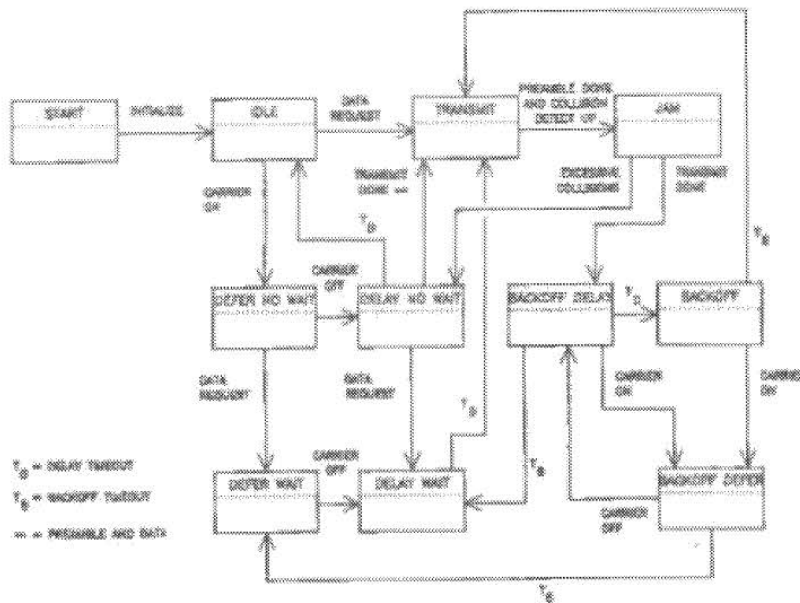
This Appendix contains a generalized state machine description of the CSMA/CD procedures for MAC. It is supportive of the formal procedures defined in 4.2. It is assumed that the reader is familiar with those formal descriptions.

The state diagrams of this Appendix are descriptive rather than definitional; the formal statements of 4.2 provide the definitive specifications.

### B2. CSMA/CD Media Access Control State Machine Overview

The CSMA/CD MAC consists of two components: the transmit component and the receive component. These components operate concurrently and independently.

**B2.1 Transmit Component Overview.** The transmit component is responsible for handling all events that affect the transmission of a frame onto the medium (see Fig B1 and Table B1).



**Fig B1**  
Transmit Component State Diagram

#### B2.2 Transmit Component Event Descriptions

**Initialize.** This event is generated by management to start up the component.

**Data Request.** This event is generated by the LLC sublayer. It indicates there is a PDU to be transmitted.

**Table B1**  
**Transmit Component State Transition**

Current State	Event	Action	Next State
0. Start	Initialise	- Perform Initialization	Idle
1. Idle	Data Request	- Construct Frame - Start Frame Transmission - No Action	Transmit
	Carrier On		Defer No Wait
2. Transmit	Preamble Done AND Collision Detect Up Transmit Done	- Start Jam Transmission - Increment Attempt Count - Start Delay Timer - Reset Attempt Count - Indicate successful Transmission	Jam Delay No Wait
3. Jam	Transmit Done	- Start Delay Timer - Start Backoff Timer	Backoff Delay
	Excessive Collisions	- Start Delay Timer - Indicate Transmit Excessive Collisions	Delay No Wait
4. Backoff	Carrier On Backoff Timeout	- No Action - Start Frame Transmission	Backoff Defer Transmit
5. Backoff Defer	Carrier Off Backoff Timeout	- Start Delay Timer - No Action	Backoff Delay Defer Wait
6. Backoff Delay	Carrier On Delay Timeout Backoff Timeout	- Stop Delay Timer - No Action - No Action	Backoff Defer Backoff Delay Wait
7. Defer No Wait	Data Request Carrier Off	- Construct Frame - Start Delay Timer	Defer Wait Delay No Wait
8. Delay No Wait	Data Request Delay Timeout	- Construct Frame - No Action	Delay Wait Idle
9. Defer Wait	Carrier Off	- Start Delay Timer	Delay Wait
10. Delay Wait	Delay Timeout	- Start Frame Transmission	Transmit

**Carrier On.** This event indicates that the physical layer has detected a change in carrier sense from no carrier to carrier.

**Carrier Off.** This event indicates that the physical layer has detected a change in the state of carrier sense from carrier to no carrier.

**Preamble Done AND Collision Detect Up.** This event indicates that the physical layer has detected a collision with the frame being transmitted and the transmission of the preamble sequence is completed.

**Delay Timeout.** This event indicates that the interframe time delay has completed.

**Backoff Timeout.** This event indicates that the time period for backing off has completed.

**Transmit Done.** The bit transmitter has transmitted all of the bits in the transmit buffer specified by the transmit buffersize (which includes preamble and data).

**Excessive Collisions.** The bit transmitter has transmitted all of the bits in the transmit buffer specified by the transmit buffersize, and the attempt count is equal to the maximum transmit attempt count allowed.

### B2.3 Transmit Component Action Descriptions

**Construct Frame.** This action encapsulates the data field with the Preamble, SFD, DA, SA, Length, PAD, and FCS fields.

**Start Frame Transmission.** This action initiates bit transmission of the frame.

**Start Jam Transmission.** This action causes the bit transmitter to transmit the bits of the jam pattern.

**Indicate Successful Transmission.** This action reports that the transmission was successful.

**Indicate Transmit Failure.** This action reports the failure of transmission and the reason.

**Increment Attempt Count.** This action increments the counter used to record the number of attempts made to transmit the same frame.

**Reset Attempt Count.** This action initializes the attempt count to 0.

**Start Backoff Timer.** This action computes the random backoff delay time and sets the backoff timer to that time.

**Start Delay Timer.** This action sets the delay timer to the interframe gap time.

**Stop Delay Timer.** This action turns the delay timer off.

**Perform Initialization.** This action turns all timers off and ensures that carrier is considered off and collision detect down. All counters are reset. Any implementation specific variables are initialized.

### B2.4 Transmit Component State Descriptions

**Start.** The transmit component has not been initialized by management.

**Idle.** The transmit component is not transmitting any data nor is it in a state where it is prevented from transmitting data.

**Transmit.** The transmit component is actively transmitting bits onto the medium.

**Jam.** The transmit component is actively transmitting jam bits onto the medium.

**Backoff.** The transmit component is waiting for its random backoff delay to expire before attempting to retransmit a frame.

**Backoff Defer.** The transmit component is waiting for both the medium to become available and for its backoff time delay to expire before attempting to retransmit a frame.

**Backoff Delay.** The transmit component is waiting for the interframe gap and the backoff delays to expire before attempting to retransmit a frame.

**Defer No Wait.** The transmit component has no frame to transmit and it cannot transmit one if it gets one because the medium is busy.

**Delay No Wait.** The transmit component has no frame to transmit and it could not if it had one because it is waiting for the interframe gap time to expire.

**Defer Wait.** The transmit component is waiting for the medium to become free before attempting to transmit or retransmit the frame.

**Delay Wait.** The transmit component is waiting for the interframe gap time to expire before attempting to transmit or retransmit the frame.

### B3. Receive Component Overview

The receive component is responsible for handling all events that affect the reception of a frame from the media. (See Fig B2 and Table B2.)



**Fig B2**  
Receive Component State Diagram

**Table B2**  
Receive Component State Transition

Current State	Event	Action	Next State
0. Start	Initialize	- Perform Initialization	Idle
1. Idle	Carrier On	- Start Receiving	Receive
2. Receive	Carrier Off	- Process Frame Received	Idle

#### B3.1 Receive Component Event Descriptions

**Initialize.** This event is generated by management to start up the component.

**Carrier On.** This event indicates that the physical layer has detected a change in carrier sense from no carrier to carrier.

**Carrier Off.** This event indicates that the physical layer has detected a change in the state of carrier sense from carrier to no carrier.

#### B3.2 Receive Component Action Descriptions

**Perform Initialization.** This action turns all timers off and ensures that carrier is considered off and collision detect down. All counters are reset. Any implementation specific variables are initialized.

**Start Receiving.** This action begins the processes of accepting bits and appending them to the buffer used to contain the frame.



**Process Frame Received.** If the frame is not addressed to this station, then ignore the frame. Otherwise, check the frame for errors. If there are no errors, pass frame up to the LLC sublayer indicating no error. Otherwise, pass the frame to the LLC sublayer indicating the error.

### **B3.3 Receive Component State Descriptions**

**Start.** The receive component has not been initialised by management.

**Idle.** The receive component is not actively receiving bits of data from the line.

**Receive.** The receive component is receiving bits of data from the line.

## Appendix C Application Context, Selected Medium Specifications

### C1. Introduction

This Appendix provides general guidance, to both the design engineer and the eventual user of specific product implementations, on what particular sections of the ISO 8802-3 CSMA/CD Local Area Network Standard might be considered useful for different application environments. It is to be emphasized that the material in this Appendix is very general, as the standard specifications are intended to be relatively application-independent. Nevertheless, certain specifications may apply more to one application environment than another. What follows are brief descriptions of application environments and lists of those generic parameters of the physical layer specifications thought to be useful in relating a general set of user requirements to a specific standard specification and its related medium. *Once a basic relationship is identified, the reader is directed to a specific section of the standard for detailed design specifications.*

### C2. Type 10BASE5 Applications

One of the major arenas for local area networks is the interconnection of work stations throughout a large department or single building. The ability to handle all kinds of message traffic at relatively high data rates among a large set of work stations are typical characteristics of these environments. Usually the basic interconnection trunk cable is installed and left in place permanently or for extended periods while work station placement may shift from time to time. The Type 10BASE5 specification provides the primary baseband backbone for intraplant CSMA/CD interconnections. Sections 7 and 8 of the standard provide detailed specifications for the physical layers associated with Type 10BASE5 environments. The generic physical layer parameters are as follows:

Maximum unrepeatereed cable segment	500 m
Maximum number of MAUs per segment	100
Connector type	Type N or coaxial "tag"
Breakdown voltage, MAU function	250 V ac rms
MTBF	1 million hours
Total Segment Resistance	5 $\Omega$
MAU separation	2.5 m
Connection shunt capacitance	4 pF
AUI functionality	DO, DI, CI, (CO optional)

### C3. Type 10BASE2 Applications

Another major arena for local area networks is the interconnection of work stations throughout a small department or work area. The ability to handle all kinds of message traffic at relatively high data rates among a selected set of locally clustered work stations are the typical characteristics of these environments. In addition, the basic interconnection trunk cable is likely to be moved frequently by the local users of the equipment to suit evolving needs. The Type 10BASE2 specification provides an interconnection schema that complements the Type 10BASE5 backbone in a hierarchical manner for intradepartment or work area CSMA/CD interconnections. Sections 7 and 10 of the standard provide detailed specifications for the physical layers associated with Type 10BASE2 environments. The generic physical layer parameters are as follows:

Maximum unrepeaters cable segment	185 m
Maximum number of MAUs per segment	30
Connector type	Type BNC "T"
Breakdown voltage, MAU function	500 V ac rms
MTBF	100 000 hours
Total Segment Resistance	15 $\Omega$
MAU separation	0.5 m
Connection shunt capacitance	8 pF
AUI functionality	DO, DI, CI

### C4. Type FOIRL Applications

Applications information for use of 60/125  $\mu\text{m}$  optical fiber is under consideration.

## Appendix D

### Receiver Wavelength Design Considerations

Reference 9.9.4.1.1, wavelength.

The center wavelength of the optical source emission is currently specified to be between 790 nm and 860 nm. Although these limits are acceptable, it is currently recognized, through the examination of manufacturers' current data, that greater choices of emitters can be obtained by extending the allowable wavelength to 910 nm.

An upper limit of 910 nm allows the selection of devices nominally centered at a lower wavelength, for example, 880 nm. This allows a tolerance for manufacturing variations, for example,  $\pm 20$  nm, and a tolerance for an operating temperature range (typically,  $0.3$  nm/ $^{\circ}$ C).

It is anticipated that future fiber optic applications including Local Area Networks will use the 910 nm upper limit for first window systems. It is therefore recommended that implementors specify receiver sensitivity over a center wavelength range from 790 nm to 910 nm.

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