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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC CORPORATION, HTC AMERICA, INC., AND APPLE INC.,
Petitioners,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC
Patent Owner

Case IPR2016-01135¹
Patent No. 5,812,789

PETITIONER'S REPLY

¹ Case IPR2017-00512 has been joined with this proceeding.

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 A. The combination of Bowes, TMS, and Thomas teaches “the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.”2

 1. The Petition sets forth that the combination of Bowes and Thomas renders obvious “the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.”3

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PETITIONER'S UPDATED EXHIBIT LIST

June 9, 2017

Ex. 1001	U.S. Patent No. 5,812,789
Ex. 1002	Prosecution History of U.S. Patent No. 5,812,789
Ex. 1003	Declaration of Robert Colwell, Ph.D., Under 37 C.F.R. § 1.68
Ex. 1004	Curriculum Vitae of Robert Colwell, Ph.D.
Ex. 1005	U.S. Patent No. 5,546,547 to Bowes <i>et al.</i> ("Bowes")
Ex. 1006	Texas Instruments, Inc., Houston, TX, "TMS320C8x System Level Synopsis," (September 1995) (Literature Ref. SPRU113) ("TMS")
Ex. 1007	U.S. Patent No. 5,001,625 to Thomas <i>et al.</i> ("Thomas")
Ex. 1008	R. Gove, "The MVP: A Highly-Integrated Video Compression Chip", IEEE 1994 ("Gove")
Ex. 1009	U.S. Patent No. 5,768,533 to Ran ("Ran")
Ex. 1010	U.S. Patent No. 5,742,797 to Celi <i>et al.</i> ("Celi")
Ex. 1011	Joint Claim Construction and Prehearing Statement, <i>Parthenon Unified Memory Architecture LLC v. Apple Inc.</i> , case no. 2:15-cv-632-JRG-RSP (Feb. 16, 2016, E.D. Tex.)
Ex. 1012	Decision of Institution of <i>Inter Partes</i> Review, <i>Samsung Elec. Co., Ltd., et al. v. Parthenon Unified Memory Architecture LLC</i> , IPR2015-01944 (Paper No. 7)
Ex. 1013	Claim Construction Memorandum Opinion and Order, <i>Parthenon Unified Memory Architecture LLC v. ZTE Corp. et al.</i> , No. 2:15-CV-00225 (E.D. Tex.)
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Ex. 1015	Claim Construction Memorandum Opinion and Order, <i>Parthenon Unified Memory Architecture LLC v. HTC Corp. et al.</i> , 2:14-CV-00690 (E.D. Tex.)

Ex. 1016	Claim Construction Memorandum Opinion and Order, <i>ST Microelectronics, Inc. v. Motorola, Inc. et al.</i> , No. 4:03-CV-00276 (E.D. Tex.)
Ex. 1017	"Pentium and Pentium Pro Processors and Related Products," ISBN 1-55512-265-5
Ex. 1018	<i>Parthenon Unified Memory Architecture LLC v. Apple Inc.</i> , case no. 2:15-cv-632-JRG-RSP, Document No. 10 (June 16, 2015, E.D. Tex.)
Ex. 1019	Texas Instruments, Inc., Houston, TX, "TMS320C80 to TMS320C82 Software Compatibility, User's Guide," (November 1995) (Literature Ref. SPRU154)
Ex. 1020	Bader Declaration (including Appendix A)
Ex. 1021	Declaration of Yakov Zolotorev in Support of Motion for <i>Pro Hac Vice</i> Admission
Ex. 1022	Deposition Transcript of Dr. Mitchell A. Thornton

I. Introduction

The Petition and the record as a whole provides detailed reasons why a person of skill in the art (“POSITA”) would have understood the combination of Bowes, TMS, and Thomas (in addition to other cited art) to render obvious each and every limitation of the challenged claims of the ’789 patent.

Patent Owner does not dispute the teachings of Bowes, TMS, Thomas or the other cited references as applied to the claims. Instead, Patent Owner only argues that a POSITA would not combine Bowes and Thomas because such a combination would reduce the bus bandwidth for the DSP below the bandwidth necessary to operate in real time. As shown below, this argument fails because it ignores the entirety of Thomas, as well as the teachings of Bowes and TMS, in that, as Patent Owner’s expert effectively admits, Thomas discloses a bus with more than twice the bandwidth necessary to support real time operations in Bowes.

As discussed in more detail below, Thomas teaches using two processing units, each using half the bus, where the bus is at least twice the size of the memory bus that is needed for real time operation in Bowes. Accordingly, Patent Owner’s argument fails because it ignores the fact that the bus teachings from Thomas, when combined with Bowes’s system, would provide more than sufficient bandwidth for the DSP to operate in real time even when sharing the bus with another device.

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