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STACK CONTROL LOGIC UNIT IS responsive to a STACK ...

Fair arbitration technique for a split transaction bus in a multiprocessor ...

Grant US4785394A • Michael A. Fischer • Datapoint Corporation

Priority 1986-09-19 • Filing 1986-09-19 • Grant 1988-11-15 • Publication 1988-11-15

An arbitration techique for a split transaction **bus** of a computer system obtains higher data throughput as a result of giving responders (e.g. memories) absolute priority over initiators (e.g. processors and I/O adapters), as a result of ...

Digital signal processor architecture

Grant US5954811A • Douglas Garde • Analog Devices, Inc.

Priority 1996-01-25 • Filing 1996-01-25 • Grant 1999-09-21 • Publication 1999-09-21

transfer selection means responsive to said instructions for **simultaneously** addressing quad operands of 32 bits each in a single row of one or more of said second and third memory banks and selectably and **simultaneously** providing one, two ...

Bus structure for overlapped data transfer

Grant US5001625A • James H. Thomas • Gould Inc.

Priority 1988-03-24 · Filing 1988-03-24 · Grant 1991-03-19 · Publication 1991-03-19

An improved system **bus** structure for versatile use in various digital computer architecture configurations, particularly those of mini-supercomputers, and, designed to support high speed, high reliability, parallel processing of bi- ...

Method and apparatus for providing multiple clients simultaneous access to a ...

Grant US5384890A • Eric C. Anderson • Apple Computer, Inc.

Priority 1992-09-30 • Filing 1992-09-30 • Grant 1995-01-24 • Publication 1995-01-24

A method and apparatus for providing multiple clients simultaneous access to a sound input/output (I/O) data stream. The present invention provides a method and apparatus for providing multiple programming data structures and multiple ...

Process and device for managing the conflicts raised by multiple access to same

Grant US4426681A • Pierre C. A. Bacot • Cii Honeywell Bull

Priority 1980-01-22 • Filing 1981-01-22 • Grant 1984-01-17 • Publication 1984-01-17

... one data item in the cache memory of processor unit CPUk for access via the connector **bus**, said process avoiding a conflict between processing of internal and external requests by the same cache memory while promoting the **simultaneous** ...

System for storing data and for providing simultaneous plural access to data by ...

Grant US5671386A • David Kim Blair • Philips Electronics North America Corporation

