Data Sheet
March 1993

AT&T Microelectronics

AT&T DSP3210 Digital Signal Processor
The Multimedia Solution

Features and Benefits

Feature	Benefit
Microprocessor bus compatibility: ■ 32-bit, byte-addressable address space ■ Retry, relinquish/retry, and bus error support ■ Page mode DRAM support ■ Direct support for both 680x0 and 80x86 signaling	Designed for efficient bus master designs allowing the DSP3210 to easily be incorporated into µP-based systems. The 32-bit, byte-addressable space enables the DSP3210 and a µP to share common address space and pointer values as well.
AT&T *VCOS*™ operating system: ■ Real-time, multitasking operating system ■ Uses host rather than local memory ■ True parallel processing ■ Complete task management	Open development environment: ■ Dramatically lower system costs ■ Full utilization of both µP and DSP3210 ■ Simplifies both algorithm and application development
Full 32-bit floating-point arithmetic C-like assembly language Single-cycle PC relative addressing	Ease of programming/higher performance.
All instructions are single-cycle (four memory accesses per instruction cycle)	Higher performance.
Access to DSP32C programs	Access to the largest existing 32-bit DSP SW base.
*Logic Automation** model	Faster, more efficient system development.

Introduction

The DSP3210 brings the power of floating-point signal processing to personal computers and workstations, opening a wide range of multimedia applications. The DSP3210 has been engineered with a single focus: to enable advanced multimedia applications in personal computers and workstations. Based on AT&T's DSP32C architecture, the DSP3210 has the unique ability to be integrated into personal computer and workstation system designs. Particular attention is paid to primary bus interfacing; the DSP3210 is compatible with both 80x86 and 680x0 microprocessor signaling. This allows designers to easily create low-cost systems by using the DSP3210 as a bus-master device. A full, bus-level *SmartModel** of the DSP3210 is offered by Logic Automation, Inc. for system simulation of designs incorporating the DSP3210.

Along with its optimizing C-compiler and assembly-language software tools, the DSP3210 is further supported with AT&T's *VCOS* operating system.

The *VCOS* operating system provides a powerful real-time, multitasking and multiprocessing environment which effectively manages multimedia applications across various computer platforms. By employing innovative task- and code-management techniques, *VCOS* operating system allows the DSP3210 to use existing system memory in PCs and workstations rather than expensive dedicated SRAM for DSP program and data storage.

Complete real-time debugging tools are included to speed both application and algorithm development. By separating the application and algorithm development phases of multimedia software creation, the *VCOS* operating system greatly simplifies and shortens development schedules.

* *Logic Automation* and *SmartModel* are registered trademarks of Logic Automation, Inc.

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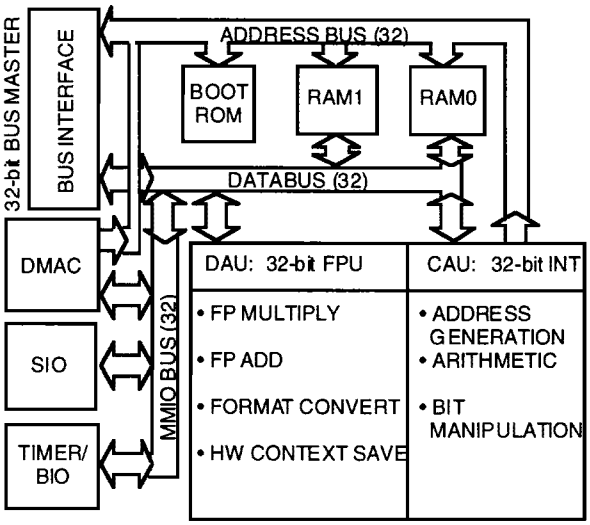

Figure 1. DSP3210 Block Diagram

The *VCOS* operating system includes its own multimedia library, complete with speech processing, speech recognition, graphics, music processing, and modem modules. The *VCOS* system is an open environment, so application developers may access third-party modules as well as AT&T's library.

Figure 1 shows the DSP3210 block diagram. In addition to a brief description of the DSP3210's application in multimedia environments, each functional unit, the instruction set, and the processor control features are described.

This data sheet is designed to be a companion document to the *AT&T DSP3210 Information Manual* (MN91-006OMOS). The brief descriptions of the DSP3210's architecture and instruction set are greatly expanded in the information manual. The data sheet is intended to give the latest, up-to-date, timing specifications and boot ROM firmware descriptions, while the information manual contains the detailed information needed to understand the DSP3210's operation.

Applications

The DSP3210 may be used in a variety of applications due to its raw floating-point power, low cost, low power dissipation, and interfacing flexibility. However, multimedia was the primary application considered when designing the DSP3210.

PC/Workstation Multimedia Applications

DSP3210 Motherboard Implementations

The DSP3210 is intended to be used in PC and workstation system architectures in which the DSP3210 is a parallel processor to a host processor. The DSP3210 maintains a 32-bit bus-master interface to system memory (see Figure 2).

The primary benefit of this system architecture is the DSP's ability to access program and data from system memory without host intervention. Furthermore, expensive local SRAM is replaced by the computer's existing system memory.

DSP3210 Add-In Cards

Existing computers with EISA, ISA, MCA, *NuBus**, SBus, and proprietary bus or CPU direct-slot capabilities can be easily retrofitted with low-cost DSP3210 boards to perform identical applications to motherboard-equipped PCs. In systems with direct CPU slots or 32-bit buses capable of bus mastering, these DSP3210-based cards require no DSP memory (memory is accessed via the bus or CPU direct slot).

Using the visible caching technique native to the *VCOS* operating system, boards installed in lower-bandwidth buses use inexpensive local 32-bit DRAM on the DSP3210 add-in card. In these environments, the DSP3210 uses the bus primarily to transfer tasks and I/O to and from the DSP3210 card.

* *NuBus* is a registered trademark of Massachusetts Institute of Technology.

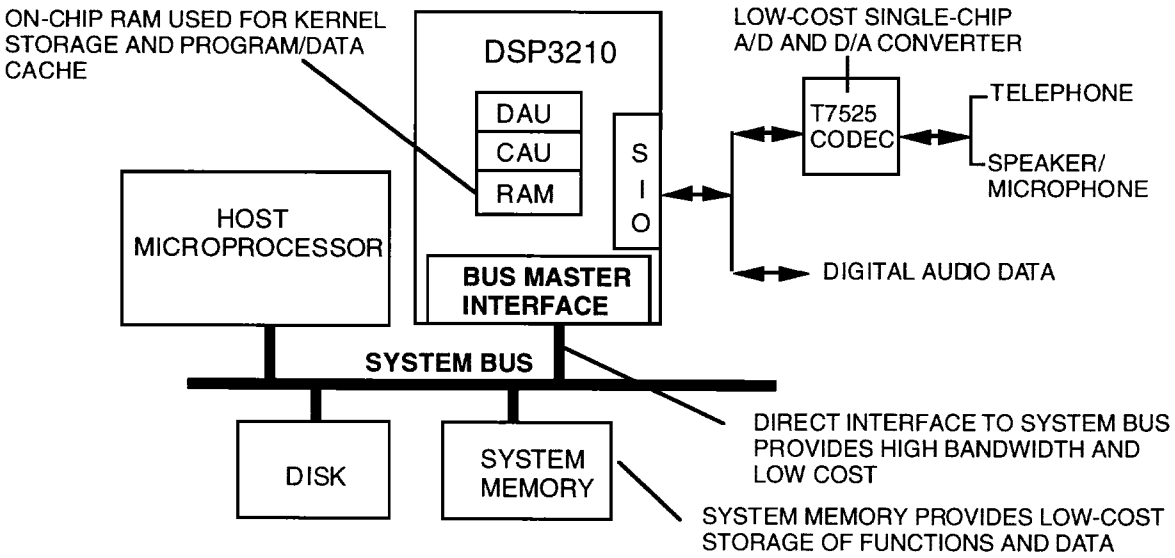

Figure 2. Typical DSP3210 PC/Workstation Motherboard Configuration

Applications (continued)

System Integration Under the *VCOS* Operating System

Since the DSP3210 supports both big- and little-endian byte ordering, sharing both data and pointer values with any host microprocessor is easily accomplished. This is especially useful in multimedia applications where intimate communications between the host microprocessor and DSP are necessary. For real-time signal processing under the *VCOS* operating system, on-chip SRAM is loaded with code and data from system memory before executing. Applications are broken into functions that are executed successively in this fashion. Nonreal-time background jobs may be either executed from system memory or cached into the DSP3210's internal memory.

Functional Description

Functional Units

The DSP3210 consists of seven functional units: control arithmetic unit (CAU), data arithmetic unit (DAU), on-chip memory (RAM0, RAM1, boot ROM), bus interface, serial I/O (SIO), DMA controller (DMAC), and timer/bit I/O (BIO) unit.

Control Arithmetic Unit (CAU)

The CAU is responsible for performing address calculations, branching control, and 16- or 32-bit integer arithmetic and logic operations. It is a RISC core consisting of a 32-bit arithmetic logic unit (ALU) that performs integer arithmetic and logical operations, a full 32-bit barrel shifter for efficient bit manipulation operations, a 32-bit program counter (PC), and twenty-two 32-bit general-purpose registers.

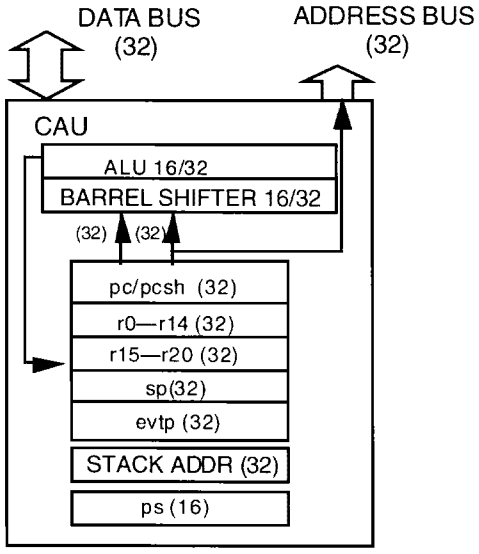

Figure 3. Control Arithmetic Unit (CAU)

The CAU performs two types of tasks: executing integer, data move, and control instructions (CA instructions), or generating addresses for the operands of floating-point instructions (DA instructions). CA instructions perform load/store, branching control, and 16- and 32-bit integer arithmetic and logical operations. DA instructions can have up to four memory accesses per instruction, and the CAU is responsible for generating these addresses using the postmodified, register-indirect addressing mode (one address is generated in each of the four states of an instruction cycle).

Data Arithmetic Unit (DAU)

The DAU is the primary execution unit for signal processing algorithms. This unit contains a 32-bit floating-point multiplier, a 40-bit floating-point adder, four 40-bit accumulators, and a control register (dauc). The multiplier and adder work in parallel to perform 16.7 million computations per second, yielding 33 MFLOP performance. The multiplier and adder each produce one floating-point result per instruction cycle. The DAU contains a four-stage pipeline (fetch, multiply, accumulate, write). Thus, in any instruction cycle, the DAU may be processing four different instructions, each in a different stage of execution.

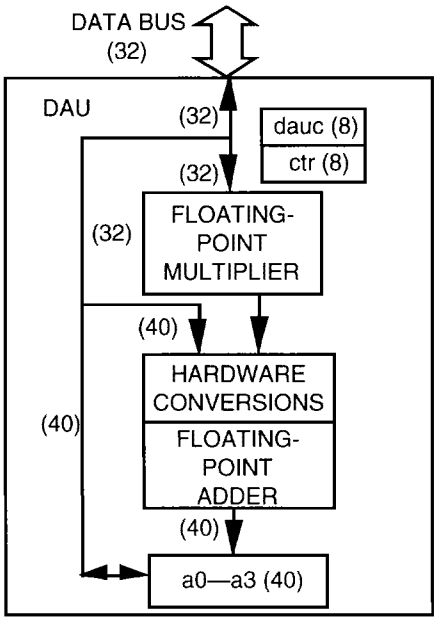

Figure 4. Data Arithmetic Unit (DAU)

The DAU supports two floating-point formats: single precision (32-bit) and extended single precision (40-bit). Extended single precision provides eight additional mantissa guard bits. Postnormalization logic transparently shifts binary points and adjusts exponents to prevent inaccurate rounding of bits when the floating-point numbers are added or multiplied. This eliminates concerns such as scaling and quantization error.

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