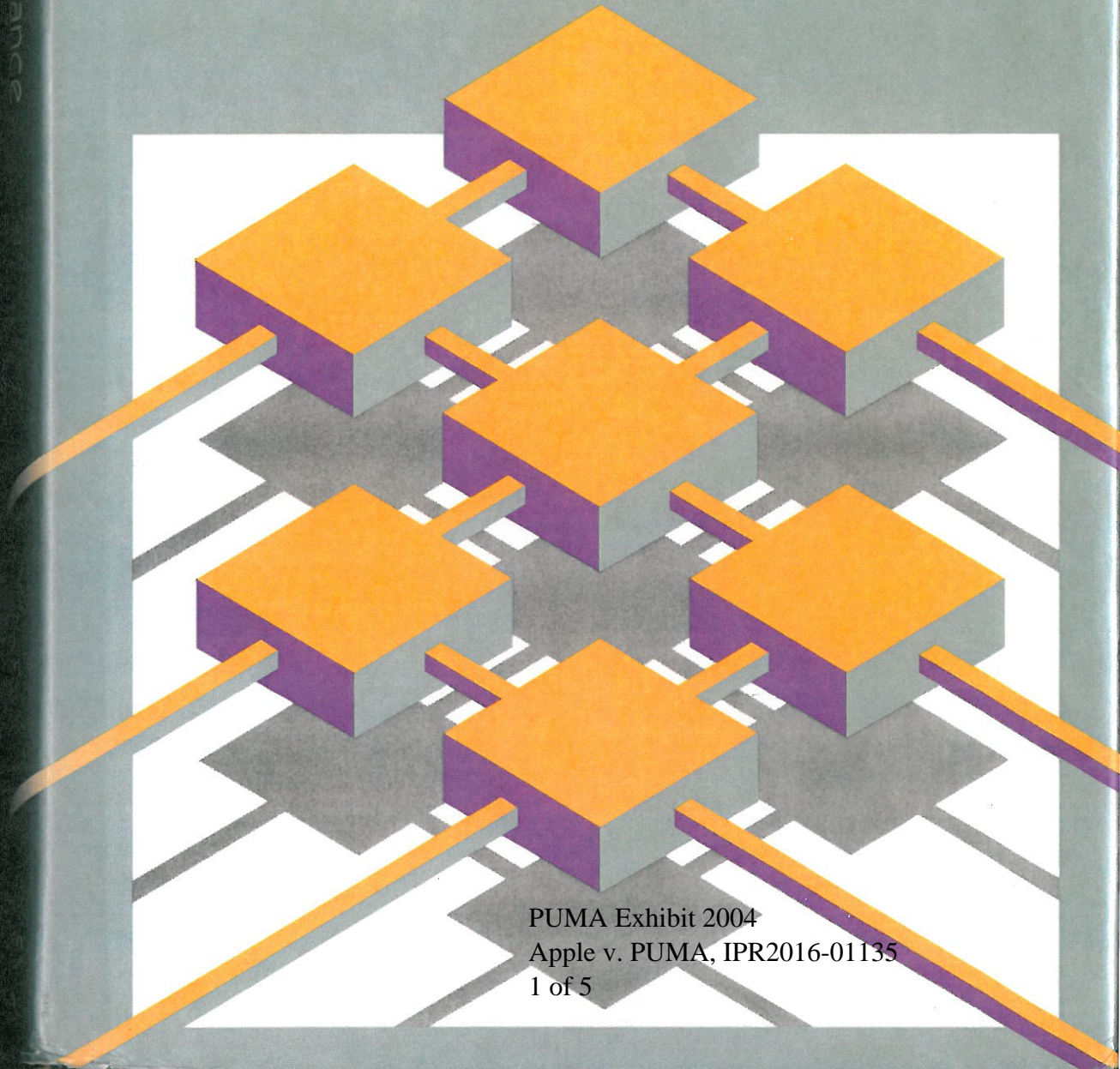


Third Edition

High-Performance Computer Architecture

Harold S. Stone

High-Performance



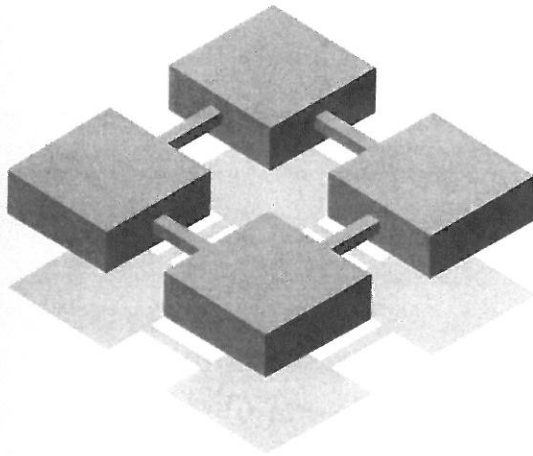
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Research Center
and
Courant Institute
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- Gharachorloo, K., 388
- Gigaflops.** *See* Gflops
- Global memory** A memory directly accessible by every processor in a multiprocessor; 359, 418–419, 423–453
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- Goodman, J. R., 48, 54, 387, 390, 449
- Gottlieb, A., 378, 442, 443
- Granularity** A measure of the size of an individual task to be executed on a parallel processor; 342–359, 417–420
- Gravitation,** 240
- Greatest common divisor (GCD),** 315
- Greedy strategy** A strategy that initiates a new pipeline operation at the earliest opportunity; 180–182
- Green, P. E., Jr., 447
- Grohoski, G. F., 221
- Grosch's Law** An empirical rule that says that the cost of computer systems increases as the square root of the computational power of the systems; 14
- Gupta, S. C., 46
- Gustafson, J. L., 320, 322
- Halstead, R., 421
- Hash lookup** A search technique in which the search key is transformed to an address at which the search begins; 326
- Hayes, J. P., 23
- Heidelberger, P., 446, 449
- Heller, D. E., 268, 308
- Hennessy, J., 23, 56–57, 228
- Hierarchy (of memory system)** A multi-level memory structure in which successive levels are progressively larger, slower, and less costly; 25, 28, 100–101, 137
- High-speed buffer memory** A memory that holds data en route between a large main memory and the registers of a high-speed processor; 318
See also Intermediate memory
- Hill, M., 60, 99, 101, 216
- Hillis, W. D., 338, 384, 385
- Hit.** *See* Cache hit
- Hit ratio** The ratio of the number of cache hits to the total number of cache accesses; 34, 43, 114
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- Hoevel, L. W., 76
- Hopcroft, J. E., 458
- Horowitz, M. 56–57
- Hoshino, T., 236, 238, 253, 287, 357, 370, 445, 448
- Hot-spot contention** An interference phenomenon observed in multiprocessors due to memory access statistics being slightly skewed from a uniform distribution to favor a specific memory module; 376–378, 381–382, 444, 474
- HP Spectrum,** 214
- Hwang, K., 227, 433
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- Hypercube** A parallel processor whose interconnection structure treats individual processors as the nodes of a multidimensional cube and interconnects two processors if the corresponding nodes of the cube are neighbors; 252, 384–385
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- IBM Corporation,** 210, 320
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- ILLIAC IV,** 164–165, 237, 247–253, 257–259, 287, 289, 330, 333
- Image processing** A computation performed on a digitized representation of an image whose purpose is to enhance the image or to extract information about the image; 13
- Inclusion principle** The property that a