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Paper No. 7
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD. and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2015-01944
Patent 5,812,789

Before MICHAEL R. ZECHER, JAMES B. ARPIN, and
MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314(a) and 37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, Samsung Electronics Company, Limited and Samsung Electronics America, Incorporated (collectively "Samsung"), filed a Petition requesting an *inter partes* review of claims 1, 3–6, 11, and 13 of U.S. Patent No. 5,812,789 (Ex. 1001, "the '789 patent"). Paper 2 ("Pet."). Patent Owner, Parthenon Unified Memory Architecture Limited Liability Corporation ("Parthenon"), filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted unless the information presented in the Petition shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Taking into account the arguments presented in Parthenon's Preliminary Response, we conclude that the information presented in the Petition establishes that there is a reasonable likelihood that Samsung would prevail in challenging claims 1, 3, 5, 11, and 13 of the '789 patent as unpatentable under 35 U.S.C. § 102(e), and claims 4 and 6 of the '789 patent as unpatentable under 35 U.S.C. § 103(a). Pursuant to § 314, we hereby institute an *inter partes* review as to these claims of the '789 patent.

A. Related Matters

The '789 patent is involved in the following district court cases: (1) *Parthenon Unified Memory Architecture LLC v. Huawei Techs. Co.*, No. 2:14-cv-00687-JRG-RSP (E.D. Tex.); (2) *Parthenon Unified Memory Architecture LLC v. Motorola Mobility, Inc.*, No. 2:14-cv-00689-JRG-RSP (E.D. Tex.); (3) *Parthenon Unified Memory Architecture LLC v. HTC Corp.*,

No. 2:14-cv-00690-RSP (E.D. Tex.); (4) *Parthenon Unified Memory Architecture LLC v. LG Elecs., Inc.*, No. 2:14-cv-00691-JRG-RSP (E.D. Tex.); (5) *Parthenon Unified Memory Architecture LLC v. Samsung Elecs. Co.*, No. 2:14-cv-00902-JRG-RSP (E.D. Tex.); (6) *Parthenon Unified Memory Architecture LLC v. Qualcomm Inc.*, No. 2:14-cv-00930-JRG-RSP (E.D. Tex.); (7) *Parthenon Unified Memory Architecture LLC v. ZTE Corp.*, No. 2:15-cv-00225-JRG-RSP (E.D. Tex.); (8) *Parthenon Unified Memory Architecture LLC v. Apple, Inc.*, No. 2:15-cv-00621-JRG-RSP (E.D. Tex.); and (9) *STMicroelectronics, Inc. v. Motorola Inc.*, No. 4:03-cv-00276-LED (E.D. Tex.). Pet. 1–2; Paper 5, 2.

In addition to this Petition, Samsung filed other petitions challenging the patentability of a certain subset of claims in the following patents owned by Parthenon: (1) U.S. Patent No 7,321,368 B2 (Case IPR2015-01500); (2) U.S. Patent No. 7,777,753 B2 (Case IPR2015-01501); (3) U.S. Patent No. 7,542,045 B2 (Case IPR2015-01502); (4) U.S. Patent No. 8,054,315 B2 (Case IPR2015-01494); (5) U.S. Patent No. 8,681,164 B2 (Case IPR2015-01503); and (6) U.S. Patent No. 5,960,464 (Case IPR2015-01946). Pet. 2.

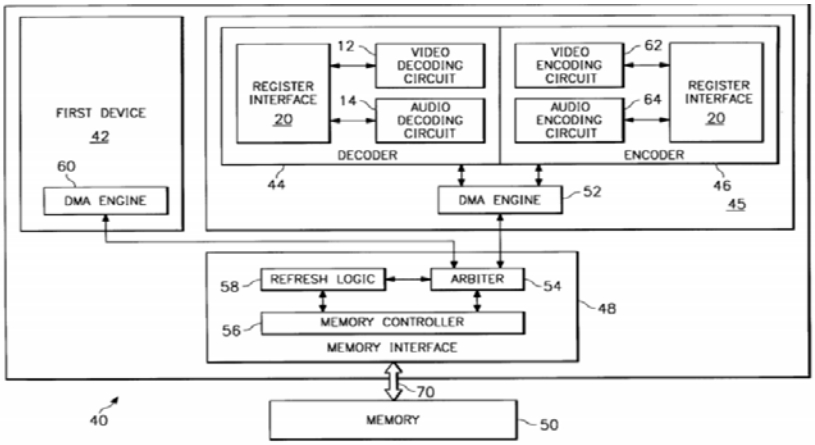
B. The '789 Patent

The '789 patent, titled "Video and/or Audio Decompression and/or Compression Device That Shares a Memory Interface," issued September 22, 1998, from U.S. Patent Application No. 08/702,911, filed on August 26, 1996. Ex. 1001, at [54], [45], [21], [86]. Because the application that led to the '789 patent was filed August 26, 1996, the '789 patent is set to expire on August 26, 2016.

The ’789 patent generally relates to an electronic system having a video or audio decompression/compression device and, in particular, to sharing a memory interface between such a device and another device in the electronic system. Ex. 1001, 1:18–23. In the Background section, the ’789 patent discloses advantages associated with using encoders and decoders to compress and decompress video and audio sequences, respectively. *See id.* at 1:32–2:3. The ’789 patent then proceeds to disclose the architecture of a conventional encoder/decoder prior to asserting that there are a number of problems associated with such an architecture. *See id*. at 2:4–25, Figs. 1a, 1b. According to the ’789 patent, one of the problems includes dedicating memory to the both the encoder and decoder, thereby increasing the cost of adding these components to an electronic system. *Id*. at 2:29–37.

The ’789 patent purportedly solves this problem because the disclosed video or audio decompression/compression device does not need its own dedicated memory, but instead may share memory with another device and still operate in real time. Ex. 1001, 4:30–34. Figure 2 of the ’789 patent, reproduced below, illustrates a diagram of an electronic system containing a device having a memory interface, as well as an encoder and decoder. *Id*. at 5:1–3.

FIG. 2



As shown in Figure 2, electronic system 40 includes first device 42, decoder 44, encoder 46, memory interface 48, and memory 50. Ex. 1001, 5:23–26. Each of first device 42, decoder 44, and encoder 46 access memory 50 through memory interface 48. *Id*. at 5:15–19. Memory interface 48 further includes arbiter 54 that is configured to arbitrate between first device 42, decoder 44, and encoder 46, when these components request access to memory 50. *Id*. at 6:15–18, 9:43–49

C. Illustrative Claim

Of the challenged claims, claim 1 is independent. Independent claim 1 is directed to an electronic system coupled to a memory. Claims 3–6, 11, and 13 directly or indirectly depend from independent claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An electronic system coupled to a memory, comprising:
>
> a first device that requires access to the memory;
>
> a decoder that requires access to the memory sufficient to maintain real time operation; and
>
> a memory interface for coupling to the memory, and coupled to the first device and to the decoder, the memory interface having an arbiter for selectively providing access for the first device and the decoder to the memory and a shared bus coupled to the memory the first device, and the decoder, the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus.

Ex. 1001, 12:29–41.

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