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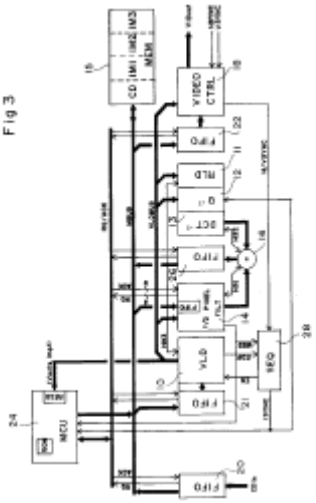
(54) System for processing images.

(57) The present invention relates to a system for processing compressed image data that arrive in packets, these packets being separated by headers including parameters. A memory bus (MBUS) is managed by a memory controller (24) in order to exchange data between processing elements and an image memory (15). A pipeline circuit (11, 12, 13) includes several processing elements, and a parameter bus (VLDBUS) is used to provide packets to be processed to the pipeline circuit as well as parameters to elements of the pipeline circuit. This parameter bus is managed by a VLD circuit that receives compressed data of the memory bus and that includes a header detector in order to provide the parameters to the elements of the pipeline circuit and to other elements of the system that require them.

Fig 3



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The present invention relates to systems for processing images, and, in particular, to a system for decoding an image encoded according to an MPEG standard.

Figure 1 represents the main elements of an MPEG decoder. Any MPEG decoder, in particular for standard MPEG 2, generally includes a variable length word decoder 10 (VLD), a sequence-of-zeros decoder 11 (RLD), an inverse quantization circuit 12 (Q^{-1}), an inverse discrete cosine transform circuit 13 (DCT^{-1}), a half-pixel filter 14, and a memory 15. The encoded data are input via a bus CDin, and the decoded data are output via a bus VIDout. Between the input and the output, the data pass through the processing circuits 10 to 13 in the order indicated above, which is illustrated by arrows in dotted lines. The output of the decoder is provided by an adder 16 that sums the outputs of the filter 14 and of the cosine transform circuit 13. The filter 14 needs a previously decoded image portion stored in memory 15.

Figure 2A illustrates a step of decoding an image portion IM1 in the process of reconstruction. The decoding of an image is carried out macroblock by macroblock, where a macroblock generally corresponds to a 16 x 16 pixel image block.

Figure 2B illustrates a format example, noted 4:2:0, of a macroblock MB. This macroblock includes a luminance block formed by four blocks Y1 to Y4 of 8 x 8 pixels and a chrominance block formed by two blocks U and V of 8 x 8 pixels. Another possible format is the format noted 4:2:2, wherein the chrominance block includes two blocks of 8 x 16 pixels.

In the current image IM1 of Figure 2A, a current macroblock MBc is decoded, previously decoded macroblocks being represented by crosshatching. In the general case, the macroblock MBc is reconstructed from a predictor macroblock MBp obtained in a previously decoded image

IMO. To find this predictor macroblock MBp, the data used for decoding the macroblock MBc provide a movement compensation vector V that defines the position of the predictor macroblock MBp with respect to the position P of the macroblock MBc in the image.

The predictor macroblock MBp is obtained in the memory 15 that stores the previously decoded image IMO and is provided to the filter 14, while the cosine transform circuit 13 processes data corresponding to the macroblock MBc.

The decoding that has just been described is a so-called predicted-type decoding. The decoder macroblock is also referred to as being of the predicted type. According to the MPEG standards, three main types of macroblocks exist, referred to as "intra," "predicted" and "bidirectional."

An intra macroblock corresponds directly to an image block, that is to say that it is not combined with a predictor macroblock at its output from the cosine transform circuit 13.

A predicted macroblock, described above, is combined with a macroblock of a previously decoded image, which, in the order of display, occurs before the image in the process of reconstruction.

A bidirectional macroblock is combined with two predictor macroblocks of two previously decoded images, respectively. These two images are respectively before (forward image) and subsequent (backward image), respectively, in the display order, with respect to the image in the process of reconstruction. Thus, the encoded images arrive in an order different from the display order.

Moreover, each of the predicted or bidirectional macroblocks is of progressive or interlaced type. When the macroblock is progressive, the circuit DCT^{-1} provides the lines of the macroblock in consecutive order. When the macroblock is interlaced, the circuit DCT^{-1} first

provides the even lines of the macroblock, then the odd lines. In addition, a predictor block that serves to decode a predicted or bidirectional macroblock is also of progressive or interlaced type. When the predictor macroblock is interlaced, it is divided into two half-macroblocks, one corresponding to even lines and the other to odd lines, each predictor half-macroblock being obtained at different places of the same previously decoded image.

An image is also of intra, predicted or bidirectional type. An image of intra type contains only intra macroblocks, an image of predicted type contains intra or predicted macroblocks, and an image of bidirectional type contains intra, predicted or bidirectional macroblocks.

In order to provide the different decoding parameters to the different circuits of the decoder, in particular the vectors V and the macroblock types, the flow of encoded data includes headers. There are several headers, namely:

- an image sequence header that includes, in particular, two quantization tables to be provided to the inverse quantization circuit 12, one being used for the macroblocks of intra type of the sequence and the other for macroblocks of the predicted or bidirectional type;

- an image group header of a sequence, which includes no information used for the decoding;

- an image header that includes the type (predicted, intra, bidirectional) of the image and information on the use of the movement compensation vectors;

- an image slice header including information used for correcting errors; and

- a macroblock header including the type of the macroblock, a quantization scale coefficient to be provided to the inverse quantization circuit 12, and the components of the movement compensation vectors. Up to four vectors can be used in the case of the processing of an interlaced bidirectional macroblock.

The high hierarchy headers (image, group, sequence) can moreover include private data used, for example, for displaying text at the same time as an image. These private data can also be used by elements external to the decoder.

The various processing circuits of an MPEG decoder are often arranged in a series architecture, commonly referred to as "pipeline" architecture, which makes it possible to process high data flow rates, but which is very complex and rigid, that is to say that it is difficult to adapt it to variants of the standards and it is poorly suited for the use of display and private data.

The simplest and least expensive solution is to connect the various processing circuits to the memory via a common bus managed by a multi-task processor.

The European Patent Application 0 503 956 (C Cube) describes such a system, which includes a processor managing the transfers on the bus and three coprocessors performing the processing operations corresponding to the circuits 10 to 14. Each different transfer type to be performed on the bus corresponds to a task performed by the processor. All the tasks are concurrent and executed upon interruptions of the processor, which are generated by the coprocessors. The coprocessors exchange the data to be processed via the bus and they receive instructions provided by the processor via the bus.

This system is simple, but it has been found that it does not enable the processing of the currently needed data flow.

An object of the present invention is to provide a particularly fast image decompression system that has a relatively simple structure.

Another object of the present invention is to provide such a decompression system that can easily be placed in parallel with identical decompression systems for processing particularly high compressed data flow rates.

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