IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of Owen *et al.*	§	Petition for *Inter Partes* Review
	§	
U.S. Patent No. 7,542,045	§	Attorney Docket No.: 52959.21
	§	Customer No.: 27683
Issued: Jun 2, 2009	§	
Title: Electronic System and Method For Display Using a Decoder and Arbiter To Selectively Allow Access to a Shared Memory	§	Real Party in Interest:
	§	Apple Inc.
	§	
	§	

Declaration of Robert Colwell, Ph.D.

Under 37 C.F.R. § 1.68

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I. Introduction

I, Robert Colwell, Ph.D., declare:

1. I am making this declaration at the request of Apple Inc. in the matter of the *Inter Partes* Review of U.S. Patent No. 7,542,045 ("the '045 Patent") to Owen *et al*.

2. I am being compensated for my work in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

3. In the preparation of this declaration, I have studied:

(1) The '045 Patent, Exhibit 1001;

(2) The prosecution history of the '045 Patent, Exhibit 1002;

(3) U.S. Patent No. 5,546,547 to Bowes *et al.* ("Bowes"), Exhibit 1005;

(4) "AT&T DSP3210 Digital Signal Processor The Multimedia Solution" Data Sheet March 1993 ("DSP3210 Data Sheet"), Exhibit 1006;

(5) EP 0626653 to Artieri, English translation ("Artieri"), Exhibit 1007;

(6) R. Gove, "The MVP: A Highly-Integrated Video Compression Chip", IEEE 1994 ("Gove"), Exhibit 1008;

(7) other documentation as cited in the analysis below.

4. In forming the opinions expressed below, I have considered:

(1) The documents listed above,

(2) The relevant legal standards, including the standard for obviousness provided in *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), and

(3) My own knowledge and experience, including my work experience in the fields of electrical engineering, computer engineering, computer architectures, memory interfacing, and multimedia technologies, and my experience in working with others involved in those fields, as described below.

II. Qualifications and Professional Experience

5. My complete qualifications and professional experience are described in my curriculum vitae, a copy of which can be found in Exhibit 1004. The following is a brief summary of my relevant qualifications and professional experience.

6. I have nearly 40 years of professional experience in the field of processor and system architecture design. I consider myself an expert in, among other things, CPU architecture and computer systems.

7. I received an undergraduate Bachelor of Science degree in Electrical

Engineering from the University of Pittsburgh in 1977. I received a Master's of Science degree in Computer Engineering from Carnegie Mellon University in 1978 as well as a Ph.D. in Computer Engineering in 1985.

8. From 1977 to 1980, I held an engineering position at Bell Telephone Laboratories where I worked on, among other things, microprocessor hardware design.

9. From 1980 to 1984, I held an engineering position at Perq Systems, where I worked on hardware design in computer environments. From 1985 to 1990, I held an engineering position at Multiflow Computer, where I served as a hardware architect. While at Multiflow Computer, I assisted in creating the first very long instruction word (VLIW) scientific supercomputer.

10. From 1990 to 2001, I held various positions at Intel including Senior CPU Architect and later Chief Architect (for Intel's IA-32, also known as x86). As part of my responsibilities at Intel, I co-invented Intel's P6 microarchitecture that formed the core of the Pentium II manufactured by Intel (as well as the Pentium III, Celeron, Xeon, and Centrino families). The P6 core is still very influential today, in Intel's top-of-the-line Core i3, i5, and i7 processors. In addition, I led Intel's x86 Pentium CPU architecture endeavors. I was honored to be named an Intel fellow in 1997 in recognition of my contributions to the P6 microarchitecture development.

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