

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2016-01114
Patent 7,777,753 B2

Before JAMES B. ARPIN, MATTHEW R. CLEMENTS, and
SUSAN L. C. MITCHELL, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Apple Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1, 2, 4, 7–10, and 12 (“the challenged claims”) of U.S. Patent No. 7,777,753 B2 (Ex. 1001, “the ’753 patent”). Paper 2 (“Pet.”). Parthenon Unified Memory Architecture LLC (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and the accompanying evidence, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the ’753 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1, 2, 4, 7–10, and 12 of the ’753 patent.

A. Related Proceedings

The ’753 patent is involved in several cases pending in the Eastern District of Texas. Pet. 1–2; Paper 5, 1–2. The ’753 patent also is involved in *Samsung Electronics, Ltd. v. Parthenon Unified Memory Architecture*,

Case IPR2015-01501 (instituted)¹ and was involved in *ZTE USA, Inc. v. Parthenon Unified Memory Architecture*, Case IPR2016-00670 (now terminated). Pet. 2. Petitioner also has filed other petitions seeking *inter partes* review of related patents.

B. The '753 patent

The '753 patent relates generally “to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.” Ex. 1001, col. 1, ll. 36–41. As of the effective filing date of the '753 patent,² a typical decoder included a dedicated memory, which represented a significant percentage of the cost of the decoder and which went unused most of the time. *Id.* at col. 2, ll. 21–63, col. 4, ll. 43–60, Figs. 1a–1c.

¹ The statutory deadline to issue a Final Written Decision in IPR2015-01501 is January 6, 2017. Upon issuance of a Final Written Decision in that proceeding, the panel shall determine whether it is appropriate to maintain this proceeding against all or some of the claims, upon which review is instituted, or to terminate this proceeding and vacate this Decision on Institution. *See* 35 U.S.C. § 315(d).

² The '753 patent claims the benefit of a string of earlier-filed U.S. patent applications, the earliest of which was filed on August 26, 1996. Pet. 7. Petitioner does not challenge the entitlement of the '753 patent to this earliest filing date and “believes that the '753 Patent will expire during pendency of the requested *inter partes* review proceeding.” *Id.* at 12. In a related proceeding, Patent Owner expressly stated that the expiration date for the '045 patent is August 26, 2016. Case IPR2015-01501, Paper 8, 1; *see* Prelim. Resp. 3.

To address these and other concerns, the '753 patent discloses an electronic system in which a first device and a video and/or audio decompression and/or compression device are coupled to a shared memory through a bus that may have bandwidth sufficient for the video and/or audio decompression and/or compression device to operate in real time. *Id.* at col. 4, l. 64–col. 5, l. 7. Figure 2 of the '753 patent is reproduced below.

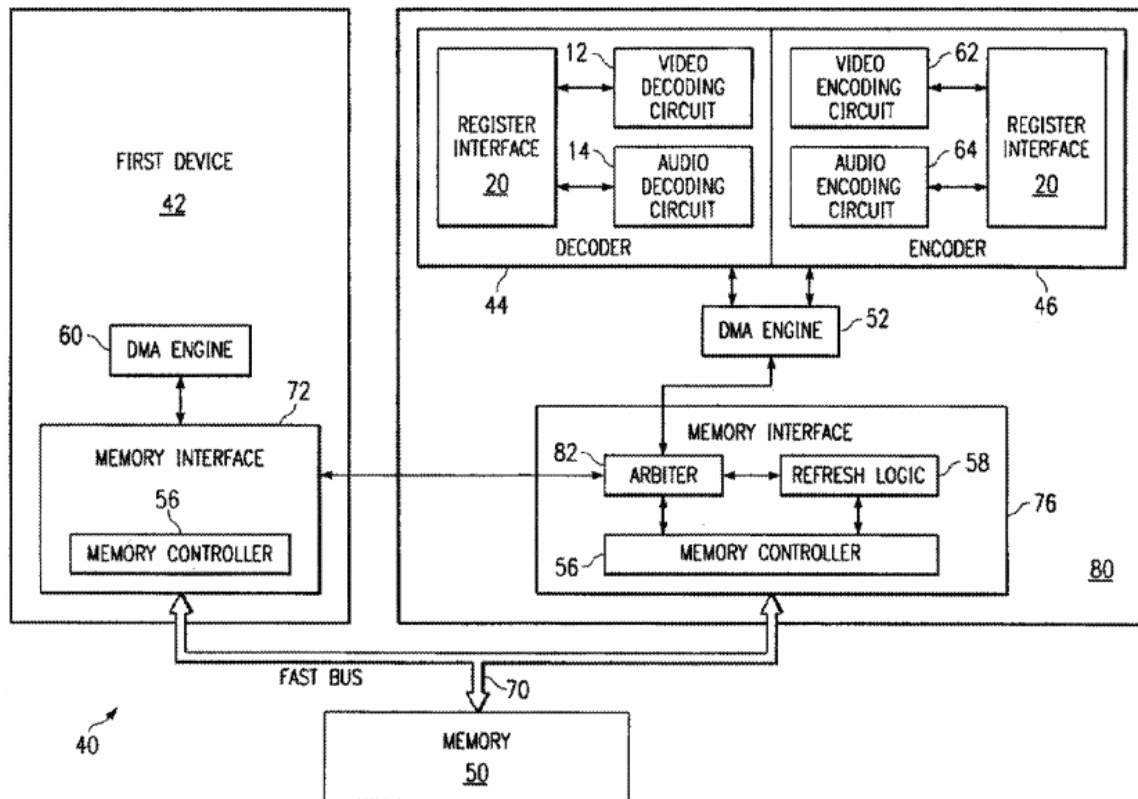


Fig. 2

Figure 2 is a block diagram of an electronic system that contains a device with a memory interface and an encoder and decoder. *Id.* at col. 6, ll. 3–5. “First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50” *Id.* at col. 6, ll. 29–32. Both first device 42 and decoder/encoder 80 have access to memory 50 through memory interfaces 72 and 76, respectively, coupled to fast bus 70. *Id.* at col. 6, ll. 27–29, col. 7, ll. 26–28, 48–51. Fast

bus 70 may have at least the bandwidth required for decoder/encoder 80 to operate in real time and, preferably, has a bandwidth of at least approximately twice the bandwidth required for decoder/encoder 80 to operate in real time. *Id.* at col. 7, ll. 48–51, col. 8, ll. 28–33.

During operation, decoder/encoder 80, first device 42, and refresh logic 58, if it is present, request access to memory 50 through arbiter 82. *Id.* at col. 12, ll. 53–56. Arbiter 82 determines which of the devices may access memory 50. *Id.* at col. 12, ll. 57–58. Decoder/encoder 80 may get access to memory 50 in the first time interval, and first device 42 may get access to memory 50 in the second time interval. *Id.* at col. 12, ll. 58–61. Direct Memory Access (DMA) engine 52 of decoder/encoder 80 determines the priority of decoder/encoder 80 for access to memory 50 and the burst length when decoder/encoder 80 has access to memory 50. *Id.* at col. 12, ll. 61–67. DMA engine 60 of first device 42 determines its priority for access to memory 50 and the burst length when first device 42 has access to memory 50. *Id.* at col. 12, ll. 65–67.

When decoder/encoder 80 or one of the other devices generates a request to access memory 50, the request is transferred to arbiter 82, and access to memory 50 is determined based on the state of arbiter 82 and on a priority scheme. *Id.* at col. 13, ll. 1–30. In particular,

[t]he state of the arbiter 82 is determined. The arbiter typically has three states. *The first state is idle* when there is no device accessing the memory and there are no requests to access the memory. *The second state is busy* when there is a device accessing the memory and there is no other request to access the memory. *The third state is queue* when there is a device accessing the memory and there is another request to access the memory.

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