Paper No._____

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.,
Petitioner,

v.

Parthenon Unified Memory Architecture LLC,
Patent Owner

Case IPR2016-01114
Patent No. 7,777,753

PETITIONER'S REPLY

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Petitioner's Updated Exhibit List
June 9, 2017

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Ex. 1002	Prosecution History of U.S. Patent No. 7,777,753
Ex. 1003	Declaration of Robert Colwell, Ph.D., Under 37 C.F.R. §1.68
Ex. 1004	Curriculum Vitae of Robert Colwell, Ph.D.
Ex. 1005	U.S. Patent No. 5,546,547 to Bowes *et al.* ("*Bowes*")
Ex. 1006	"AT&T DSP3210 Digital Signal Processor The Multimedia Solution" Data Sheet March 1993 ("Datasheet")
Ex. 1007	Published European Patent Application EP 0626653 A1 naming Artieri, together with English translation and affidavit attesting to the accuracy of the translation ("*Artieri*")
Ex. 1008	U.S. Patent No. 6,029,217 to Arimilli *et al.* ("*Arimilli*")
Ex. 1009	R. Gove, "The MVP: A Highly-Integrated Video Compression Chip", IEEE 1994 ("*Gove*")
Ex. 1010	T. Shanley et al., "PCI System Architecture", Addison–Wesley Publ'g Co. (3rd ed. Feb. 1995) ("*Shanley*")
Ex. 1011	U.S. Patent No. 5,787,264 to Christiansen *et al.* ("*Christiansen*")
Ex. 1012	U.S. Patent No. 5,473,380 to Tahara ("*Tahara*")
Ex. 1013	Claim Construction Memorandum Opinion and Order, *Parthenon Unified Memory Architecture LLC v. Samsung Elecs. Co. Ltd. et al.*, No. 2:14-CV-00902 (E.D. Tex.)
Ex. 1014	File History of U.S. Patent No. 5,752,073
Ex. 1015	"ISO/IED 11172-2:1993 Information technology – Coding of moving pictures and associated audio for digital storage media at up to about 1,5Mbits/s- Part 2: Video;" 1st ed., August 1, 1993 ("MPEG Standard")
Ex. 1016	Texas Instruments, Inc., Houston, TX, "TMS320C8x System Level Synopsis," (1995) (Literature Ref. SPRU113B) ("TMS")
Ex. 1017	"Pentium and Pentium Pro Processors and Related Products", ISBN 1-55512-265-5

Ex. 1018	Joint Claim Construction and Prehearing Statement, *Parthenon Unified Memory Architecture LLC v. Apple Inc.*, case no. 2:15-cv-632-JRG-RSP (Feb. 16, 2016, E.D. Tex.)
Ex. 1019	VESA Unified Memory Architecture Hardware Specifications Proposal, Version 1.0p
Ex. 1020	Institution Decision, IPR2015-01501 (U.S. Patent No. 7,777,753)
Ex. 1021	Bader Declaration (including Appendix A & B)
Ex. 1022	Institution Decision, IPR2015-01502 (U.S. Patent No. 7,542,045)
Ex. 1023	Joint Claim Construction Chart, *Parthenon Unified Memory Architecture LLC v. Apple Inc.*, case no. 2:15-cv-632-JRG-RSP (April 4, 2016, E.D. Tex.)
Ex. 1024	Microprocessor Report, MPEG Choices for PCs Abound (July 31, 1995).
Ex. 1025	Declaration of Yakov Zolotorev in Support of Motion for *Pro Hac Vice* Admission
Ex. 1026	Transcript of Teleconference Hearing, IPR2016-01114, IPR2016-01118 and IPR2016-01134 (February 27, 2017)
Ex. 1027	Deposition Testimony of Mitchell A. Thornton, Ph.D., P.E. (May 22, 2017)
Ex. 1028	Reply Declaration of Robert Colwell, Ph.D., Under 37 C.F.R. §1.68

I. Introduction

The Petition and trial record provide detailed reasons why a person of skill in the art ("POSITA") would have understood *Bowes* and *Christiansen* to teach or suggest an arbiter included in the "memory interface circuit" of the decoder, as recited in claims 7-10 and 12 of the '753 Patent. None of Patent Owner's arguments overcome the express teachings of *Bowes* and *Christiansen*, and Patent Owner's Response does not provide a persuasive rebuttal of Petitioner's unpatentability showing. Accordingly, the Board should confirm unpatentability of claims 7-10 and 12 in its Final Written Decision.

The record shows that a POSITA would have understood that bus arbitration unit logic 240 in *Bowes*' MCA 200 controls whether the DSP 20 or another agent has access to shared memory via the memory bus. *See, e.g.*, Ex. 1003, p. 110. Accordingly, that arbiter logic and its associated request/grant signaling paths are "*hardware, including signaling paths to or from … an arbiter, to coordinate communication via a memory bus*," and are in the "memory interface circuit"[1] of

[1] *See* Institution Decision (Paper 7), pp. 13-14 (adopting construction of "memory interface circuit" to mean "hardware, including signaling paths to or from a competing device or an arbiter, to coordinate communication via a memory bus").

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