

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner

Case IPR2016-01114
Patent No. 7,777,753

**DECLARATION OF ROBERT COLWELL, Ph.D.,
UNDER 37 C.F.R. § 1.68
IN SUPPORT OF PETITIONER REPLY**

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I. Introduction

I, Robert Colwell, Ph.D., declare:

1. I am making this declaration at the request of Apple Inc. in the matter of the *Inter Partes* Review of U.S. Patent No. 7,777,753 (“the ’753 Patent”) to Owen *et al.* I am the Robert Colwell who has previously submitted a declaration in this proceeding (Ex. 1003). The terms of my engagement, my qualifications, professional experience and prior testimony, and the legal standards and claim constructions I am applying were set forth in my previous declarations. I offer this declaration in reply to the testimony of Prof. Thornton provided in this proceeding (Ex. 2009). In forming my opinion, I have considered the materials noted in my previous declarations in these proceedings, as well as the following additional materials:

- (1) Declaration of Mitchell A. Thornton, Ph. D., P.E. (Exhibit 2009); and
- (2) Transcript of Deposition of Mitchell A. Thornton, Ph.D., P.E., May 22, 2017 (Exhibit 1027);
- (3) Institution Decision, Paper 7;

together with any other documents specifically referenced herein.

II. Claim Construction

2. It is my understanding that in its Institution Decision, the Board has adopted Petitioner's construction of the term "memory interface circuit" to mean "*hardware, including signaling paths to or from a competing device or an arbiter, to coordinate communication via a memory bus.*" Institution Decision, Paper 7, p. 13 (emphasis added). I note that Dr. Thornton likewise states, in his declaration, that he understands that the Board has so construed the term "memory interface circuit" and that he has used the Board's construction in his analysis. Ex. 2009, ¶¶ 33-34.

3. For avoidance of doubt, I reaffirm my prior claim construction analysis of the term "memory interface circuit" (*see* Ex. 1003, ¶¶ 49-52) and apply the Board's adopted construction that a "memory interface circuit" is *hardware, including signaling paths to or from a competing device or an arbiter, to coordinate communication via a memory bus.*

4. Furthermore, I have applied the Board's adopted claim construction of the term "decoder" as *hardware and/or software that translates data streams into video or audio information.* Institution Decision, Paper 7, p. 12. The opinions I expressed in my earlier declaration (Ex. 1003) have not changed in light of the Board's adopted claim construction of "decoder."

III. Challenges #1 and #2 Mooted – Analysis Reaffirmed

5. It is my understanding that, in a separate proceeding, the Board has confirmed unpatentability of claims 1, 2 and 4 of the '753 Patent. It is also my understanding that claims 1, 2, and 4 of the '753 Patent are no longer a part of this proceeding. However, to the extent my prior analysis of claims 1, 2, and 4 is relied upon in support of the remaining challenges of claims 7-10 and 12 of the '753 Patent, I reaffirm my prior analysis of grounds #1 and #2 (*see, e.g.*, Ex. 1003, ¶¶ 89-131, 135-139, pp. 71-89, 94-95).

IV. Challenge #3: Claim 7 is Obvious over Bowes, as informed by the DSP3210 Data Sheet, in view of Artieri, and further in view of Christiansen

6. It remains my opinion that Bowes, as informed by the DSP3210 Data Sheet, and in view of Artieri and Christiansen, renders obvious claim 7. Ex. 1003, ¶ 140. It also remains my opinion that (i) one of ordinary skill in the art would have been motivated to combine the teachings of Bowes, DSP3210 Data Sheet, and Artieri (Ex. 1003, ¶ 148), and (ii) that one of ordinary skill in the art would have been motivated to further combine Christiansen for the reasons set forth in my prior declaration. Ex. 1003, ¶¶ 149-150.

7. I understand Patent Owner's argument in opposition focuses solely on the claim limitation that recites "an arbiter included in the memory interface circuit of the decoder." In particular, I understand the Patent Owner and its declarant, Dr.

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