

**IN THE UNITED STATES DISTRICT COURT  
FOR THE EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION**

**PARTHENON UNIFIED MEMORY  
ARCHITECTURE LLC,**

**Plaintiff,**

v.

**APPLE INC.,**

**Defendant.**

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**Case No. 2:15-cv-00621**

**Jury Trial Requested**

**JOINT CLAIM CONSTRUCTION CHART**

In accordance with Patent Rule 4-5(d) and the Third Amended Court’s Docket Control Order of March 7, 2016, 2015 (Dkt. 103), the parties hereby submit this Joint Claim Construction Chart. Attached as Appendix A is a chart listing the complete language of the disputed claims with disputed terms. Attached as Appendix B is a chart with the parties’ proposed constructions for the disputed terms.

Dated: April 4, 2016

Respectfully submitted,

*/s/ Marc Belloli*  
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*/s/ Michael McBride*

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**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) on April 4, 2016.

*/s/ Marc Belloli* \_\_\_\_\_

**APPENDIX B – Claim Construction Chart**

Term(s)	PUMA’s Construction	Apple’s Construction	Court’
“fast bus” ’368 patent: claim 7 ’045 patent: claim 4	“bus with a bandwidth equal to or greater than the required bandwidth to operate in real time”	Indefinite.	
a. “in real time” / “real time operation” / “operate in real time” ’789 patent: claims 1, 13  b. “the bus having a sufficient bandwidth to enable the decoder to access the memory and operate in real time when the first device simultaneously accesses the bus” ’789 patent: claim 1  c. “wherein the bus has a bandwidth of at least twice the bandwidth required for the decoder to operate in real time” ’789 patent: claim 13	“[processing] fast enough to keep up with an input data stream”	Indefinite.	

**APPENDIX B – Claim Construction Chart**

Term(s)	PUMA’s Construction	Apple’s Construction	Court’s
<p>a. “coupleable to a main memory” / “coupleable to a memory” /                      ’045 patent: claims 1, 4, 12                      ’753 patent: claim 7</p> <p>b. “coupled to a memory” “coupled to the memory” / “coupled to the main memory” / “coupled to a system memory”                      ’789 patent: claims 1                      ’368 patent: claims 1, 7, 13, 20                      ’045 patent: claims 1, 4, 5                      ’753 patent: claims 1</p> <p>c. “coupling to the memory”                      ’789 patent: claim 1</p>	<p>a. “directly or indirectly connectable to a memory/main memory”                      b. “directly or indirectly connected to a memory/main memory”                      c. “directly or indirectly connecting to a memory/main memory”</p>	<p>a. “directly or indirectly connectable to the memory/main memory/system memory using no more than one bus”                      b. “directly or indirectly connected to the memory/main memory/system memory using no more than one bus”                      c. “directly or indirectly connecting to the memory using no more than one bus”</p>	
<p>“control circuit”                      ’464 patent: claims 1,</p>	<p>No construction necessary.</p>	<p>“an electronic control device that is not a CPU or other</p>	

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