PROCEEDINGS

# DATA COMPRESSION

## CONFERENCE

March 29 - 31, 1994 • Snowbird, Utah

*Edited by*
*James A. Storer*
*Martin Cohn*

*Sponsored by the IEEE Computer Society*
*Technical Committee on Computer Communications*

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# The MVP: A Highly-Integrated Video Compression Chip

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## ABSTRACT

We introduce a new highly-integrated processing chip for performing a variety of functions, however this chip is particularly well suited for video compression algorithms. Applications include multimedia PCs, virtual reality 3D graphics, full-duplex videoconferencing, HDTV, and color hardcopy. We have architected the Multimedia Video Processor, or MVP, to provide a yet unattainable level of *performance* from a single chip, although with the *programmability* typically found in today's general-purpose computers. While advanced semiconductor design and process techniques have been used for its design, the *key* to the advantage of this component lies in optimization of the architecture for real-time video and graphics processing. This paper will analyze video compression application requirements, describe the MVP architecture, and pose its potential as a very capable solution for a wide range of markets.

## INTRODUCTION

The computer and consumer video industries are pursuing varied paths to offer cost-effective computing products which provide new forms of information and entertainment. Products are emerging from cable TV delivery of interactive digital movies to digital mobile offices. Digital compression and video processing at a reasonable cost are spurring this revolution. While algorithm developments have been important, most of the enabling advances lie in the availability of high-density memory and high-performance processing ICs. With the pending general availability of the Multimedia Video Processor, or MVP, in 1994, a yet unattained level of digital signal processing performance will be available and with all the flexibility of present day programmable computers. Standard-based video-conferencing and playback of compressed digital video and audio (using Px64, JPEG or MPEG "multi-standard" codecs systems) with a single MVP processor will be possible, as well as codecs with yet-to-be-defined algorithms like model-based compression. However, not only will the MVP support compression, it will also handle processing of high-resolution video, full-motion video processing from sources like camcorders, digital audio processing, hardcopy raster image processing, and 3D graphics, and all under software control and generation. From this wide range of functions, we calculated that several billion operations per second are required to provide video-based applications on the desktop. Current and soon to appear desktop host processors like X86, Pentium, Alpha, and MIPS do not have the computational power to meet these demands.

## KEYS TO THE MVP ARCHITECTURE

The MVP's unique architecture and computational power enables users to integrate these varied functions on a single processing component. The keys to obtaining both exceptional processing speeds and fully-programmable features with the MVP include the use of:

(1) *an efficient parallel processing architecture,*
(2) *fast pixel processing tuned to image, video, and graphics processing,*
(3) *intelligent control of image data flow throughout the architecture,*
(4) *single-chip integration without slower chip-to-chip communications.*

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