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Arimilli et al.

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[54] **QUEUED ARBITRATION MECHANISM FOR DATA PROCESSING SYSTEM**

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[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/317,006**

[22] Filed: **Oct. 3, 1994**

[51] **Int. Cl.**[7] **G06F 13/20**

[52] **U.S. Cl.** **710/107**; 710/113; 710/116

[58] **Field of Search** 395/290, 293–298, 395/287, 849, 859, 865; 710/107, 110, 113–118, 29, 39, 45

[56] **References Cited**

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[57] **ABSTRACT**

A queued arbitration mechanism transfers all queued processor bus requests to a centralized system controller/arbiter in a descriptive and pipelined manner. Transferring these descriptive and pipelined bus requests to the system controller allows the system controller to optimize the system bus utilization via prioritization of all of the requested bus operations and pipelining appropriate bus grants. Intelligent bus request information is transferred to the system controller via encoding and serialization techniques.

5 Claims, 3 Drawing Sheets

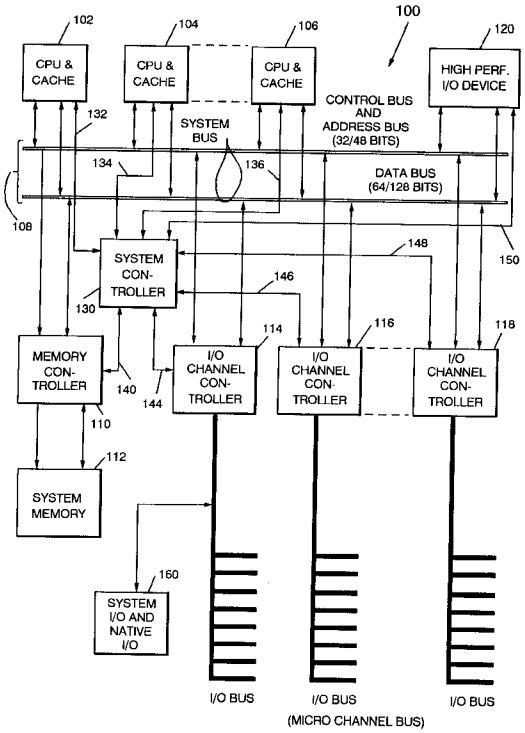


FIG. 1

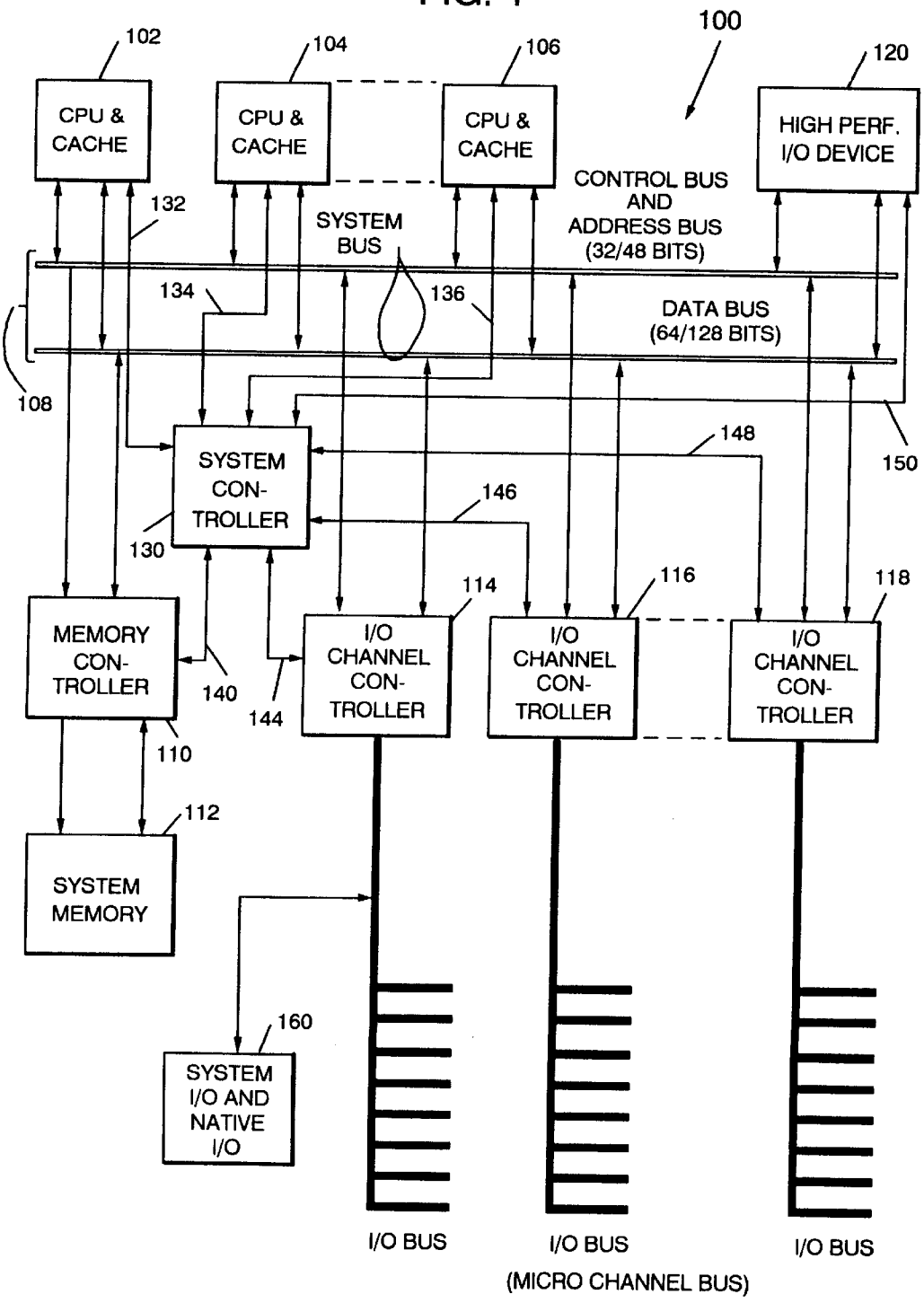


FIG. 2

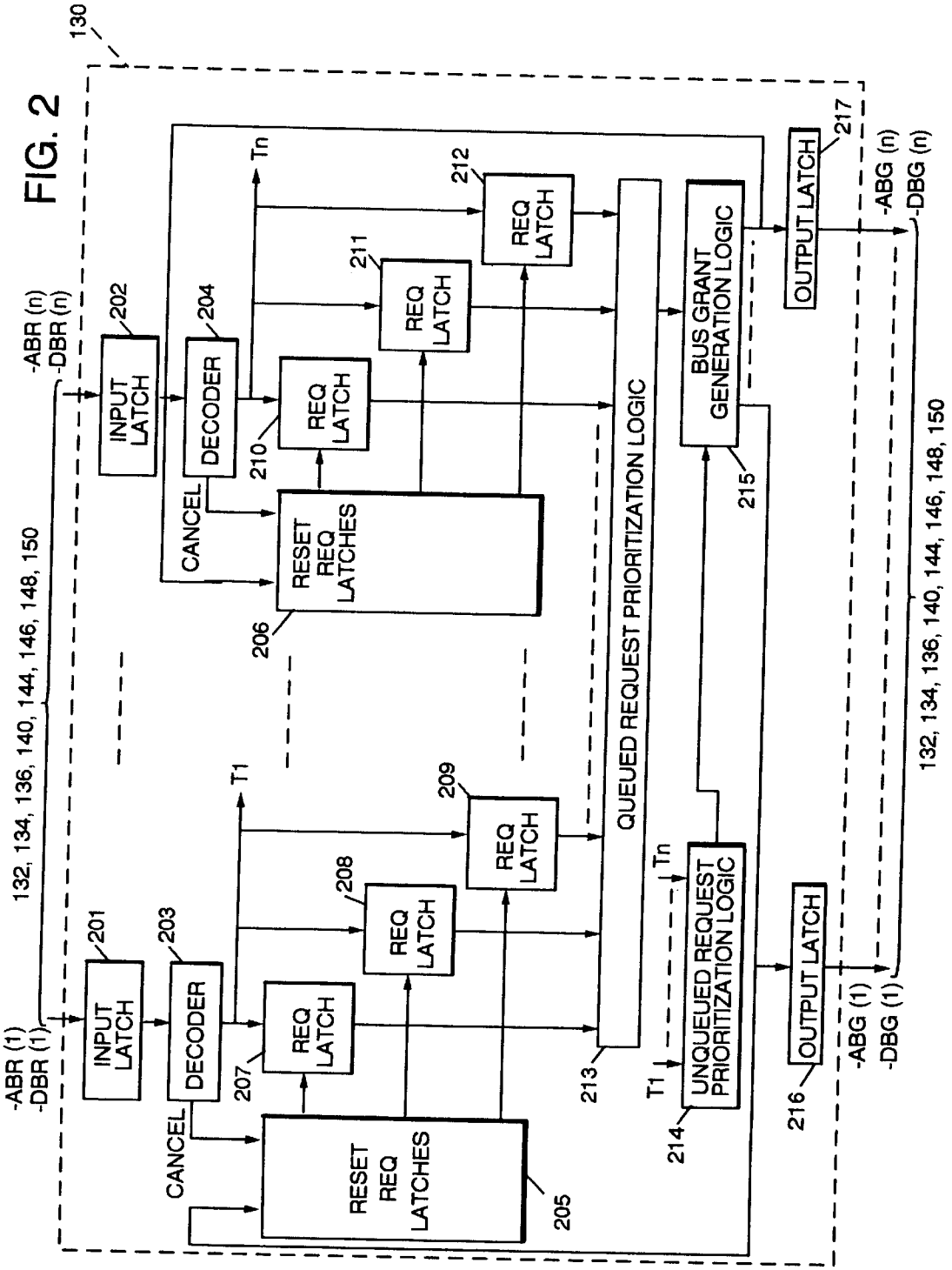
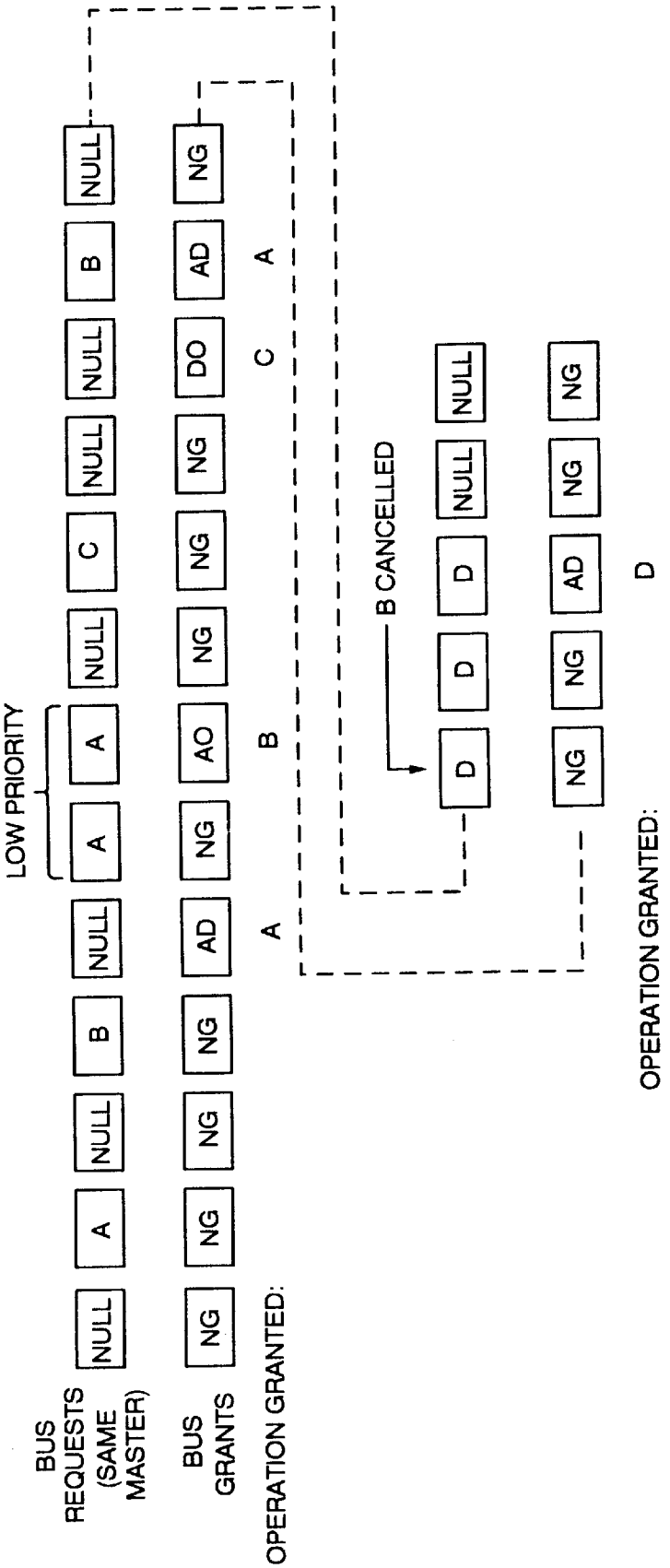


FIG. 3



QUEUED ARBITRATION MECHANISM FOR DATA PROCESSING SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

This application for patent is related to the following applications for patent filed concurrently herewith:

EFFICIENT ADDRESS TRANSFER TECHNIQUE FOR A DATA PROCESSING SYSTEM, Ser. No. 08/317,007;

DUAL LATENCY STATUS AND COHERENCY REPORTING FOR A MULTIPROCESSING SYSTEM, Ser. No. 08/316,980;

SYSTEM AND METHOD FOR DETERMINING SOURCE OF DATA IN A SYSTEM WITH INTERVENING CACHES, Ser. No. 08/317,256;

METHOD AND APPARATUS FOR REMOTE RETRY IN A DATA PROCESSING SYSTEM, Ser. No. 08/316,978;

ARRAY CLOCKING METHOD AND APPARATUS FOR INPUT/OUTPUT SUBSYSTEMS, Ser. No. 08/316,976;

DATA PROCESSING SYSTEM HAVING DEMAND BASED WRITE THROUGH CACHE WITH ENFORCED ORDERING, Ser. No. 08/316,979;

COHERENCY AND SYNCHRONIZATION MECHANISMS FOR I/O CHANNEL CONTROLLERS IN A DATA PROCESSING SYSTEM, Ser. No. 08/316,977;

ALTERNATING DATA VALID CONTROL SIGNALS FOR HIGH PERFORMANCE DATA TRANSFER, Ser. No. 08/326,190;

LOW LATENCY ERROR REPORTING FOR HIGH PERFORMANCE BUS, Ser. No. 08/326,203.

Each of such cross-referenced applications are hereby incorporated by reference into this Application as though fully set forth herein.

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to data processing systems and, in particular, to a system and method for intelligent communication of bus requests and bus grants within a data processing system.

BACKGROUND OF THE INVENTION

Conventional data processing systems, especially multiprocessor systems, allocate access to the shared system bus coupling the various bus devices to system memory through a mechanism whereby individual bus devices each control access to the system bus. Typically, each bus device will queue it's individual bus requests for various operations internally. Then, each bus device makes the determination of which of the various operations it wishes to perform on the system bus by sending the appropriate corresponding bus request to the system controller. Thus, each individual bus device determines internally which of its bus requests has higher priority. The system controller is then required to arbitrate between the received bus requests from the individual bus devices.

One disadvantage of this arbitration mechanism is that a portion of the decision process for accessing the various resources coupled to the system bus is delegated to each of the bus devices. As a result, the system controller is only able to view a portion of all of the various requests from the individual bus devices, since each of the individual bus devices retains and queues a significant number of bus requests. Thus, there is a need in the art for a more efficient arbitration mechanism for granting access to the system bus.

SUMMARY OF THE INVENTION

It is an object of the present invention to centralize the decision-making process for granting access to the system bus. In an attainment of this object, the present invention provides a mechanism of transferring all of the queued bus requests from the individual bus devices to the system controller, which has a centralized knowledge of the availability of all of the system resources coupled to the system bus.

The system controller samples the bus devices' requests on a cycle-by-cycle basis. The requests are encoded, which allows each of the bus devices to precisely communicate to the system controller each of their internally "queued" operations. Quickly transferring these "descriptive and pipelined" bus requests from each of the bus devices to a centralized control point, allows the system controller to "optimize" the system bus utilization by prioritizing all of the requested bus operations and pipelining the appropriate bus grants.

One advantage of the present invention is that it provides an ability to transfer "intelligent" bus request information from each bus device to the system controller, and provides the ability to transfer multiple packets of bus requests information (via encoding and serialization techniques).

Another advantage of the present invention is that the bus requests are compact and can be issued in a pipelined manner and that bus grants may be pipelined to either the same bus device or different bus devices.

Yet another advantage of the present invention is that it supports latch-to-latch or non-latch-to-latch implementations. Those skilled in the art will appreciate the benefit of accommodating both implementations. (Latch-to-latch implementations allow higher system bus clock rates, while non-latch-to-latch implementations provides lower system bus latencies.)

Yet still another advantage of the present invention is that the queuing of descriptive bus requests allows the system controller to efficiently control, distribute, and allocate system bus resources.

And, yet still another advantage of the present invention is that the system controller may resolve system level multiprocessor problems such as deadlocks and livelocks. Unlike traditional arbitration techniques, the present invention bus does not require bus devices to adhere to any arbitration "fairness" protocols.

Another advantage of the present invention is that the bus devices may support speculative bus requests and the system controller may support speculative bus grants.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention.

BRIEF DESCRIPTION OF THE DRAWING

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates a block diagram of a data processing system in accordance with the present invention;

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