This Power of Attorney copy is intended for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson E. Owen et al.
Application No.	:	08/702,910
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY
Examiner	:	Glenn Gossage
Art Unit	:	2751
Docket No.	:	96-S-12 (850063.553)
Date	:	April 12, 1999

Assistant Commissioner for Patents
Washington, DC 20231

APPOINTMENT OF ASSOCIATE POWER OF ATTORNEY

Sir:

I, Lisa K. Jorgenson, attorney of record in the above-identified application, appoint as associate attorneys David V. Carlson, Reg. No. 31,153; Michael J. Donohue, Registration No. 35,859, Kevin S. Ross, Reg. No. 42,116; Dale C. Barr, Reg. No. 40,498; Kevin S. Costanza, Reg. No. 37,801, Brian L. Johnson, Reg. No. 40,033, Paul F. Rusyn, Reg. No. 42,118, Dennis M. de Guzman, Reg. No. 41,702; E. Russell Tarleton, Reg. No. 31,800, John M. Wechkin, Reg. No. 42,216; Robert D. McCutcheon, Reg. No. 38,717; and Theodore E. Galanthay, Reg. No. 24,122.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	April 15, 2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FEE DEFICIENCY AUTHORIZATION FORM

Commissioner for Patents:

Applicants hereby authorize the Director to charge any deficiencies in fees due by way of the enclosed papers only under 37 CFR 1.16 and 1.17 to Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

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1370876_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	David V. Carlson/daniel davis
Attorney Docket Number:	96-S-012C4 (850063.553C4)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1090**

Electronic Acknowledgement Receipt

EFS ID:	5161400
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/daniel davis
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	15-APR-2009
Filing Date:	
Time Stamp:	18:11:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

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Payment Type	Deposit Account
Payment was successfully received in RAM	$1090
RAM confirmation Number	5236
Deposit Account	191090
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Application Data Sheet	553C4_ADS.pdf	968095 233bf336847d04802bf9e064cc9dfb7b375aac99	no	5
Warnings:					
Information:					
2		553C4_app.pdf	1397024 d487a2efaea29c7d50e27fdb7e1eac88fa07b000	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	24	
	Claims		25	29	
	Abstract		30	30	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	553C4_drawings.pdf	709474 1572b3a1ba1240e3b2ccd3c643b4b08240e80184	no	6
Warnings:					
Information:					
4	Oath or Declaration filed	553C4_dec.pdf	99642 b70e3251b944005e20a60018c7bda8760469b400	no	4
Warnings:					
Information:					
5	Power of Attorney	553C4_POA.pdf	36613 e08248a98610c794db46d1c32c89d32ae7945011	no	1
Warnings:					
Information:					
6	Miscellaneous Incoming Letter	553C4_FDA.pdf	48563 33be232ad8e2875c8feae87f56925eea21a3b0ea	no	1
Warnings:					
Information:					
7	Fee Worksheet (PTO-06)	fee-info.pdf	33491 7cb46c2e41112f638da898caeb497dd55bb7bdac	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3220805		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C4 (850063.553C4)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jefferson	Eugene	Owen	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Citizenship under 37 CFR 1.41(b) i: US

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Postal Code	94303	Country i	US

Applicant 3 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
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Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Tucker	State/Province	GA	Country of Residence i	US

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C4 (850063.553C4)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY	

Citizenship under 37 CFR 1.41(b) [i]	FR		
Mailing Address of Applicant:			
Address 1	2820 Livsey Court		
Address 2			
City	Tucker	**State/Province**	GA
Postal Code	30084	**Country**[i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	30423		
Email Address	davec.docketing@seedip.com	Add Email	Remove Email

Application Information:

Title of the Invention	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY		
Attorney Docket Number	96-S-012C4 (850063.553C4)	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C4 (850063.553C4)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY	

Customer Number	30423

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	11/956165	2007-12-13

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/956165	Continuation of	10/174918	2002-06-19	7321368	2008-01-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10/174918	Continuation of	09/539729	2000-03-30	6427194	2002-07-30

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
09/539729	Continuation of	08/702910	1996-08-26	6058459	2000-05-02

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	STMicroelectronics, Inc.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	96-S-012C4 (850063.553C4)
	Application Number	
Title of Invention	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY	

Mailing Address Information:			
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Address 2			
City	Carrollton	**State/Province**	TX
Country [i]	US	Postal Code	75006
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/David V. Carlson/			Date (YYYY-MM-DD)	2009-04-15
First Name	David	Last Name	Carlson	Registration Number	31153

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Cross-reference to Related Applications

This application is a continuation of U.S. Patent Application No. 11/956,165, filed December 13, 2007, and allowed April 6, 2009; which is a continuation of U.S. Patent No. 7,321,368, issued January 22, 2008; which is a continuation of U.S. Patent No. 6,427,194, issued July 30, 2002; which is a continuation of U.S. Patent No. 6,058,459, issued May 2, 2000. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.

Cross-reference to Other Related Applications

The present application contains some text and drawings in common with U.S. Patent Application No. 08/702,911, filed August 26, 1996, and issued September 22, 1998 as U.S. Patent No. 5,812,789, entitled: "VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE" by Raul Z. Diaz and Jefferson E. Owen, which had the same effective filing date and ownership as the present application, and to that extent is related to the present application, which is incorporated herein by reference.

Background

The present invention relates to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.

The size of a digital representation of uncompressed video images is dependent on the resolution and color depth of the image. A movie composed of a

sequence of such images, and the audio signals that go along with them, quickly become large enough so that, uncompressed, such a movie typically cannot fit entirely onto a conventional recording medium such as a Compact Disc (CD). It is now also typically prohibitively expensive to transmit such a movie uncompressed.

It is therefore advantageous to compress video and audio sequences before they are transmitted or stored. A great deal of effort is being expended to develop systems to compress these sequences. Several coding standards currently in use are based on the discrete cosine transfer algorithm including MPEG-1, MPEG-2, H.261, and H.263. (MPEG stands for "Motion Picture Expert Group", a committee of the International Organization for Standardization, also known as the International Standards Organization, or ISO.) The MPEG-1, MPEG-2, H.261, and H.263 standards are decompression protocols that describe how an encoded bitstream is to be decoded. The encoding can be done in any manner, as long as the resulting bitstream complies with the standard.

Video and/or audio compression devices (hereinafter "encoders") are used to encode the video and/or audio sequence before it is transmitted or stored. The resulting bitstream is decoded by a video and/or audio decompression device (hereinafter "decoder") before the video and/or audio sequence is displayed. However, a bitstream can only be decoded by a decoder if it complies with the standard used by the decoder. To be able to decode the bitstream on a large number of systems, it is advantageous to encode the video and/or audio sequences in compliance with a well accepted decompression standard. The MPEG standards are currently well accepted standards for one-way communication. H-261, and H.263 are currently well accepted standards for video telephony.

Once decoded, the images can be displayed on an electronic system dedicated to displaying video and audio, such as television or a Digital Video Disk (DVD) player, or on electronic systems where image display is just one feature of the system, such as a computer. A decoder needs to be added to these systems to allow them to display compressed sequences, such as received images and associated audio, or ones taken from a storage device. An encoder needs to be added to allow the system to compress video

and/or audio sequences, to be transmitted or stored. Both need to be added for two-way communication such as video telephony.

A typical decoder, such as an MPEG decoder 10 shown in Figure 1a, contains video decoding circuit 12, audio decoding circuit 14, a microcontroller 16, and a memory interface 18. The decoder can also contain other circuitry depending on the electronic system in which the decoder is designed to operate. For example, when the decoder is designed to operate in a typical television, it will also contain an on-screen display (OSD) circuit.

Figure 1b shows a better decoder architecture, used in the STi3520 and STi3520A MPEG Audio/MPEG-2 Video Integrated Decoder manufactured by ST Microelectronics, Inc., Carrollton, Texas. The decoder has a register interface 20 instead of a microcontroller. The register interface 20 is coupled to an external microcontroller 24. The use of a register interface 20 makes it possible to tailor the decoder 10 to the specific hardware with which the decoder 10 interfaces, or to change its operation without having to replace the decoder by just reprogramming the register interface. It also allows the user to replace the microcontroller 24, to upgrade or tailor the microcontroller 24 to a specific use, by just replacing the microcontroller and reprogramming the register interface 20, without having to replace the decoder 10.

The memory interface 18 is coupled to a memory 22. A typical MPEG decoder 10 requires 16 Mbits of memory to operate in the Main Profile at Main Level mode (MP at ML). This typically means that the decoder requires a 2Mbyte memory. Memory 22 is dedicated to the MPEG decoder 10 and increases the price of adding a decoder 10 to the electronic system. In current technology, the cost of this additional dedicated memory 22 can be a significant percentage of the cost of the decoder.

An encoder also requires a memory interface 18 and dedicated memory. Adding the encoder to an electronic system again increases the price of the system by both the price of the encoder and its dedicated memory.

Figure 1c shows a conventional decoder inserted in a computer architecture. A conventional computer generally includes a peripheral bus 170 to connect several

necessary or optional components, such as a hard disk, a screen, etc. These peripherals are connected to bus 170 via interfaces (e.g., a display adapter 120 for the screen) which are provided directly on the computer's motherboard or on removable boards.

A Central Processing Unit (CPU) 152 communicates with bus 170 through an interface circuit 146 enabling a main memory 168 of the computer to be shared between CPU 152 and peripherals of bus 170 which might require it.

The decoder 10 is connected as a master peripheral to bus 170, that is, it generates data transfers on this bus without involving CPU 152. The decoder receives coded or compressed data CD from a source peripheral 122, such as a hard disk or a compact disk read only memory (CD-ROM), and supplies decoded images to display adapter 120. Recent display adapters make it possible to directly process the "YUV" (luminance and chrominance) image data normally supplied by a decoder, while a display adapter is normally designed to process "RGB" (red, green, blue) image information supplied by CPU 152.

Display adapter 120 uses memory 12-1 for storing the image under display, which comes from the CPU 152 or from the decoder 10. A conventional decoder 10 also uses dedicated memory 22. This memory is typically divided into three image areas or buffers M1 to M3 and a buffer CDB where the compressed data are stored before they are processed. The three image buffers respectively contain an image under decoding and two previously decoded images.

Figure 1d illustrates the use of buffers M1 to M3 in the decoding of a sequence of images I0, P1, B2, B3, P4, B5, B6, P7. I stands for a so-called "intra" image, whose compressed data directly corresponds to the image. P stands for a so-called "predicted" image, the reconstruction of which uses pixel blocks (or macroblocks) of a previously decoded image. Finally, B stands for a so-called "bidirectional" image, the reconstruction of which uses macroblocks of two previously decoded images. The intra and predicted images are likely to be used to reconstruct subsequent predicted and bidirectional images, while the bidirectional images are not used again.

Images I0 and P1 are respectively stored in buffers M1 and M2 during their decoding. The filling and the emptying of a buffer in Fig. 1d are indicated by oblique lines. The decoding of image P1 uses macroblocks of image I0. Image I0, stored in buffer M1, is displayed during the decoding of image B2, this image B2 being stored in buffer M3. The decoding of image B2 uses macroblocks of images I0 and P1. Image B2 is displayed immediately after image I0. As the locations of buffer M3 become empty, they are filled by decoded information of image B3. The decoding of image B3 also uses macroblocks of images I0 and P1. Once image B3 is decoded, it is displayed immediately, while image P4 is decoded by using macroblocks of image P1. Image P4 is written over image I0 in buffer M1 since image I0 will no longer be used to decode subsequent images. After image B3, image P1 is displayed while buffer M3 receives image B5 under decoding. The decoding of image B5 uses macroblocks of images P1 and P4. Image P1 is kept in buffer M2 until the decoding of image B6, which also uses macroblocks of images P1 and P4, and so on.

Referring again to Figure 1c, when any component needs access to the main memory 168 either to read from or write to the main memory 168, it generates a request which is placed on the bus 170. When the request is a write, the data to be written is also placed on the bus 170. The request is processed and the data is then either written to or read from the main memory 168. When data is read from the main memory 168, the data is now placed on the bus and goes to the component that requested the read.

There are typically many components in the computer systems that may require access to the main memory 168, and they are typically all coupled to the same bus 170, or possibly to several buses if there are not enough connectors on one bus to accommodate all of the peripherals. However, the addition of each bus is very expensive. Each request is typically processed according to a priority system. The priority system is typically based on the priority given to the device and the order in which the requests are received. Typically, the priority system is set up so no device monopolizes the bus, starving all of the other devices. Good practice suggest that no device on the bus require more than approximately 50% of the bus's bandwidth.

The minimum bandwidth required for the decoder 10 can be calculated based on the characteristics and desired operation of the decoder. These characteristics include the standard with which the bitstream is encoded to comply, whether the decoder is to operate in real time, to what extent frames are dropped, and how the images are stored. Additionally, the latency of the bus that couples the decoder to the memory should be considered.

If the decoder does not operate in real time, the decoded movie would stop periodically between images until the decoder can get access to the memory to process the next image. The movie may stop and wait quite often between images.

To reduce the minimum required bandwidth and still operate in real time, the decoder 10 may need to drop frames. If the decoder 10 regularly does not decode every frame, then it may not need to stop between images. However, this produces very poor continuity in the images. This is problematic with an image encoded to the MPEG-1 or MPEG-2 standards, or any standard that uses temporal compression. In temporal (interpicture) compression, some of the images are decoded based on previous images and some based on previous and future images. Dropping an image on which the decoding of other images is based is unacceptable, and will result in many poor or even completely unrecognizable images.

The computer can also contain both a decoder and encoder to allow for video telephony, as described above. In this case, not operating in real time would mean that the length of time between the occurrence of an event such as speaking at one end of the conversation until the event is displayed at the other end of the conversation--is increased by the time both the encoder and then the decoder must wait to get access to the bus and the main memory. Not being able to operate in real time means that there would be gaps in the conversation until the equipment can catch up. This increases the time needed to have a video conference, and makes the conference uncomfortable for the participants.

One widely used solution to allow a component in a computer system to operate in real time is to give the component its own dedicated memory. Thus, as shown in Figure 1c, the decoder 10 can be given its own dedicated memory 22, with a dedicated bus

26 to connect the decoder 10 to its memory 22. The dedicated memory 22 significantly increases the cost of adding a decoder 10 to the computer. A disadvantage of a computer equipped with a conventional decoder is that it has a non-negligible amount of memory which is unused most of the time.

Indeed, memory 22 of the decoder is only used when decoded images are being viewed on the computer screen or need to be encoded, which amounts to only a fraction of the time spent on a computer. This memory--inaccessible to the other peripherals or to the CPU--has a size of 512 Kbytes in an MPEG-1 decoder and Mbytes in an MPEG-2 decoder. Further, this memory is oversized, since it is obtained by using currently available memory components.

Summary of the Invention

The present application discloses an electronic system that contains a first device and video and/or audio decompression and/or compression device capable of operating in real time. Both the first device and the video and/or audio decompression and/or compression device require access to a memory. The video and/or audio decompression and/or compression device shares the memory with the first device. The two devices are coupled to the memory through a fast bus having a bandwidth of at least the minimum bandwidth needed for the video and/or audio decompression and/or compression device to operate in real time.

In one preferred embodiment of the invention the two devices share an arbiter. The arbiter and Direct Memory Access (DMA) engines of the video and/or audio decompression and/or compression device and of the first device are configured to arbitrate between the two devices when one of them is requesting access to the memory. This allows both the video and/or audio decompression and/or compression device and the first device to share the memory.

When the video and/or audio decompression and/or compression device used in an electronic system, such as a computer, already containing a device that has a memory the video and/or audio decompression and/or compression device can share that

memory, and the memory of the video and/or audio decompression and/or compression device can be eliminated. Eliminating the memory greatly reduces the cost of adding the video and/or audio decompression and/or compression device to the electronic system.

The decoder memory is part of the main memory of the computer. The computer should have a fast bus (such as a memory bus, a PCI -"Peripheral Component Interconnect" - bus, a VLB -"VESA (Video Electronics Standards Association) Local Bus", or an AGP - "Advanced Graphics Port" - bus, or any bus having a bandwidth sufficient to allow the system to operate in real time) which will accept high image rates between the decoder, the main memory and the display adapter.

According to an embodiment of the present invention, the decoder directly supplies a display adapter of the screen with an image under decoding which is not used to decode a subsequent image.

According to an embodiment of the present invention, the main memory stores predicted images which are obtained from a single preceding image and also stores intra images which are not obtained from a preceding image. The images directly supplied to the display adapter are bidirectional images obtained from two preceding intra or predicted images.

According to an embodiment of the present invention, the decoder is disposed on the computer's motherboard.

An advantage of the present invention is the significant cost reduction due to the fact that the video and/or audio decompression and/or compression device does not need its own dedicated memory but can share a memory with another device and still operate in real time.

A further advantage of the present invention is that the video and/or audio decompression and/or compression device can share the memory with a device without being integrated into this device, allowing the first device to be a standard device with some adjustments made to its memory interface.

Other advantages and objects of the invention will be apparent to those of ordinary skill in the art having reference to the following specification together with the drawings.

Brief Description of the Drawings

Figure 1a and 1b are electrical diagrams, in block form, of prior art decoders.

Figure 1c is an electrical diagram, in block form, of a computer architecture including a conventional decoder.

Figure 1d, illustrates the use of image buffers in the processing of an image sequence by a conventional MPEG decoder.

Figure 2 is an electrical diagram, in block form, of an electronic system containing a device having a memory interface and an encoder and decoder.

Figure 3 is an electrical diagram, in block form, of a computer system containing a core logic chipset designed for the CPU to share a memory interface with an encoder and/or decoder according to one embodiment of the present invention.

Figure 4 is an electrical diagram, in block form, of a computer architecture including an encoder and/or decoder according to another embodiment of the present invention.

Figure 5 illustrates the use of image buffers in the processing of an image sequence by an MPEG decoder according to the present invention.

Figure 6 is an electrical diagram, in block form, of an embodiment of an MPEG decoder architecture according to the present invention.

Figure 7 is an electrical diagram, in block form, of a computer system containing a graphics accelerator designed to share a memory interface with an encoder and/or decoder.

Detailed Description of the Preferred Embodiment

Figure 2 shows an electronic system 40 containing a first device 42 having access to a memory 50, and a decoder 44 and encoder 46, having access to the same memory 50. First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50, and either contains or is coupled to a memory interface. In the preferred embodiment of the invention, electronic system 40 contains a first device 42, a decoder 44, an encoder 46, and a memory 50, although, either the decoder 44 or encoder 46 can be used in the video and/or audio decompression and/or compression device 80 without the other. For ease of reference, a video and/or audio decompression and/or compression device 80 will hereinafter be referred to as decoder/encoder 80. The decoder/encoder 80 may be a single device, or a cell in an integrated circuit; or it may be two separate devices, or cells in an integrated circuit. In the preferred embodiment of the invention, the first device 42, decoder/encoder 80, are on one integrated circuit, however, they can be on separate integrated circuits in any combination.

The decoder 44 includes a video decoding circuit 12 and an audio decoding circuit 14, both coupled to a register interface 20. The decoder 44 can be either a video and audio decoder, just a video encoder, or just an audio decoder. If the decoder 44 is just a video decoder, it does not contain the audio decoding circuitry 14. The audio decoding can be performed by a separate audio coder-decoder (codec) coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 80 is in a system containing a processor and is coupled to the processor, the audio decoding is performed in software. This frees up space on the die without causing significant delay in the decoding. If the audio decoding is performed in software, the processor should preferably operate at a speed to allow the audio decoding to be performed in real time without starving other components of the system that may need to utilize the processor. For example, current software to perform AC-3 audio decoding takes up approximately 40% of the bandwidth of a 133 MHz Pentium. The encoder 46 includes a video encoding circuit 62 and an audio encoding circuit 64, both coupled to a register interface 20. The encoder 46 can be either a video and audio encoder, just a video encoder, or just an audio

encoder. If the encoder 46 is just a video encoder, it does not contain the audio encoding circuitry 64. The audio encoding can be performed by a separate audio codec coupled to the first device 42, or through software. In the preferred embodiment of the invention, when the decoder/encoder 80 is in a system containing a processor and is coupled to the processor, the audio encoding is performed in software, presenting the same advantages of freeing up space on the die without causing significant delay in the encoding, as in the case of decoding discussed above. The register interfaces 20 of the decoder 44 and encoder 46 are coupled to a processor.

The decoder 44 and encoder 46 are coupled to the Direct Memory Access (DMA) engine 52. The decoder and encoder can be coupled to the same DMA engine as shown in Figure 2, or each can have its own DMA engine, or share a DMA engine with another device. When the decoder/encoder 80 are two separate devices or cells, decoder 44 and encoder 46 can still be coupled to one DMA engine 52. When the decoder/encoder is one device or is one cell on an integrated circuit, the DMA engine 52 can be part of the decoder/encoder 80, as shown in Figure 2. The DMA engine 52 is coupled to the arbiter 82 of the memory interface 76. The arbiter 82 is preferably monolithically integrated into the memory interface 76 of the decoder or into the memory interface 72 of the first device. However, the arbiter 82 can be a separate cell or device coupled to the memory interfaces 76, 72 of the decoder/encoder 80 and the first device 42. The arbiter 82 is also coupled to the refresh logic 58 and the memory controller 56 of the device into which it is monolithically integrated. The refresh logic 58, like the arbiter 82, can be monolithically integrated into the memory interface 76 of the decoder, into the memory interface 72 of the first device, or can be a separate cell or device coupled to the arbiter 82.

The first device 42 also contains a memory interface 72 and a DMA engine 60. The DMA engine 60 of the first device 42 is coupled to the memory interface 72 of the first device 72.

Both memory interfaces 72 and 76 are coupled to a memory 50. The memory controllers 56 are the control logic that generates the address the memory interfaces 72, 76 access in the memory 50 and the timing of the burst cycles.

In current technology, memory 50 is typically a Dynamic Random Access Memory (DRAM). However, other types of memory can be used. The refresh logic 58 is needed to refresh the DRAM. However, as is known in the art, if a different memory is used, the refresh logic 58 may not be needed and can be eliminated.

The decoder/encoder 80 is coupled to the memory 50 through devices, typically a bus 70, that have a bandwidth greater than the bandwidth required for the decoder/encoder 80 to operate in real time. The minimum bandwidth required for the decoder/encoder 80 can be calculated based on the characteristics and desired operation of the decoder, including the standard with which the bitstream is encoded to comply, whether the decoder/encoder 80 is to operate in real time, to what extent frames are dropped, and which images are stored. Additionally, the latency of the bus 70 that couples the decoder/encoder 80 to the memory 50 should be considered.

A goal is to have the decoder/encoder 80 operate in real time without dropping so many frames that it becomes noticeable to the movie viewer. To operate in real time the decoder/encoder 80 should decode and/or encode images fast enough so that any delay in decoding and/or encoding cannot be detected by a human viewer. This means that the decoder/encoder 80 has a required bandwidth that allows the decoder/encoder 80 to operate fast enough to decode the entire image in the time between screen refreshes, typically 1/30 of a second, with the human viewer unable to detect any delay in the decoding and/ or encoding. To operate in real time, the required bandwidth should be lower than the bandwidth of the bus. In order not to starve the other components on the bus, i.e., deny these components access to the memory for an amount of time that would interfere with their operation, this required bandwidth should be less than the entire bandwidth of the bus. Therefore, a fast bus 70 should be used. A fast bus 70 is any bus whose bandwidth is equal to or greater than the required bandwidth. In current technology, there are busses, including the Industry Standard Architecture (ISA) bus, whose bandwidth is significantly below the bandwidth required for this.

In the preferred embodiment of the invention, the decoder/encoder 80 is coupled to the memory 50 through a fast bus 70 that has a bandwidth of at least the

bandwidth required for the decoder/encoder 80 to operate in real time, a threshold bandwidth. Preferably the fast bus 70 has a bandwidth of at least approximately twice the bandwidth required for the decoder/encoder 80 to operate in real time. In the preferred embodiment, the fast bus 70 is a memory bus, however, any bus having the required bandwidth can be used.

The decoder/encoder 80 only requires access to the memory during operation. Therefore, when there is no need to decode or encode, the first device 42 and any other devices sharing the memory 50 have exclusive access to the memory and can use the entire bandwidth of the fast bus 70.

In the preferred embodiment, even during decoding and encoding, the decoder/encoder 80 does not always use the entire required bandwidth. Since the fast bus 70 has a bandwidth a little less than twice the size of the required bandwidth, the decoder/encoder 80 uses at most 60% of the bandwidth of the fast bus 70.

The required bandwidth is determined based on the size and resolution of the image and the type of frame (I, P, or B). In the preferred embodiment the decoder/encoder typically will be using less than 40% of the bandwidth of the fast bus 70. This frees up the remaining bandwidth to be used by the other devices with which the decoder/encoder 80 is sharing the memory 50.

The decoder/encoder 80 can decode a bitstream formatted according to any one or a combination of standards. In the preferred embodiment of the invention, the decoder/encoder 80 is a multi-standard decoder/encoder capable of decoding and encoding sequences formatted to comply with several well accepted standards. This allows the decoder/encoder 80 to be able to decode a large number of video and/or audio sequences. The choices of which standards the decoder/encoder 80 is capable of decoding bitstreams formatted to, and of encoding sequences to comply with, are based on the desired cost, efficiency, and application of the decoder/encoder 80.

In the preferred embodiment, these standards are capable of both intrapicture compression and interpicture compression. In intrapicture compression the redundancy within the image is eliminated. In interpicture compression the redundancy between two

images is eliminated, and only the difference information is transferred. This requires the decoder/encoder 80 to have access to the previous or future image that contains information needed to decode or encode the current image. These previous and/or future images need to be stored and then used to decode the current image. This is one of the reasons the decoder/encoder 80 requires access to the memory, and requires a large bandwidth. The MPEG-1 and MPEG-2 standards allow for decoding based on both previous images and/or future images. Therefore, for a decoder/encoder 80 capable of operating in real time to be able to comply with the MPEG-1 and MPEG-2 standards, it should be able to access two images--a previous and a future image--fast enough to decode the current image in the 1/30 of a second between screen refreshes.

An MPEG environment is asymmetrical; there are much fewer encoders than decoders. The encoders are very difficult and expensive to manufacture, and the decoders are comparatively easy and cheap. This encourages many more decoders than encoders, with the encoders in centralized locations, and decoders available such that every end user can have a decoder. Therefore, there are many receivers but few transmitters.

For video telephony and teleconferencing, each end user must be able to both receive and transmit. H.261, and H.263 are currently well accepted standards for video telephony. An encoder that can encode sequences to comply with the H.261 and H.263 standards is less complicated, having a lower resolution and lower frame rate than an encoder that complies with the MPEG-1 or MPEG-2 standards, possibly making the quality of the decoded images somewhat lower than those from an encoder that complies with the MPEG-1 or MPEG-2 standards. Since it should be inexpensive and operate in real time, such an encoder is also less efficient than an encoder to encode sequences to comply with the MPEG-1 or MPEG-2 standards, meaning that the compression factor--which is the ratio between the source data rate and the encoded bitstream data rate--of such an encoder is lower for a given image quality than the compression factor of an MPEG encoder. However, because such an encoder is less complicated, it is much cheaper and faster than an encoder capable of complying with the MPEG-1 and/or MPEG-2 standards. This makes

video telephony possible, since both a long delay in encoding the signal and a cost that is prohibitively expensive for many users is unacceptable in video telephony.

In the preferred embodiment, the decoder/encoder 80 is capable of decoding a bitstream formatted to comply with the MPEG-1, MPEG-2, H.261, and H.263 standards, and encoding a sequence to produce a bitstream to comply with the H.261, and H.263 standards. This allows the decoder/encoder 80 to be able to be used for video telephony. The encoding to comply with the H.261 and H.263 standards but not the MPEG-1 and MPEG-2 standards balances the desire to reduce the cost of transmission and storage by encoding to produce the highest compression factor and the desire to keep cost low enough to be able to mass market the device.

Figure 3 shows one embodiment of a computer where the decoder/encoder 80 is sharing a main memory 168 with a core logic chipset 190. The core logic chipset 190 can be any core logic chipset known in the art. In the embodiment shown in Figure 3, the core logic chipset 190 is a Peripheral Component Interconnect (PCI) core logic chipset 190, which contains a PCI core logic device 158, the processor interface 154, a memory interface 72, and bus interface 156 for any system busses 170 to which it is coupled. The core logic chipset 190 can also contain an Accelerated Graphics Port (AGP) 160 if a graphics accelerator 200 is present in the computer, and an Enhanced Integrated Device Electronics (EIDE) interface 186. The core logic chipset 190 is coupled to a processor (Central Processing Unit or CPU) 152, peripherals such as a hard disk drive 164 and a Digital Versatile Disk (DVD) CD-ROM 166, a bus such as a PCI bus 170, the arbiter 82, and the main memory 168.

In this embodiment, the main memory 168 is the memory 50 to which the memory interfaces 72 and 76 are coupled. The main memory 168 is coupled to the memory interfaces 72 and 76 through a memory bus 167. In current technology the memory bus 167, which corresponds to the fast bus 70 for coupling the core logic chipset to the memory, is capable of having a bandwidth of approximately 400 Mbytes/s. This bandwidth is at least twice the bandwidth required for an optimized decoder/encoder 80, allowing the decoder/encoder 80 to operate in real time.

The core logic chipset 190 can also be coupled to cache memory 162 and a graphics accelerator 200 if one is present in the computer. The PCI bus 170 is also coupled to the graphics accelerator 200 and to other components, such as a Local-Area Network (LAN) controller 172. The graphics accelerator 200 is coupled to a display 182 and a frame buffer 184. The graphics accelerator can also be coupled to an audio codec 180 for decoding and/or encoding audio signals.

Figure 4 shows another embodiment of a computer where the decoder/encoder 80 is sharing the main memory 168. In this embodiment, the main memory 168 corresponds to the shared memory 50 of Figure 2. In Figure 4, the decoder/encoder 80 according to the present invention is connected as a peripheral to a conventional computer equipped with a fast peripheral bus 170, for example, a PCI bus, although the bus can be VESA Local Bus (VLB), an Accelerated Graphics Port (AGP) bus, or any bus having the required bandwidth. In this embodiment, the fast peripheral bus 170 corresponds to the fast bus 70. As shown, the decoder/encoder 80 does not have a dedicated memory, but utilizes a region 22' of the main memory 168 of the computer.

Region 22' includes a Compressed Data Buffer (CDB), into which image source 122 writes the compressed image data, and two image buffers M1 and M2 associated with intra or predicted images. As will be seen hereafter, a buffer associated with bidirectional images is not required, these bidirectional images B being directly supplied to display adapter 120 as they are being decoded.

Thus, in the system of Figure 4, compressed or coded data CD are transferred from image source 122 to buffer CDB of memory 168. These same compressed data are then transferred to the decoder/encoder 80 which, if they correspond to intra or predicted images, retransmits them in decoded form to buffers Ml and M2 of memory 168. In the case where the compressed data correspond to bidirectional images, the decoder/encoder 80 decodes these data and directly supplies display adapter 120 with the decoded data. The display adapter then supplies these data to a display device such as a screen. The intra or predicted images stored in buffers M1 and M2 are transferred to

display adapter 120 at the appropriate time and are used in the decoding of subsequent predicted or bidirectional images.

With a decoder/encoder 80 according to the invention, the rates on peripheral bus 170 are particularly high, which is why a fast bus is needed. However, the rate required is substantially decreased due to the bidirectional images not being stored in main memory 168, but being directly sent to display adapter 120. According to the invention, the bandwidth used on a PCI bus is approximately 20% with an MPEG-1 decoder/encoder and approximately 80% with an MPEG-2 decoder/encoder. These bandwidths correspond to worst case situations. The bandwidth in typical operation can be lower.

Of course, the storage capacity of the main memory 168 available for other uses is reduced during the operation of the decoder/encoder 80 because the decoder/encoder 80 is using the memory region 22'. However, in this embodiment the size of region 22' is decreased from the size of the dedicated memory 22 used in the prior art (Figures 1a and 1c) by one image buffer. The memory region 22' is also only occupied while viewing video sequences. When the decoder/encoder is no longer used, memory region 22' can be freed at once for the other tasks.

The modifications to be made on the computer to use a decoder/encoder according to the invention primarily involve software changes and are within the capabilities of those skilled in the art, who will find the necessary information in the various standards relating to the computer. For the computer to be able to use its peripherals, it conventionally executes background programs called peripheral drivers, which translate specific addresses issued by the CPU or a master peripheral (such as the decoder/encoder 80) into addresses adapted to the variable configuration of the computer.

For example, a peripheral driver associated with the decoder/encoder according to the invention translates the fixed addresses issued by the decoder/encoder 80 to have access to its image memory into addresses corresponding to the physical location of region 22', this region being likely to be variably assigned by the operating system according to the occupancy of memory 168. Similarly, this peripheral driver answers

requests issued by image source 122 to supply compressed data by transferring these data into buffer CDB of region 22'.

In an alternative embodiment the third image buffer M3 (Figure 1c) remains in the memory region 22' used for the decoder/encoder 80. A conventional decoder/encoder should be able to be used in several applications, especially to supply television images. In the case of television, the images are supplied in interlaced form, that is, all the odd lines of an image are supplied prior to the even lines. An MPEG decoder generally reconstructs the images in progressive form, that is, it supplies the image lines consecutively. The third image buffer M3 is then necessary to store the bidirectional images in the order of arrival of the lines (in progressive form) and then reread this image in interlaced form. The third image buffer M3 may also be needed if there is a delay between when the images are decoded and when they can be viewed, requiring the images to be stored.

Figure 5 illustrates the use of memory region 22' in the decoding according to the invention of sequence 10, P1, B2, B3, P4, B5, B6, P7. Image I0 is stored in buffer M1 during its decoding. As the decoding and the storage in buffer M2 of image P1 begins, image I0 is displayed. The macroblocks used to decode image P1 are fetched from buffer M1. Images B2 and B3 are displayed as they are being decoded, the macroblocks used for their decoding being fetched from buffers M1 and M2. Image P1 is displayed while image P4 is being decoded and stored in buffer M1 in the place of image I0. Image P1 is kept in buffer M2 until image B6 is decoded and displayed, and so on.

Figure 6 shows an architecture of an MPEG decoder according to the invention. Like any conventional MPEG decoder, this decoder includes a Variable Length Decoder (VLD) receiving compressed data from a First-In, First-Out (FIFO) memory 30. The VLD is followed by a Run-Level Decoder (RLD), an inverse quantization circuit Q-1 and an inverse discrete cosine transform circuit DCT-1. The output of circuit DCT-1 is supplied to a first input of an adder 32, a second input of which receives macroblocks of a previously decoded image via a filter 34 and a FIFO 35. The decoded image data are

supplied by the output of adder 32 and via a FIFO 37. FIFO 30 is supplied with compressed data from bus 10 via an interface circuit PCI I/F 39.

A decoder according to the invention differs from a conventional decoder in that the interface circuit 39 also connects FIFOs 35 and 37 to bus 170. A memory controller 41 calculates and supplies through bus 170 the addresses corresponding to the various exchanges required.

The management of the addresses of buffers M1 and M2 is similar to that performed by the memory controller of a conventional decoder, since these addresses are, according to the invention, translated according to the physical location of these buffers in memory 168 by a peripheral driver. Moreover, the memory controller of a decoder/encoder 80 according to the preferred embodiment of the invention is substantially simplified due to the absence of the third image buffer M3. The memory controller of a conventional decoder has to manage this buffer in a specific way to avoid a bidirectional image under decoding being written over a bidirectional image under display.

Figure 7 shows a computer where the decoder/encoder 80 is sharing a frame buffer 184 with a graphics accelerator 200. The graphics accelerator 200 can be any graphics accelerator known in the art. In the embodiment shown in Figure 7, the graphics accelerator 200 contains a Two-Dimensional (2D) accelerator 204, a Three-Dimensional (3D) accelerator 206, a Digital to Analog Converter (DAC) 202, a memory interface 72, and bus interface 210 for any system busses 170 to which it is coupled. The graphics accelerator 200 can also contain an audio compressor/decompressor 208, here an AC-3 decoder. The graphics accelerator 200 is coupled to a display 182, and a frame buffer 184.

In this embodiment, the frame buffer 184 is the memory 50 to which the memory interfaces 72 and 76 are coupled. The frame buffer 184 is coupled to the memory interfaces 72 and 76 through a memory bus 185. In this embodiment, memory bus 185 corresponds to the fast bus 70. In current technology the memory bus 185 for coupling a graphics accelerator to a memory is capable of having a bandwidth of up to 400 Mbytes/s. This bandwidth is more that twice the bandwidth required for an optimized decoder/encoder 80. This allows the decoder/encoder 80 to operate in real time.

The graphics accelerator 200 can also be coupled to an audio codec 180 for decoding and/or encoding audio signals. The PCI bus 170 is also coupled to a chipset 190, and to other components, such as a LAN controller 172. In the present embodiment the chipset is a PCI chipset, although it can be any conventional chipset. The chipset 190 is coupled to a processor (CPU) 152, main memory 168, and a PCI bridge 192. The PCI bridge bridges between the PCI bus 170 and the ISA bus 198. The ISA bus 198 is coupled to peripherals, such as a modem 199 and to an EIDE interface 186, which is coupled to other peripherals, such as a hard disk drive 164 and a DVD CD-ROM 166, although, if the peripherals are compatible to the PCI bus the EIDE interface 186 can be integrated into the PCI chipset 190 and the peripherals 164 and 166 can be coupled directly to the PCI chipset, eliminating the PCI bridge 192 and the ISA bus 198.

Referring to Figure 2, the operation of the arbiter 82 during a memory request will now be described. During operation the decoder/encoder 80, the first device 42, and the refresh logic 58, if it is present, request access to the memory through the arbiter 82. There may also be other devices that request access to the memory 50 through this arbiter. The arbiter 82 determines which of the devices gets access to the memory 50. The decoder/encoder gets access to the memory in the first time interval, and the first device gets access to the memory in the second time interval. The Direct Memory Access (DMA) engine 52 of the decoder/encoder 80 determines the priority of the decoder/encoder 80 for access to the memory 50 and of the burst length when the decoder/encoder 80 has access to the memory. The DMA engine 60 of the first device determines its priority for access to the memory 50 and the burst length when the first device 42 has access to the memory.

The decoder/encoder 80 or one of the other devices generates a request to access the memory 50. The request will be transferred to the arbiter 82. The state of the arbiter 82 is determined. The arbiter typically has three states. The first state is idle when there is no device accessing the memory and there are no requests to access the memory. The second state is busy when there is a device accessing the memory and there is no other

request to access the memory. The third state is queue when there is a device accessing the memory and there is another request to access the memory.

It is also determined if two requests are issued simultaneously. This can be performed either before or after determining the state of the arbiter. Access to the memory is determined according to the following chart.

Arbiter state	Simultaneous requests	Action
Idle	Yes	One of the requests gets access to the memory based on the priority scheme, and the other request is queued.
Busy	Yes	Both requests are queued in an order based on the priority scheme.
Queue	Yes	Both requests are queued in an order based on the priority scheme.
Idle	No	The device gets access to the memory.
Busy	No	The request is queued.
Queue	No	The requests are queued in an order based on the priority scheme.

The priority scheme can be any priority scheme that ensures that the decoder/encoder 80 gets access to the memory 50 often enough and for enough of a burst length to operate properly, yet not starve the other devices sharing the memory. The priority of the first device, device priority, and the priority of the decoder/encoder 80, decoder priority, are determined by the priority scheme. This can be accomplished in several ways.

To operate in real time, the decoder/encoder 80 has to decode an entire image in time to be able to display it the next time the screen is refreshed, which is typically every 1/30 of a second. The decoder/encoder 80 should get access to the memory to store and retrieve parts of this and/or of past and/or future images, depending on the

decoding standard being used, often enough and for long enough burst lengths to be able to decode the entire image in the 1/30 of a second between screen refreshes.

There are many ways to do this. One way is to make the burst length of the first device and any other device like the screen refresh that shares the memory and memory interface (hereinafter sharing device) have short burst lengths, and to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Another way is to preempt the sharing device if its burst length exceeds a burst length threshold and again to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. Preferably, when the preemption is used the sharing device would be preempted when its burst length exceeds 16 words. A third way is to limit the bandwidth available to the sharing devices. This way the decoder/encoder 80 always has enough bandwidth to operate in real time. Preferably the bandwidth of the sharing devices is limited only when the decoder/encoder 80 is operating. In the preferred embodiment a memory queue such as a FIFO in the decoder/encoder 80 generates an error signal when it falls below a data threshold. The error is sent to the CPU 152 and the CPU 152 can either shut down the system, drop an image frame or resume the decoding/encoding process.

There are also many ways to make sure that the same device is not the next device to get access to the memory when other devices have been waiting for a long time. This both ensures that the decoder/encoder 80 gets access to the memory 50 often enough, yet does not starve the other devices sharing the memory. One way to do this is to disallow back-to-back requests. Another is to have shifting priority, where a particular request starts with a lower priority when first made, and the priority increases with the length of time the request is in the queue, eventually reaching a priority above all of the other requests. In the preferred embodiment, the decoder/encoder 80 has a one-clock cycle delay between requests to allow a sharing device to generate a request between the decoder/encoder requests.

In the preferred embodiment of the invention, the burst length of the decoder/encoder is relatively short, approximately four to seventeen words. This allows the

graphics accelerator more frequent access to the memory to ensure that the display is not disturbed by the sharing of the memory interface 48 and memory 50 when the decoder/encoder shares a memory with the graphics accelerator 200.

An electronic system 40, shown in Figure 2, containing the first device 42 coupled to the memory 50, the decoder/encoder 80 coupled to the same memory 50, where the decoder/encoder 80 shares the memory 50 with the first device 42 provides several advantages. Referring to Figure 2 and Figure 1b simultaneously, the decoder 44 and encoder 46 according to the preferred embodiment of the invention do not each need their own dedicated memory 22 that was necessary in the prior art for the decoder/encoder to operate in real time, resulting in significant reduction in the cost of the device. Allowing the decoder/encoder 80 to share the memory 50 with a first device 42 and to allow the decoder/encoder 80 to access the memory 50 through a fast bus 70 having a bandwidth of a least the bandwidth threshold permits the decoder/encoder to operate in real time. This reduces stops between images and the dropping of a significant number of frames to a point where both are practically eliminated. This produces better images and eliminates any discontinuities and delays present in the prior art.

Additionally, in the embodiment of the invention where the fast bus 70 is a system bus to which the decoder/encoder 80 is already coupled, the number of pins of the decoder/encoder 80 is considerably smaller than that of a conventional decoder. The decoder/encoder according to the invention only requires the signals of the peripheral bus 170 (49 signals for the PCI bus), while a conventional decoder further includes an interface with its dedicated memory 22, which is typically an external memory.

Thus, decoding in a computer can be performed according to the invention by means of a low-cost (due to the small number of pins) single integrated circuit, without the additional, costly, dedicated memory 22. This single integrated circuit can be directly placed on the computer motherboard for a low additional cost. 0f course, the decoder/encoder according to the invention can be mounted, as is conventional, on an extension board to be connected to a bus.

A further advantage of the present invention is that the video and/or audio decompression and/or compression device can share memory with the first device without being integrated into the first device. This allows the first device to be a standard device with some adjustments made to its memory interface.

Further background on compression can be found in: International Organization for Standards, *Information Technology - Coding of Moving Pictures and Associated Audio for Digital Storage Media at up to About 1.5 Mbits/S*, Parts 1-6, International Organization for Standards; International Standards Organization, *Information Technology - Generic Coding of Moving Pictures and Associated Audio Information*, Parts 1-4, International Organization for Standards; Datasheet "STi3500A" Datasheet of SGS-THOMSON Microelectronics; STi3500A - Advanced Information for an MPEG Audio/ MPEG-2 Video Integrated Decoder" (June 1995); Watkinson, John, *Compression in Video and Audio*, Focal Press, 1995; Minoli, Daniel, *Video Dialtone Technology*, McGraw-Hill, Inc., 1995. Further background on computer architecture can be found in Anderson, Don and Tom Shanley, *ISA System Architecture*, 3rd ed., John Swindle ed., MindShare Inc., Addison-Wesley Publishing Co., 1995. All of the above references are incorporated herein by reference.

While the invention has been specifically, described with reference to several preferred embodiments, it will be understood by those of ordinary skill in the prior art having reference to the current specification and drawings that various modifications may be made and various alternatives are possible therein without departing from the spirit and scope of the invention. For example: Although the memory is described as DRAM, other types of memories including read-only memories, Static Random Access Memories (SRAMs), or FIFOs may be used without departing from the scope of the invention.

Any conventional decoder including a decoder complying to the MPEG-1, MPEG-2, H.261, or H.261 standards, or any combination of them, or any other conventional standard can be used as the decoder/encoder.

We claim:

1. An electronic system comprising:

a bus;

a main memory coupled to the bus having stored therein data corresponding to video images;

a video circuit coupled to the bus, the video circuit configured to receive data from the main memory corresponding to a current video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device, the current video image to be displayed adapted to be stored in the main memory;

a processor coupled to the main memory, the processor for storing non-image data in the main memory and retrieving non-image data from the main memory; and

an arbiter circuit coupled to the processor and to the video circuit, the arbiter circuit configured to receive requests for access to the main memory from the video circuit and the processor and to control access to the main memory by:

providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state;

queuing a request for access to the main memory when the arbiter circuit is in a busy state; and

queuing a request for access to the main memory in an order based on a priority of the request and a priority of each of one or more other requests for access to the main memory that are currently queued when the arbiter circuit is in a queue state.

2. The electronic system of claim 1, wherein the data corresponding to video images that is stored in the main memory further includes data corresponding to video images to be decoded and data corresponding to video images that have been

previously decoded, and wherein the video circuit is further configured to receive data from the main memory corresponding to at least one previously decoded video image.

3. The electronic system of claim 1, wherein the video circuit directly supplies a display adapter with an image under decoding which is not used to decode a subsequent image.

4. The electronic system of claim 1, wherein the arbiter circuit is further configured to control access to the main memory by preempting access control for a request received from the processor and providing access control for a request received from the video circuit when the request received from the processor exceeds a burst length threshold.

5. The electronic system of claim 1, wherein the video circuit is further configured to have a one-clock cycle delay between issuing requests for access to the main memory.

6. The electronic system of claim 1, wherein the video circuit and the arbiter circuit are integrated into a computer motherboard.

7. An electronic circuit for use with a memory, comprising:

a bus coupleable to a memory;

a decoder coupled to the bus for receiving encoded video images and for outputting data for displaying decoded video images on a display device, the decoder configured to receive data from the memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being output for storing in the memory, the decoder having a memory interface circuit;

a central processing unit coupled to the bus for accessing the memory, the central processing unit having a memory interface circuit; and

an arbiter included in the memory interface circuit of the decoder and coupled to the memory interface circuit of the central processing unit, the arbiter configured to control access to the memory by determining a priority for requests to access the memory, each of the requests received from one of the decoder and the central processing unit, and providing access to the memory based on the determined priorities of the requests.

8. The electronic circuit of claim 7, wherein the arbiter is further configured, when simultaneous requests for access to the memory are received from the decoder and the central processing unit, to:

provide access to the memory for at least one of the simultaneous requests based on the priority of each of the simultaneous requests when the arbiter is in an idle state;

queue the simultaneous requests in an order based on the priority of each of the simultaneous requests when the arbiter is in a busy state; and

queue the simultaneous requests in an order based on the priority of each of the simultaneous requests and the priority of each of one or more other requests that are currently queued when the arbiter is in a queue state.

9. The electronic system of claim 7, wherein the arbiter is further configured to preempt access for a request received from the central processing unit and to provide access control for a request received from the encoder when the request received from the central processing unit exceeds a burst length threshold.

10. The electronic system of claim 7, wherein the arbiter is further configured to increase the priority associated with each of the requests according to an amount of time the request has been waiting for access to the memory.

11. The electronic system of claim 7, wherein the arbiter and the decoder are integrated into a computer motherboard.

12. The electronic system of claim 7, wherein the arbiter and the decoder are integrated into a single chip.

13. A method, comprising:

storing in a shared memory data corresponding to video images and other data that does not correspond to video images;

receiving in a video decoder data corresponding to a compressed current video image and data corresponding to at least one previously decoded video image from the shared memory, and outputting from the video decoder decoded video data corresponding to the compressed current video image; and

for each of multiple requests for access to the shared memory received from the video decoder and one or more other devices,

providing access to the shared memory for the request when the shared memory is not being accessed and no other requests to access the shared memory are currently pending;

queuing the request when the shared memory is being accessed; and

queuing the request in an order based on a priority of the request and a priority of each of one or more other requests that are currently pending when the shared memory is being accessed and the one or more other requests are currently pending.

14. The method of claim 13 wherein at least some of the multiple requests for access to the shared memory include simultaneous requests received from the video decoder and at least one of the one or more other devices, the method further comprising:

providing access to the shared memory for at least one of the simultaneous requests based on a priority of each of the simultaneous requests when the shared memory

is not being accessed and no other requests to access the shared memory are currently pending;

queuing the simultaneous requests in an order based on the priority of each of the simultaneous requests when the shared memory is being accessed; and

queuing the simultaneous requests in an order based on the priority of each of the simultaneous requests and the priority of each of one or more other requests that are currently pending when the shared memory is being accessed and the one or more other requests are currently pending.

15. The method of claim 13, further comprising preempting access to the shared memory for a request received from the one or more other devices and providing access to the shared memory for a request received from the video encoder when the request received from the one or more other devices exceeds a burst length threshold.

16. The method of claim 13, further comprising increasing the priority associated with each of any currently pending requests according to an amount of time the request has been pending.

17. The method of claim 13, wherein the one or more other devices are one or more of a processor, a core logic chipset, and a graphics accelerator.

ABSTRACT OF THE DISCLOSURE

An electronic system, an integrated circuit and a method for display are disclosed. The electronic system contains a first device, a memory and a video/audio compression/decompression device such as a decoder/encoder. The electronic system is configured to allow the first device and the video/audio compression/decompression device to share the memory. The electronic system may be included in a computer in which case the memory is a main memory. Memory access is accomplished by one or more memory interfaces, direct coupling of the memory to a bus, or direct coupling of the first device and decoder/encoder to a bus. An arbiter selectively provides access for the first device and/or the decoder/encoder to the memory based on priority. The arbiter may be monolithically integrated into a memory interface. The decoder may be a video decoder configured to comply with the MPEG-2 standard. The memory may store predicted images obtained from a preceding image.

This Declaration copy is intended for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

Please send all correspondence to:

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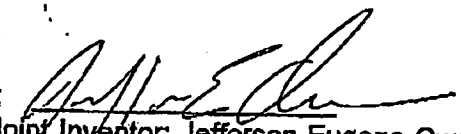
(214) 466-7414

Inventor's Signature: 
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Full Name of First Joint Inventor: Jefferson Eugene Owen
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SCORE Placeholder Sheet for IFW Content

Application Number: 12424389 Document Date: 4/15/2009

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Form Revision Date: February 8, 2006

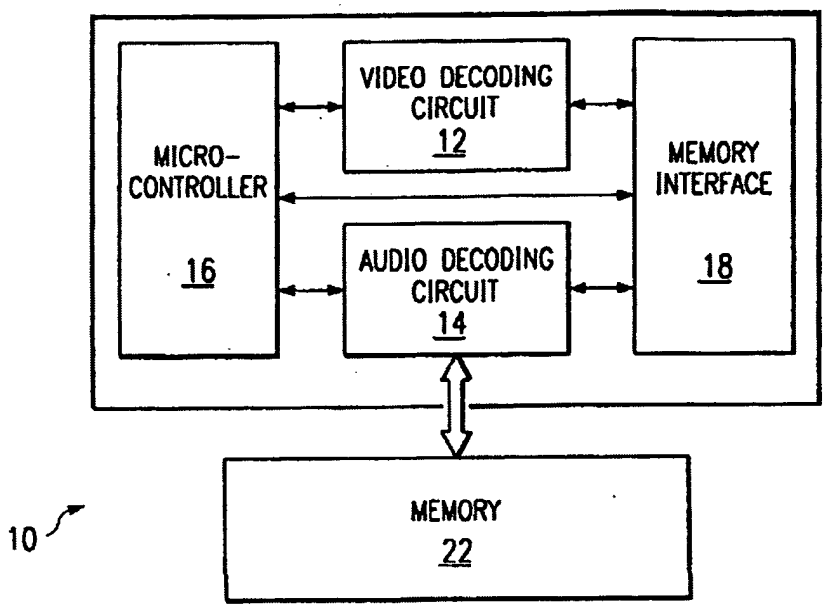


Fig. 1a
(Prior Art)

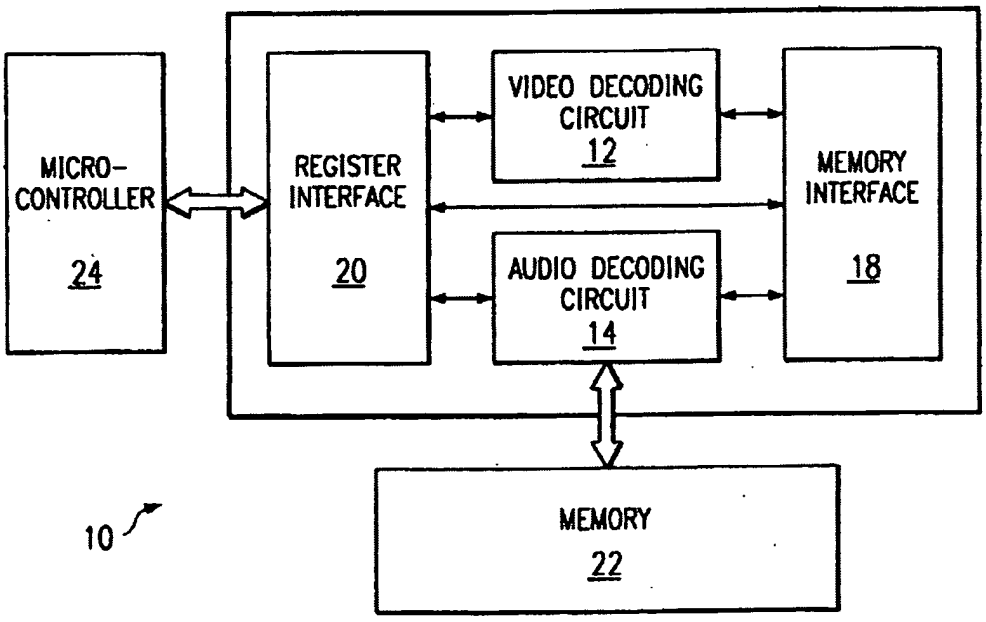


Fig. 1b
(Prior Art)

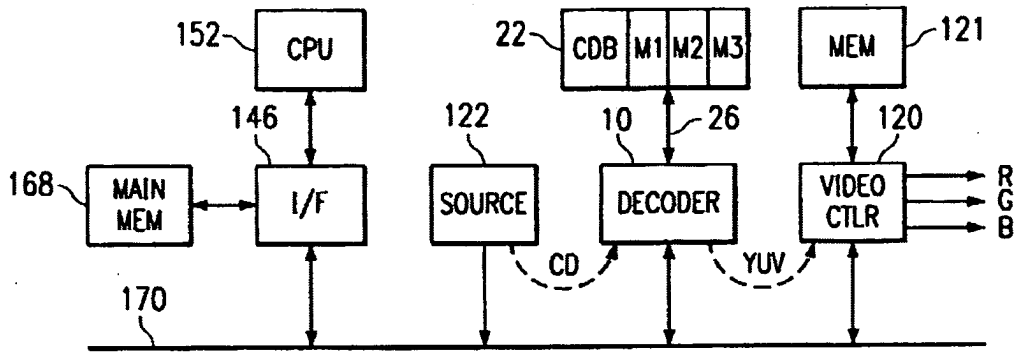


Fig. 1c
(Prior Art)

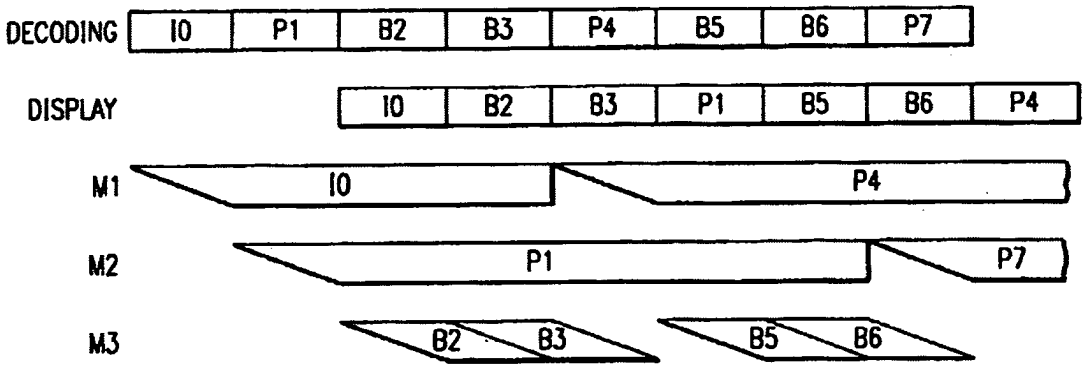
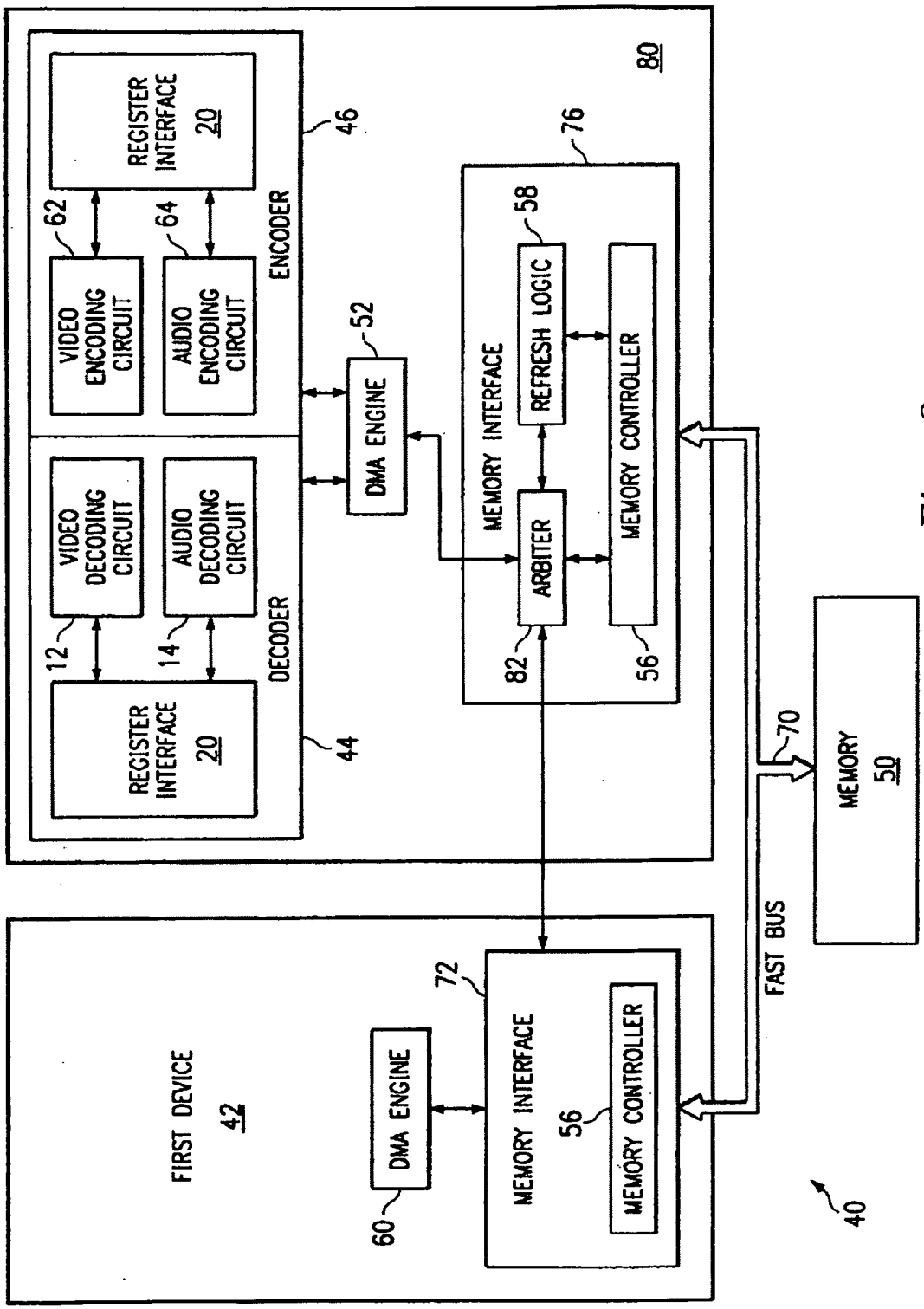


Fig. 1d
(Prior Art)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64
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AUDIO ENCODING CIRCUIT
52
DMA ENGINE
DECODER
44
VIDEO DECODING CIRCUIT
AUDIO DECODING CIRCUIT
12
14
REGISTER INTERFACE 20
MEMORY INTERFACE
76
58
REFRESH LOGIC
ARBITER
82
MEMORY CONTROLLER
56
70
MEMORY 50
FAST BUS
FIRST DEVICE 42
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DMA ENGINE
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MEMORY INTERFACE
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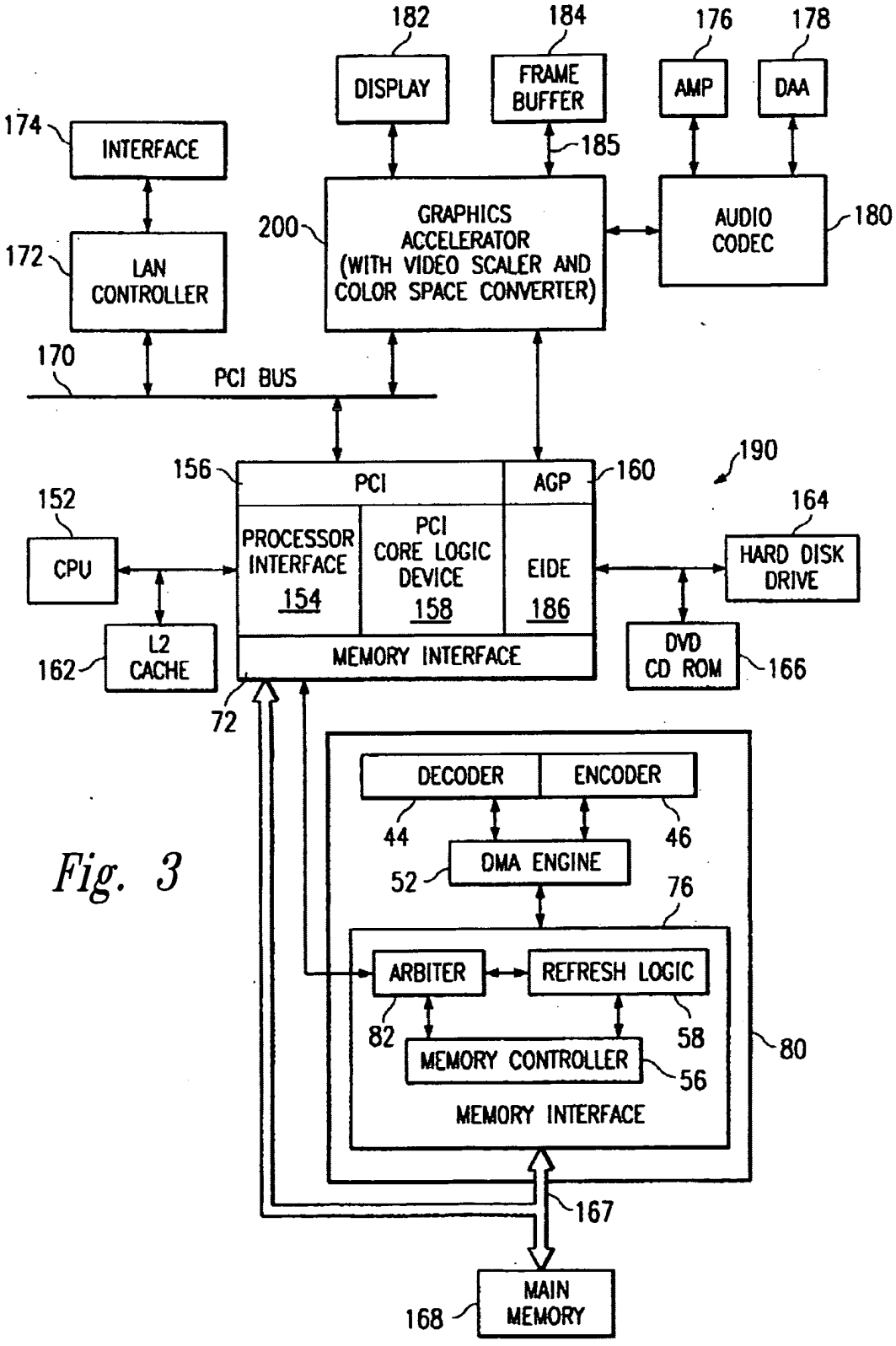
MEMORY CONTROLLER
40

Fig. 2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DISPLAY
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FRAME BUFFER
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AMP
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DAA
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INTERFACE
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200
GRAPHICS ACCELERATOR (WITH VIDEO SCALER AND COLOR SPACE CONVERTER)
AUDIO CODEC
180
172
LAN CONTROLLER
170
PCI BUS
190
156
PCI
AGP
160
152
PROCESSOR INTERFACE 154
PCI CORE LOGIC DEVICE 158
EIDE 186
164
CPU
HARD DISK DRIVE
L2 CACHE
162
MEMORY INTERFACE
DVD CD ROM
166
72
DECODER
ENCODER
44
46
DMA ENGINE
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MEMORY INTERFACE
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MAIN MEMORY
168

Fig. 3

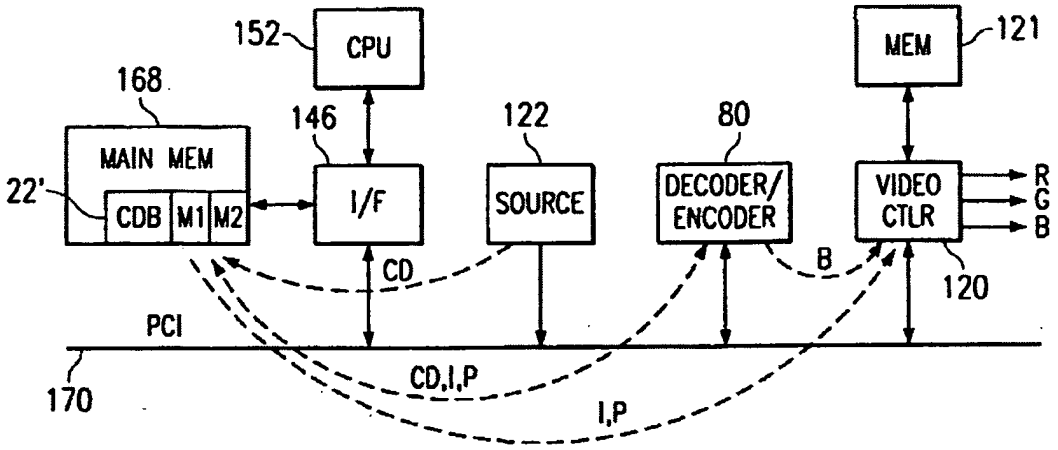


Fig. 4

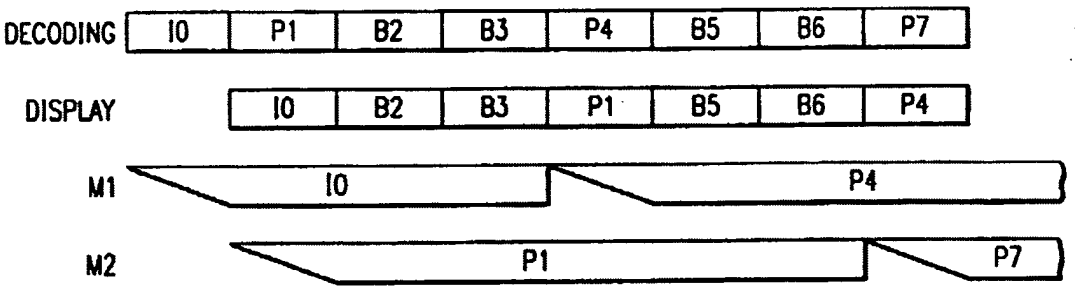


Fig. 5

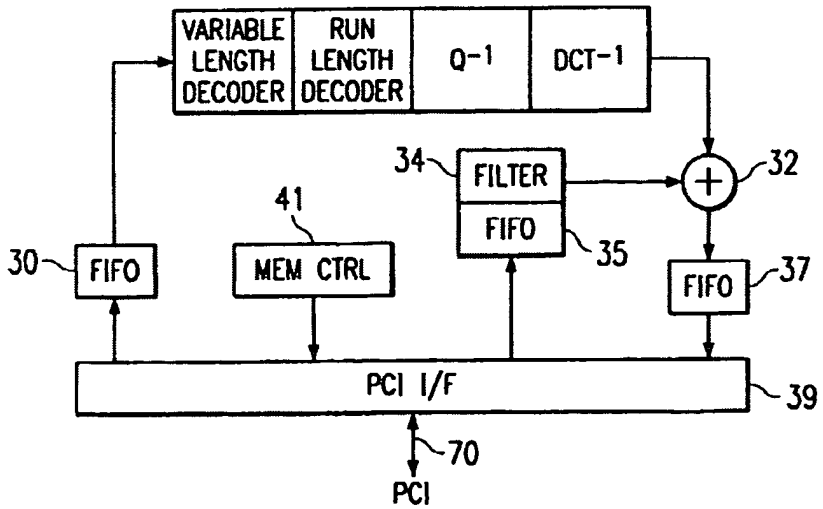
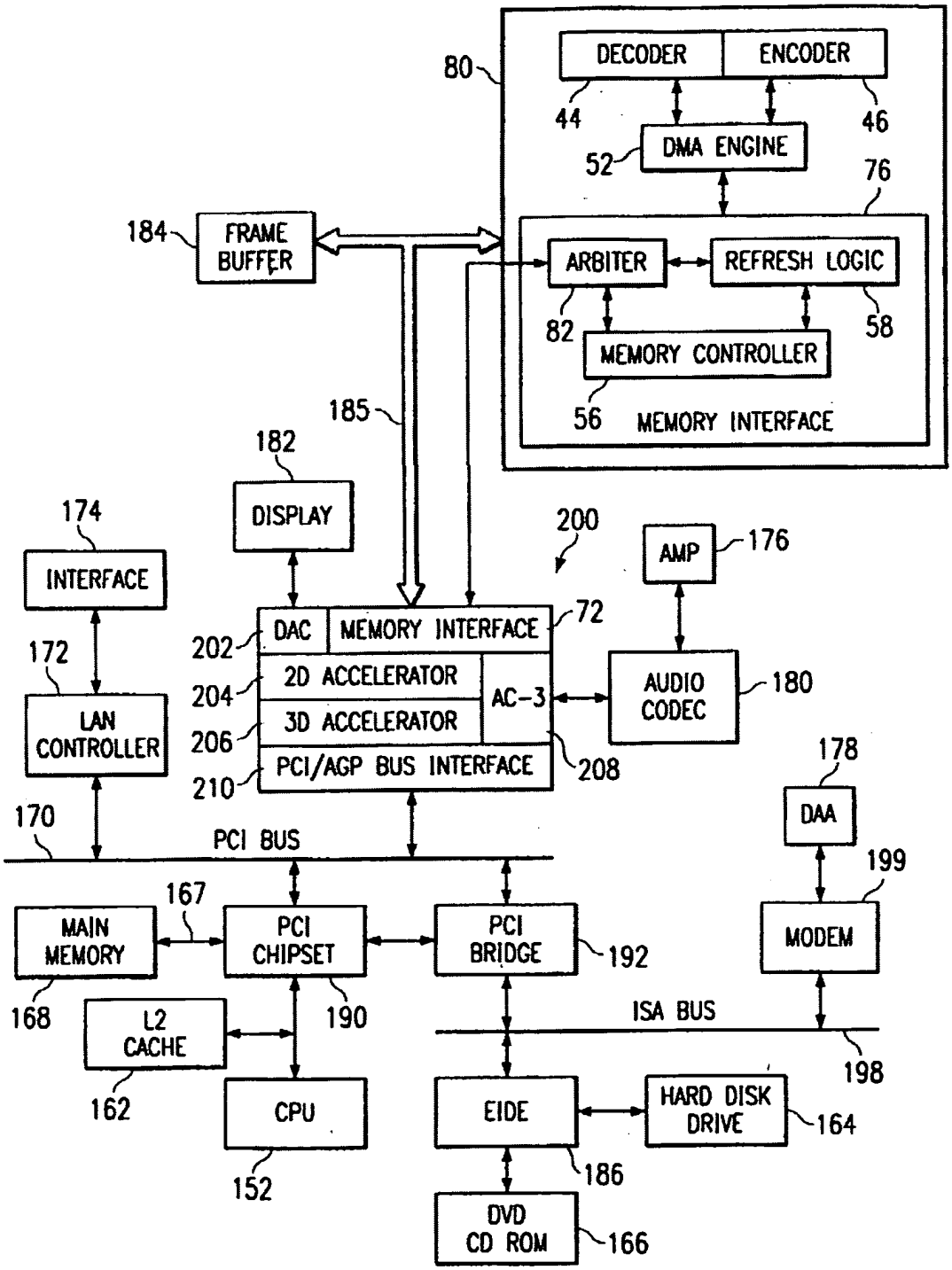


Fig. 6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AC-3
AUDIO CODEC
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LAN CONTROLLER
3D ACCELERATOR
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DAA
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PCI BUS
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MAIN MEMORY
PCI CHIPSET
PCI BRIDGE
192
MODEM
168
L2 CACHE
190
ISA BUS
198
162
CPU
EIDE
HARD DISK DRIVE
164
152
186
DVD CD ROM
166

Fig. 7

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Filing Date: 04/15/09

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12/424,389

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**17** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**3** minus 3 =	*	x$110			x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL			TOTAL	**1090**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/424,389	04/15/2009	2621	1090	96-S-012C4 (850063.553C4)	17	3

CONFIRMATION NO. 1455

30423
STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

FILING RECEIPT

Date Mailed: 05/07/2009

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Applicant(s)

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Stanford, CA;
Osvaldo Colavin, Tucker, GA;

Assignment For Published Patent Application

STMICROELECTRONICS, INC., Carrollton, TX

Power of Attorney:

Lisa Jorgenson--34845
Irena Rappaport--39260

Domestic Priority data as claimed by applicant

This application is a CON of 11/956,165 12/13/2007
which is a CON of 10/174,918 06/19/2002 PAT 7,321,368
which is a CON of 09/539,729 03/30/2000 PAT 6,427,194
which is a CON of 08/702,910 08/26/1996 PAT 6,058,459

Foreign Applications

If Required, Foreign Filing License Granted: 05/01/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/424,389**

Projected Publication Date: 08/13/2009

Non-Publication Request: No

Early Publication Request: No

Title

ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Preliminary Class

375

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12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)

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PUBLICATION NOTICE

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Title:ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Publication No.US-2009-0201305-A1
Publication Date:08/13/2009

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C4 (850063.553C4)	APPLICATION NO. 12/424,389
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE April 15, 2009	GROUP ART UNIT 2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,257,095	03/17/81	Nadir	710	119	
	AB	4,774,660	09/27/88	Conforti	364	200	
	AC	4,894,565	01/16/90	Marquardt	307	518	
	AD	5,027,400	06/25/91	Baji et al.	380	20	
	AE	5,212,742	05/18/93	Normile et al.	382	166	
	AF	5,250,940	10/05/93	Valentaten et al.	345	189	
	AG	5,363,500	11/08/94	Takeda	395	425	
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	AJ	5,459,519	10/17/95	Scalise et al.	348	431.1	
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	AR	5,621,893	04/15/97	Joh	395	200.02	
	AS	5,623,672	04/22/97	Popat	395	728	
	AT	5,682,484	10/28/97	Lambrecht	710	128	
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	AW	5,774,676	06/30/98	Stearns et al.	709	247	
	AX	5,778,096	07/07/98	Stearns	382	233	

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,793,384	08/11/98	Okitsu	345	535	
	AB	5,797,028	08/18/98	Gulick et al.	395	800.32	
	AC	5,809,245	09/15/98	Zenda	345	204	
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	AE	5,812,789	09/22/98	Diaz et al.	709	247	
	AF	5,815,167	09/29/98	Muthal	345	541	
	AG	5,960,464	09/28/99	Lam	711	202	
	AH	5,835,082	11/10/98	Perego	345	202	
	AI	5,912,676	06/15/99	Malladi et al.	345	521	
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	AO	06-030442	02/04/94	JP (with English abstract)		
	AP	06-178274	06/24/94	JP (with English abstract)		
	AQ	06-348238	12/24/94	JP (with English abstract and machine translation)		
	AR	2,100,700	01/17/95	CA		
	AS	0 673 171	09/20/95	EP		
	AT	08-018953	01/19/96	JP (with English abstract and machine translation)		
	AU	96/20567	07/04/96	WIPO		

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	AA	0 495 574	03/19/97	EP		
	AB	2740583	04/30/97	FR (with English abstract)		
	AC	0827110	03/04/98	EP		
	AD	0827348	03/04/98	EP		
	AE	10-108117	04/24/98	JP (with English abstract)		
	AF	10-145739	05/29/98	JP (with English abstract)		
	AG	0 710 029	03/27/02	EP		
	AH	0772159	01/21/04	EP		
	AI	69631364	11/04/04	DE (with English abstract)		
	AJ	0 639 032	07/18/94	EP (with English abstract)		

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AK		U.S. District Court, Eastern District of Texas Live (Sherman), Civil Docket For Case #: 4:03-cv-00276-LED, STMicroelectronics, Inc., Plaintiff v. Motorola, Inc., and Freescale Semiconductor, Inc., Defendants, Counterclaim Plaintiffs v. STMicroelectronics N.V., and STMicroelectronics, Inc., Counterclaim Defendants, date filed 18 July 2003, 47 pages
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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
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	AC		Allen J. Baum et al., "A Multimedia Chipset for Consumer Audio-Visual Applications," *IEEE Transactions on Consumer Electronics*, August 1997, Vol. 43, No. 3, pages 646-648.
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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Shailender Chaudhry and Alok Choudhary, "A Framework for Analysis of Guaranteed QOS Systems," *Video Techniques and Software for Full-Service Networks*, November 21, 1996, Vol. 2915, pages 25-38.
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	AH		Rabin Deka, "A Comprehensive Study of Digital Signal Processing Devices," *Microprocessors and Microsystems*, May 1995, Vol. 19, No. 4, pages 209-221.
	AI		Erwan Demairy et al., "On the Correctness of Multimedia Applications," *The 11th Euromicro Conference on Real-Time Systems*, IEEE Computer Society, June 9-11, 1999, pages 226-233.
	AJ		C.H. Van Dusen et al., "From Concept to an Implementation," *International Broadcasting Convention*, September 12-16, 1996.
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	AA		Borko Furht, "Processor Architectures for Multimedia: A Survey," *Multimedia Modeling*, November 17-20, 1997, pages 89-109.
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	AK		Karl Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," *IEEE Computer Graphics and Applications*, November 1992, pages 53-64.
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	AM		T. Russell Hsing, "The Challenge of VLSI Technology to Low-Bit Rate Video," pages 164-168, May 17-19, 1989.

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	AJ		D. Kim et al., "A Real-Time MPEG Encoder Using a Programmable Processor," *IEEE*, 1994, pages 161-170.
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	AL		Kiyoshi Kohiyama et al., "Architecture of MPEG-2 Digital Set-Top-Box for CATV Vod System," *IEEE*, 1996, pages 667-672.

EXAMINER	DATE CONSIDERED

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C4 (850063.553C4)	APPLICATION NO. 12/424,389
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE April 15, 2009	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Takeo Koinuma and Noriharu Miyaho, "ATM in B-ISDN Communication Systems and VLSI Realization," *IEEE Journal of Solid-State Circuits*, April 1995, Vol. 30, No. 4, pages 341-347.
	AB		Toshio Kondo et al., "Two-Chip MPEG-2 Video Encoder," *IEEE Micro*, April 1996, Vol. 16, No. 2, pages 51-58.
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	AA		Raymond T. Ng and Jinhai Yang, "An analysis of buffer sharing and prefetching techniques for multimedia systems," *Multimedia Systems*, Vol. 4, No. 2, 1996, pages 55-69.
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	AA		P. Venkat Rangan et al., "Designing an On-Demand Multimedia Service," *IEEE Communications Magazine*, July 1992, Vol. 30, No. 7, pages 56-64.
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	AA		Kevin Tsang and Belle W.Y. Wei, "A VLSI Architecture for a Real-Time Code Book Generator and Encoder of a Vector Quantizer," *IEEE Transactions on a Joint Publication of IEEE Circuits and Systems Society, the IEEE Computer Society, the IEEE Solid-State Circuits Council*, September 1994, Vol. 2, No. 3, pages 360-364.
	AB		Shin-ichi Uramoto et al., "An MPEG2 Video Decoder LSI with Hierarchical Control Mechanism," *IEEE 1997 Custom Integrated Circuits Conference*, April 26, 1995, pages 1697-1708.
	AC		Olivier Verscheure and Jean-Pierre Hubaux, "Perceptual Video Quality and Activity Metrics: Optimization of Video Service Based on MPEG-2 Encoding," *Multimedia Telecommunications and Applications*, November 1996, pages 249-265.
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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Katsuyuki Yamazaki et al., "ATM Networking and Video-Coding Techniques for QOS Control in B-ISDN," *IEEE Transactions on Circuits and Systems for Video Technology*, June 1993, Vol. 3, No. 3, pages 175-181.
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	AH		Apple Macintosh Quadra 840AV when executing the "Fusionrecorder 1.0" application as described in the 1993 Developer Note entitled "Macintosh Quadra 840AV and Macintosh Centris 660AV Computers
	AI		C-Cube CL450 MPEG Video Decoder ("CL450") as described in the "CL450 MPEG Decoder User's Manual," C-Cube Microsystems, Milpitas, CA 1992 (MOT-S 721789-721874)
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EXAMINER			DATE CONSIDERED

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1130564_1.DOC

Date: August 28, 2009

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C4 (850063.553C4)	APPLICATION NO. 12/424,389
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE April 15, 2009	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
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	AG		Maturi, G., "Single Chip MPEG Audio Decoder, "*IEEE Transactions on Consumer Electronics*, Vol. 38, No. 3, pp. 348-356, August 1992.
	AH		"MPEG Video Overview," *SGS-Thomson Microelectronics Technical Note*, pp. 1-4, 1992.
	AI		Video Electronics Standards Association, "VESA Unified Memory Architecture Hardware Specifications Proposal," Version: 1.0p, pp. 1-38, October 31, 1995.
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Date: August 28, 2009

Electronic Acknowledgement Receipt

EFS ID:	5974329
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Tyler Livas
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
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Filing Date:	15-APR-2009
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	850063_553C4_IDS_LTR.pdf	57324 80a6a83560842d94dca70e0ba7872dc230871dc3	no	3

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	850063_553C4_IDS.pdf	176275 2ffa5ed9ccfde9519d5b9d525a049a00696ed646	no	13
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3	NPL Documents	NPL_HSING.pdf	344104 2480bd66e7614eb380e1298b7b4ae2ce6c5eac38	no	5
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
Art Unit	:	2621
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	August 28, 2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

Commissioner for Patents:

In accordance with 37 CFR 1.56 and 1.97 through 1.98, applicants wish to make known to the Patent and Trademark Office the references set forth on the attached Information Disclosure Statement. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior U.S. Patent No. 7,542,045, issued June 2, 2009, which is a continuation of U.S. Patent No. 7,321,368, issued January 22, 2008; which is a continuation of U.S. Patent No. 6,427,194, issued July 30, 2002; which is a continuation of U.S. Patent No. 6,058,459, issued May 2, 2000.

The present application contains some text and drawings in common with U.S. Patent Application No. 08/702,911, filed August 26, 1996, and issued September 22, 1998 as U.S. Patent No. 5,812,789, entitled: "VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY INTERFACE" by Raul Z. Diaz and Jefferson E. Owen, which had the same effective filing date and ownership as the present application, and to that extent is related to the present application, which is incorporated herein by reference. The references listed on the attached Information Disclosure Statement were

submitted to and/or cited by the Patent and Trademark Office in the prior applications and, therefore, are not required to be provided in this application.

If the Examiner wishes, copies of any and all cited art will be provided upon request.

Applicant's attorney is aware of a law suit involving a patent in the same general subject matter, namely, a law suit involving U.S. Patent 5,812,789. This patent is not in the continuation chain of the present application, but was filed on the same date and shares some of the technical disclosure. The undersigned attorney has obtained from the public records a docket sheet printout of the litigation, which is included on the attached Information Disclosure Statement. It is the first item listed on the second page of the 1449 under the section titled "Other Prior Art," which is shown as item AK on page 3 of 13.

If the Examiner wishes to have any documents from these court papers, he is requested to let the attorney signing below know and it will be ordered from the court records to be able to be provided it to the Examiner.

Applicant's attorney believes that providing the court's docket sheet to Examiner and offering to obtain any requested documents fulfills the duty of disclosure under 37 C.F.R. 1.56 and MPEP 2001.6(c). If the Examiner believes more is needed to complete this duty, he is requested to let the attorney know.

As to any reference supplied, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 CFR 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Applicants believe this Information Disclosure Statement has been timely filed, however, the Director is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

DVC:lcs

Enclosures:
Information Disclosure Statement
Cited References (1)

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PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/424,389	04/15/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 08/28/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LINDA WISE/

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)	1455

30423 7590 10/16/2009

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
10/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/424,389	OWEN ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 8/28/2009 was considered by the examiner.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-3, 6-8, 11-14, and 17 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2, 4, 20-23 of U.S. Patent No. 7,321,368, and claims 1-3, 5-9, 12-17 of U.S. Patent No. 7,542,045. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the features of claims 1-3, 6-8, 11-14, and 17 of the instant application are contained in claims 1-2, 4, 20-23 of U.S. Patent No. 7,321,368, and claims 1-3, 5-9, 12-17 of U.S. Patent No. 7,542,045. Please see the tables below.

Table I:

Current Application: 12/424,389	U.S. Patent No. 7,321,368
1-3, 6-8, 11-14, and 17	1-2, 4, 20-23
	U.S. Patent No. 7,542,045
1-3, 6-8, 11-14, and 17	1-3, 5-9, 12-17

Table II: For instance, claim 1 of 7,321,368 and claim 1 of current application:

Current Application: 12/424,389	U.S. Patent No. 7,321,368
1. An electronic system comprising: a bus; a main memory coupled to the bus having stored therein data corresponding to video images; a video circuit coupled to the bus, the video circuit configured to receive data from the main memory corresponding to a current	1. An electronic system comprising: a main memory having stored therein data corresponding to images to be decoded and also decoded data corresponding to images that have previously been decoded; a bus coupled to the memory; a decoder coupled to the bus for receiving compressed images and for outputting data for

video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device, the current video image to be displayed adapted to be stored in the main memory; a processor coupled to the main memory, the processor for storing non-image data in the main memory and retrieving non-image data from the main memory; and an arbiter circuit coupled to the processor and to the video circuit, the arbiter circuit configured to receive requests for access to the main memory from the video circuit and the processor and to control access to the main memory by: providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state; queuing a request for access to the main memory when the arbiter circuit is in a busy state; and queuing a request for access to the main memory in an order based on a priority of the request and a priority of each of one or more other requests for access to the main memory that are currently queued when the arbiter circuit is in a queue state.	displaying the decoded images on a display device, the decoder receiving data from the main memory corresponding to at least one previously decoded image and to a current image to be decoded and outputting decoded data corresponding to a current image to be displayed, the current image being stored in the main memory; a microprocessor system coupled to the main memory, the microprocessor system storing non-image data in and retrieving data from the main memory; and an arbiter circuit coupled to both the microprocessor system and the decoder for controlling the access to said main memory by the decoder and the microprocessor.

From the tables above, it would have obvious to one skilled in the art to utilize the arbiter as disclosed in US Patent No. 7,321,368 to have the extra features as in the current application, since the arbiter circuit in the US Patent 7,321,368 has included all the features.

The same reasons are applied to U.S. Patent No. 7,542,045.

Applicant is also noted that the Power of Attorney filed on 04/15/2009 is invalid because it contains more than 10 practitioners. Applicant is referred to MPEP sections 402 and 403 to correct the problem.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12424389	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	541, 531, 542, 547, 555, 501, 519, 545	10/12/09	HN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB text search attached	10/12/09	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/HAU H NGUYEN/ Primary Examiner.Art Unit 2628

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	95	"5,576,765" "5,774,206"	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/13 17:09
S2	2	(("5,576,765") or ("5,774,206")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2006/09/13 17:13
S3	1	10/174918	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/13 17:42
S4	644	((system main) near2 memory) and (decoder with (arbiter arbitrat$3))	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/13 17:43
S5	244	S4 and (@ad<"19960826")	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/13 17:44
S6	17	S5 and (((cpu host) and decod $3) with ((main system) near memory))	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:02
S7	3	("5263142" | "5301287" | "5459519").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/09/13 17:47
S8	463	(arbiter arbitrat$3) with ((cpu $5processor host) with decod $3)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:03
S9	182	(arbiter arbitrat$3) with ((cpu $5processor host) with decod $3) with memory	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:10
S10	342	shar$3 with ((cpu $5processor host) with decod$3) with memory	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:09
S11	114	S10 and (arbiter arbitrat$3)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:11
S12	36	S10 same (arbiter arbitrat$3)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 09:35

S13	1	("6741259").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/09/14 09:36
S14	106	345/541.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 10:36
S15	37	S14 and decod$3	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 10:37
S16	70	345/542.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 10:36
S17	24	S16 and decod$3	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2006/09/14 10:49
S18	3	(arbiter same (decoder and microprocessor)).clm.	US-PGPUB	OR	ON	2006/09/14 10:50
S19	2	(arbiter with (decoder and microprocessor)).clm.	US-PGPUB	OR	ON	2006/09/14 10:50
S20	7	((main near memory) and (decoder and microprocessor)).clm.	US-PGPUB	OR	ON	2006/09/14 10:51
S21	17	((main near memory) and (decoder and (cpu host microprocessor))).clm.	US-PGPUB	OR	ON	2006/09/14 10:52
S22	35	((main near memory) and (decod$3 and (cpu host microprocessor))).clm.	US-PGPUB	OR	ON	2006/09/14 10:53
S23	136	(((system main) near memory) and (decod$3 and (cpu host microprocessor))).clm.	US-PGPUB	OR	ON	2006/09/14 10:53
S24	11	S23 and (arbiter arbitrat$3).clm.	US-PGPUB	OR	ON	2006/09/14 10:54
S25	36	"5812789"	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/05 10:17
S26	98	"5461679"	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 13:28
S27	1	("6058459").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/03/07 14:26
S28	1739	((main system) near2 memory) with (frame adj buffer)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 14:27

S29	473	S28 and (@ad<"19960826")	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 14:28
S30	72	S29 and (video with decod$3)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 14:47
S31	9	S30 and (advanced adj micro). as.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 16:35
S32	0	(("6710777").PN.").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/03/07 16:53
S33	1	("6710777").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 16:54
S34	33	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/03/07 16:54
S36	2	(("5,576,765") or ("05,774,20")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/03/07 17:07
S37	2	(("5,576,765") or ("5,774,206")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/03/07 17:39
S38	1	("5,212,742").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/03/07 17:39
S39	155	("5212742").URPN.	USPAT	OR	ON	2007/03/07 17:40
S40	0	10/641279	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/16 11:05

S41	100	(arbiter arbitrat$3) with (cpu host) with decod$3 with memory	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/20 17:52
S42	100	S41 and (@ad<"199608226")	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/20 17:25
S43	38	S41 and (@ad<"19960826")	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/20 17:35
S44	87	memory with shar$3 with (cpu host microprocessor) with decoder	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/20 17:35
S45	34	S44 and (@ad<"19960826")	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2007/11/20 17:35
S46	1	("6771264 ").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2007/11/20 17:52
S47	1	("7321368").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2008/04/25 23:26
S48	1	("7,321,368").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2008/12/22 04:01
S49	75	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5576765" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774206" | "5774676" | "5778096" | "5793384" | "5797028" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5912676" | "5923665" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/22 04:17
S50	2	(("5,461,679") or ("5,797,028")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2009/03/13 12:54

S51	6	"US 6427194"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2009/03/13 13:06
S52	2	(("6058459") or ("6427194")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2009/03/13 13:12
S53	13	("4257095" | "5212742" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789" | "5815167" | "5960464" | "6058459").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 13:26
S54	116	("5461679").URPN.	USPAT	OR	ON	2009/03/13 13:38
S55	9	("4257095" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 13:40
S56	334	(video near2 decod$3) with arbit$6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:44
S57	40	S56 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:45
S58	11246	(cpu microprocessor (central adj process$3 adj unit)) with arbit$6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
S59	3850	(cpu microprocessor (central adj process$3 adj unit)) with arbit$6 with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
S60	1301	(decoder decoding) with arbit $6 with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:48
S61	236	S59 and S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:49
S62	70	S61 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 13:49

S63	38	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5576765" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774206" | "5774676" | "5778096" | "5793384" | "5797028" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5912676" | "5923665" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/03/13 14:09
S64	3042	((system host main) near2 memory) with (arbiter arbitrat $3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:49
S65	3019	(decod$3 decoder) with (arbiter arbitrat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
S66	270	S64 and S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
S67	91	S66 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/03/13 14:50
S68	10	((video near decoder) and arbiter).clm.	US-PGPUB	OR	ON	2009/03/13 15:24
S69	298	((cpu microprocessor) and (arbitrat$3 arbiter)).clm.	US-PGPUB	OR	ON	2009/03/13 15:45
S70	1318	(video near decoder).clm.	US-PGPUB	OR	ON	2009/03/13 15:45
S71	5	S69 and S70	US-PGPUB	OR	ON	2009/03/13 15:45
S72	12	(memory with arbiter with decoder).clm.	US-PGPUB	OR	ON	2009/03/13 15:48
S73	49	(memory with (arbitrat$3 arbiter) with (cpu microprocessor (host near2 processor))).clm.	US-PGPUB	OR	ON	2009/03/13 15:51
S74	52	(decoder with (arbitrat$3 arbiter)).clm.	US-PGPUB	OR	ON	2009/03/13 15:51

S75	3	S73 and S74	US-PGPUB	OR	ON	2009/03/13 15:51
S76	31	"6058459"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/08 15:47
S77	2	(("7057639") or ("7161558")).PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	OFF	2009/10/11 23:41
S78	2	"20060087893"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 11:41
S79	1	(11/956165).APP.	USPAT; USOCR	OR	ON	2009/10/12 15:31
S80	5	((host main) near2 memory) with stor$3 with non adj image	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 15:33
S81	125	((host main) near2 memory) with access$3 with idle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 15:35
S82	38	S81 and (arbiter arbitrat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 15:36
S83	5	"7321368"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 15:39
S84	54	((host main) near2 memory) with busy near2 state	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 16:11
S87	159	(previous and current) near2 video with (decompress$3 decod$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 16:59
S88	64	S87 and ((host main) near2 memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 16:59

S89	50	(jefferson near2 owen).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 17:06
S91	8	S89 and (priority with queue)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 17:07
S92	9	("4257095" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/12 17:11
S93	85	((host main) near2 memory) with (priority with queue)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 17:14
S94	2064	priority with queue with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:00
S95	76565	decod$3 with video	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:01
S96	59	S94 and S95	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:01
S97	5	S96 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:04
S98	9	("4257095" | "5459519" | "5682484" | "5774676" | "5778096" | "5793384" | "5809245" | "5809538" | "5812789").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/12 19:05
S99	206	(arbiter arbitrat$3) with ((host main) near2 memory) with (video image)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:18
S100	104	S99 and (@ad<"19960826")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:19

S101	5	("4028663" | "4788640" | "4821177" | "5016165" | "5072420").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/10/12 19:26
S102	24	("4788640").URPN.	USPAT	OR	ON	2009/10/12 19:44
S103	171	(arbiter arbitrat$3) with (cpu microprocessor processor) with decoder	USPAT	OR	ON	2009/10/12 19:50
S104	49	(arbiter arbitrat$3) with (cpu microprocessor processor) with decoder with request$3	USPAT	OR	ON	2009/10/12 19:50
S105	72	(arbiter arbitrat$3) with (cpu microprocessor processor) with decoder with request$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 19:51
S106	5	"7321368"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/10/12 21:21

10/13/09 2:55:34 AM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12424389	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/12/2009								
	1	✓								
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	17	✓								

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C4 (850063.553C4)	APPLICATION NO. 12/424,389
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE April 15, 2009	GROUP ART UNIT 2621

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,257,095	03/17/81	Nadir	710	119	
	AB	4,774,660	09/27/88	Conforti	364	200	
	AC	4,894,565	01/16/90	Marquardt	307	518	
	AD	5,027,400	06/25/91	Baji et al.	380	20	
	AE	5,212,742	05/18/93	Normile et al.	382	166	
	AF	5,250,940	10/05/93	Valentaten et al.	345	189	
	AG	5,363,500	11/08/94	Takeda	395	425	
	AH	5,371,893	12/06/94	Price et al.	395	725	
	AI	5,450,542	09/12/95	Lehman et al.	395	162	
	AJ	5,459,519	10/17/95	Scalise et al.	348	431.1	
	AK	5,461,679	10/24/95	Normile et al.	283	304	
	AL	5,522,080	05/28/96	Harney	395	727	
	AM	5,557,538	09/17/96	Retter et al.	364	514 A	
	AN	5,576,765	11/19/96	Cheney et al.	348	407	
	AO	5,579,052	11/26/96	Artieri	348	416	
	AP	5,590,252	12/31/96	Silverbrook	395	133	
	AQ	5,598,525	01/28/97	Nally et al.	395	520	
	AR	5,621,893	04/15/97	Joh	395	200.02	
	AS	5,623,672	04/22/97	Popat	395	728	
	AT	5,682,484	10/28/97	Lambrecht	710	128	
	AU	5,748,203	05/05/98	Tang et al.	345	521	
	AV	5,774,206	06/30/98	Wasserman et al.	395	200.77	
	AW	5,774,676	06/30/98	Stearns et al.	709	247	
	AX	5,778,096	07/07/98	Stearns	382	233	

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	AA	5,793,384	08/11/98	Okitsu	345	535	
	AB	5,797,028	08/18/98	Gulick et al.	395	800.32	
	AC	5,809,245	09/15/98	Zenda	345	204	
	AD	5,809,538	09/15/98	Pollman et al.	711	151	
	AE	5,812,789	09/22/98	Diaz et al.	709	247	
	AF	5,815,167	09/29/98	Muthal	345	541	
	AG	5,960,464	09/28/99	Lam	711	202	
	AH	5,835,082	11/10/98	Perego	345	202	
	AI	5,912,676	06/15/99	Malladi et al.	345	521	
	AJ	5,923,665	07/13/99	Sun et al.	370	477	
	AK	5,936,616	08/10/99	Torborg, Jr. et al.	345	202	
	AL	6,058,459	05/02/00	Owen et al.	711	151	
	AM	6,297,832	10/02/01	Mizuyabu et al.	345	540	
	AN	6,330,644	12/11/01	Yamashita et al.	711	147	

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		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO	06-030442	02/04/94	JP (with English abstract)		
	AP	06-178274	06/24/94	JP (with English abstract)		
	AQ	06-348238	12/24/94	JP (with English abstract and machine translation)		
	AR	2,100,700	01/17/95	CA		
	AS	0 673 171	09/20/95	EP		
	AT	08-018953	01/19/96	JP (with English abstract and machine translation)		
	AU	96/20567	07/04/96	WIPO		

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	AA	0 495 574	03/19/97	EP		
	AB	2740583	04/30/97	FR (with English abstract)		
	AC	0827110	03/04/98	EP		
	AD	0827348	03/04/98	EP		
	AE	10-108117	04/24/98	JP (with English abstract)		
	AF	10-145739	05/29/98	JP (with English abstract)		
	AG	0 710 029	03/27/02	EP		
	AH	0772159	01/21/04	EP		
	AI	69631364	11/04/04	DE (with English abstract)		
	AJ	0 639 032	07/18/94	EP (with English abstract)		

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	AK		U.S. District Court, Eastern District of Texas Live (Sherman), Civil Docket For Case #: 4:03-cv-00276-LED, STMicroelectronics, Inc., Plaintiff v. Motorola, Inc., and Freescale Semiconductor, Inc., Defendants, Counterclaim Plaintiffs v. STMicroelectronics N.V., and STMicroelectronics, Inc., Counterclaim Defendants, date filed 18 July 2003, 47 pages
	AL		Bryan Ackland, "The Role of VLSI in Multimedia," *IEEE Journal of Solid-State Circuits*, April 1994, Vol. 29, No. 4, pages 381-388.
	AM		Joel F. Adam and David L. Tennenhouse, "The Vidboard: A Video Capture and Processing Peripheral for a Distributed Multimedia System," *ACM Multimedia*, August 1-6, 1993, Vol. 5, No. 2, pages 113-120.
	AN		Matthew Adiletta, et al., "Architecture of a Flexible Real-Time Video Encoder/Decoder: The DECchip 21230," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 136-148.
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	April 15, 2009	2621

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	AA		Yin Bao and Adarshpal S. Sethi, "OCP_A: An Efficient QoS Control Scheme for Real Time Multimedia Communications," *IEEE Global Telecommunications Conference*, Conference Record, November 3-8, 1997, Vol. 2 of 3, pages 741-745.
	AB		Mark Baugher, "The OS/2 Resource Reservation System," *Multimedia Computing and Networking 1995*, February 1995, Vol. 2417, pages 167-176.
	AC		Allen J. Baum et al., "A Multimedia Chipset for Consumer Audio-Visual Applications," *IEEE Transactions on Consumer Electronics*, August 1997, Vol. 43, No. 3, pages 646-648.
	AD		Vasudev Bhaskaran et al., "Multimedia Architectures: From Desktop Systems to Portable Appliances," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 14-25.
	AE		Philip Bonannon et al., "The Architecture of the Dali Main-Memory Storage Manager," *Multimedia Tools and Applications*, 1997, Vol. 4, pages 115-151.
	AF		C. Bouville et al., "DVFLEX: A Flexible MPEG Real Time Video CODEC," *International Conference on Image Processing*, September 16-19, 1996, Vol. II of III, pages 829-832.
	AG		V. Michael Bove, Jr., "The Impact of New Multimedia Representations on Hardware and Software Systems," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 34-39.
	AH		Apurva Brahmbatt, "A VLSI Architecture for Real Time Code Book Generator and Encoder of a Vector Quantizer," *International Conference on Image Processing*, IEEE Signal Processing Society, Vol. 2, September 16-19, 1996, pages 991-994.
	AI		Dave Bursky, "Codec Compresses Images in Real Time: Real-Time Motion Video or Still Images Can be Compressed with Single-Chip Multistandard Core," *Electronic Design*, October 3, 1993.
	AJ		Dave Bursky, "Performing Over 8 BOPS, A Two Chip Set Can Compress or Expand Video in Real Time Image Processing Chip Set Handles Full Motion Video," *Electronic Design*, May 3, 1993.
	AK		Navin Chaddha et al., "A Real-Time Scalable Color Quantizer Trainer/Encoder," *The Twenty-Eighth Asilomar Conference on Signals, Systems & Computers*, October 30-November 2, 1994, pages 203-207.
	AL		Shih-Fu Chang et al., "Columbia's VoD and Multimedia Research Testbed with Heterogeneous Network Support," *Multimedia Tools and Applications*, 1997, Vol. 5, pages 171-184.

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	April 15, 2009	2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Shailender Chaudhry and Alok Choudhary, "A Framework for Analysis of Guaranteed QOS Systems," *Video Techniques and Software for Full-Service Networks*, November 21, 1996, Vol. 2915, pages 25-38.
	AB		Geng-Lin Chen et al., "Video Encoder Architecture for MPEG2 Real Time Encoding," *IEEE Transactions Consumer Electronics*, August 1996, Vol. 42, No. 3, pages 290-299.
	AC		Raymond M.K. Cheng and Donald W. Gillies, "Disk Management for a Hard Real-Time File System," *Multimedia Systems*, Vol. 4, No. 2, 1996, pages 255-260.
	AD		Leonardo Chiariglione, "MPEG: A Technological Basis for Multimedia Applications," *Multimedia*, Spring 1995, Vol. 2, No. 1.
	AE		Winston Sijin Choe et al., "ATM-Based Multi-Party Conferencing System," *IEEE Global Telecommunications Conference*, November 1995, Vol. 1 of 3, pages 592-596.
	AF		Francoise Colaitis, "Opening Up Multimedia Object Exchange with MHEG," *Multimedia*, Summer 1994, Vol. 2, No. 2.
	AG		Geoff Coulson et al., "The Design of a QoS-Controlled ATM-Based Communications System in Chorus," *IEEE Journal on Selected Areas in Communications*, May 1995, Vol. 13, No. 4, pages 686-699.
	AH		Rabin Deka, "A Comprehensive Study of Digital Signal Processing Devices," *Microprocessors and Microsystems*, May 1995, Vol. 19, No. 4, pages 209-221.
	AI		Erwan Demairy et al., "On the Correctness of Multimedia Applications," *The 11th Euromicro Conference on Real-Time Systems*, IEEE Computer Society, June 9-11, 1999, pages 226-233.
	AJ		C.H. Van Dusen et al., "From Concept to an Implementation," *International Broadcasting Convention*, September 12-16, 1996.
	AK		Santanu Dutta et al., "VLSI Issues in Memory-System Design for Video Signal Processors," *IEEE* 1995, pages 498-503.
	AL		Fandrianto, Jan and Tim Williams, "A Programmable Solution for Standard Video Compression," in *IEEE Computer Society Press,* Thirty-Seventh IEEE Computer Society International Conference, San Francisco, CA, February 24-28, 1992, pp. 47-50.
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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Borko Furht, "Processor Architectures for Multimedia: A Survey," *Multimedia Modeling*, November 17-20, 1997, pages 89-109.
	AB		Subramanian Ganesan, "A Dual-DSP Microprocessor System for Real-Time Digital Correlation," *Microprocessors and Microsystems*, Vol. 15, No. 7, September 1991, pages 379-384.
	AC		Wanda Gass, "Architecture Trends of MPEG Decoders for Set-Top Box," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 162-169.
	AD		J. Goodenough et al., "A General Purpose, Single Chip Video Signal Processing (VSP) Architecture for Image Processing, Coding and Computer Vision," *IEEE* 1994, pages 1-4.
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	AJ		Fouad Guediri and Pavani Chilamakuri, "An Affordable Solution to Real-Time Video Compression," *Technical Conference, Session 10 Imaging & HDTV*, March 8, 1995, pages 261-265.
	AK		Karl Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," *IEEE Computer Graphics and Applications*, November 1992, pages 53-64.
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Date: August 28, 2009

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	AD		M. Irvin et al., "A New Generation of MPEG-2 Video Encoder ASIC & ITS Application to New Technology Markets," *International Broadcasting Convention*, September 12-16, 1996, Pub. No. 428.
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	AH		Kevin A. Kettler and Jay K. Strosnider, "Scheduling Analysis of the Micro Channel Architecture for Multimedia Applications," *International Conference on Multimedia Computing and Systems*, May 14-19, 1994, pages 403-414.
	AI		Saied Hosseini Khayat and Adreas D. Bovopoulos, "A Proposed Bus Arbitration Scheme for Multimedia Workstations," *International Conference on Multimedia Computing and Systems*, May 14-19, 1994, pages 415-423.
	AJ		D. Kim et al., "A Real-Time MPEG Encoder Using a Programmable Processor," *IEEE*, 1994, pages 161-170.
	AK		Toshiro Kinugasa et al., "A Video Pre/Post-processing LSI for Video Capture," *1996 Digest of Technical Papers*, June 5-7, 1996, pages 396-397.
	AL		Kiyoshi Kohiyama et al., "Architecture of MPEG-2 Digital Set-Top-Box for CATV Vod System," *IEEE*, 1996, pages 667-672.

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1130564_1.DOC

Date: August 28, 2009

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 96-S-012C4 (850063.553C4)	APPLICATION NO. 12/424,389
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANTS Jefferson Eugene Owen et al.	
	FILING DATE April 15, 2009	GROUP ART UNIT 2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Takeo Koinuma and Noriharu Miyaho, "ATM in B-ISDN Communication Systems and VLSI Realization," *IEEE Journal of Solid-State Circuits*, April 1995, Vol. 30, No. 4, pages 341-347.
	AB		Toshio Kondo et al., "Two-Chip MPEG-2 Video Encoder," *IEEE Micro*, April 1996, Vol. 16, No. 2, pages 51-58.
	AC		S.W. Lau and John C.S. Lui, "A Novel Video-On-Demand Storage Architecture for Supporting Constant Frame Rate with Variable Bit Rate Retrieval," *Network and Operating Systems Support for Digital Audio and Video*, April 19-21, 1995, pages 294-305.
	AD		Woobin Lee et al., "MediaStation 5000: Integrating Video and Audio," *Multimedia*, Summer 1994, Vol. 1, No. 2, pages 50-61.
	AE		Woobin Lee et al., "Real-Time MPEG Video Compression Using the MVP," *Data Compression Conference '94*, March 29-31, 1994.
	AF		Chia-Hsing Lin et al., "Low Power Design for MPEG-2 Video Decoder," *IEEE Transactions on Consumer Electronics*, August 1996, Vol. 42, No. 3, pages 513-521.
	AG		Cha-Hsing Lin and Chein-WeiJen, "On the Bus Arbitration for MPEG2 Video Decoder," *VLSI Tech, Systems and Appl. 1995 Symposium*, pages 201-205.
	AH		J. Lin et al., "DMA-based Communications between PC and DSP," *Microprocessors and Microsystems*, April 1991, Vol. 15, No. 3, pages 137-142.
	AI		Ferran Lisa et al., "A Reconfigurable Coprocessor for a PCI-based Real Time Computer Vision System," *Field-Programmable Logic and Applications*, 7th International Workshop, FPL 1997, London, UK, September 1-3, 1997, pages 392-399.
	AJ		M. Norley Liu, "MPEG Decoder Architecture for Embedded Applications," *IEEE Transactions on Consumer Electronics*, November 1996, Vol. 42, No. 4, pages 1021-1028.
	AK		Kamal N. Majeed, "Dual Processor Automotive Controller," *IEEE*, 1988, pages 39-44.
	AL		Masatoshi Matsuo et al., "A Programmable Video Codec System for Low-Bit-Rate Communication," *IEEE Transactions on Consumer Electronics*, August 1997, Vol. 43, No. 3, pages 903-910.
	AM		Kiyoshi Miura et al., "A 600 mW Single Chip MPEG2 Video Decoder," *IEICE Trans. Electrono*, December 1995, Vol. E78-C, No. 12, pages 1691-1696.
	AN		Steven G. Morton, "A236 Parallel DSP Chip Provides Real-Time Video Processing Economically and Efficiently," *Electro '96 Professional Program Proceedings*, April 30-May 2, 1996, pages 261-268.

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OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		Raymond T. Ng and Jinhai Yang, "An analysis of buffer sharing and prefetching techniques for multimedia systems," *Multimedia Systems*, Vol. 4, No. 2, 1996, pages 55-69.
	AB		Agnes Ngai et al., "A Scalable Chip Set for MPEG2 Real-Time Encoding," *CompCon*, 1996, pages 193-198.
	AC		Lek Heng Ngoh et al., "On Storage Server Issues for Multimedia-on-Demand System," *Multimedia Modeling*, November 1995, pages 393-409.
	AD		Huw Oliver et al., "Distributed Connection Management for Real-Time Multimedia Services," *From Multimedia Services to Network Services*, December 1997, pages 59-74.
	AE		T.H. Ooi et al., "A PC-Based MPEG Compressed Data Decoder," *IEEE Transactions on Consumer Electronics*, November 1995, Vol. 41, No. 4, pages 1169-1173.
	AF		Yasushi Ooi et al., "An MPEG-2 Encoder Architecture Based on a Single Chip Dedicated LSI with a Control MPU," *IEEE*, 1997, pages 599-602.
	AG		Banu Ozden et al., "On the Design of a Low-Cost Video-on-Demand Storage System," *IEEE Journal of Solid State Circuits*, April 1994, Vol. 29, No. 4, pages 40-54.
	AH		Pallavi Shah, "Multimedia on the Internet," *The Twentieth Annual International Computer Software & Applications Conference*, August 21-23, 1996, page 150.
	AI		Pramod Pancha and Magda El Zarki, "Bandwidth-Allocation Schemes for Variable-Bit-Rate MPEG Sources in ATM Networks," *IEEE Transactions on Circuits and Systems for Video Technology*, June 1993, Vol. 3, No. 3, pages 190-198.
	AJ		R. Radhakrishna Pillai, "Multimedia Over the Internet," *The Twentieth Annual International Computer Software & Applications Conference*, August 21, 23, 1996, page 149.
	AK		Peter Pirsch et al., "Architectural Approaches for Multimedia Processors," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 2-13.
	AL		Peter Pirsch et al., "VLSI Architectures for Video Compression – A Survey," *Proceedings of the IEEE*, February 1995, Vol. 83, No. 2, pages 220-246.
	AM		Peter Pirsch and Winfried Gehrke, "VLSI Architectures for Video Signal Processing," *Image Processing and its Applications*, July 4-6, 1995, Conference Publication No. 410, pages 6-10.
	AN		Herbert Plansky, "Variable Block-Size Vector Quantization in the Transform Domain," *Signal Processing VI Theories and Applications*, Volume III, 1992, pages 1243-1246.

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	96-S-012C4 (850063.553C4)	12/424,389
	APPLICANTS	
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Jefferson Eugene Owen et al.	
	FILING DATE	GROUP ART UNIT
	April 15, 2009	2621

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
	AA		P. Venkat Rangan et al., "Designing an On-Demand Multimedia Service," *IEEE Communications Magazine*, July 1992, Vol. 30, No. 7, pages 56-64.
	AB		S.F. Reddaway, "Fractal Graphics and Image Compression on a DAP," *The Design and Application of Parallel Digital Processors*, April 11-15, 1988, page 201.
	AC		William D. Richard et al., "The Washington University Broadband Terminal," *IEEE Journal on Selected Areas in Communications*, February 1993, Vol. 11, No. 2, pages 276-282.
	AD		William D. Richard et al., "The Washington University Multimedia System," *Multimedia Systems*, Vol. 1, No. 3, 1993, pages 120-131.
	AE		Reza Rooholamini and Vladimir Cherkassky, "ATM-Based Multimedia Servers," *Multimedia*, Spring 1995, Vol. 2, No. 1, pages 39-52.
	AF		Amr Sabaa et al., "Design and Modelling of a Nonblocking Input Buffer ATM Switch," *Can. J. Elect. & Comp. Eng.*, Vol. 22, November 3, 1997, pages 87-93.
	AG		N.L. Seed et al., "An Enhanced Transputer Module for Real-Time Image Processing," *Third International Conference on Image Processing*, 1989, pages 131-135.
	AH		Pallavi Shah, "Multimedia on the Internet," *The Twentieth Annual International Computer Software & Applications Conferences*, COMPSAC '96, August 21-23, 1996, page 150.
	AI		Doug Shepherd et al., "Quality-of-Service Support for Multimedia Applications," *Multimedia*, Fall 1996, Vol. 3, No. 3, pages 78-82.
	AJ		N. Sriskanthan et al., "A Real-Time PC-Based Video Phone System on ISDN/Lan," *IEEE Transactions on Consumer Electronics*, May 1995, Vol. 41, No. 2, pages 332-342.
	AK		Paul A. Stirpe and Dinesh C. Verma, "Application Migration to Reserved Bandwidth Networks," *Multimedia Computing and Networking 1995*, February 1995, Vol. 2417, pages 428-434.
	AL		Ichiro Tamitani et al., "An Encoder/Decoder Chip Set for the MPEG Video Standard," *IEEE International Conference on Acoustics, Speech and Signal Processing*, March 23-26, 1992, pages 661-664.
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	AN		Fouad A. Tobagi et al., "Streaming RAID – A Disk Array Management System for Video Files," *ACM Multimedia 93*, August 1-6, 1993, pages 393-400.

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			OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	AA		Kevin Tsang and Belle W.Y. Wei, "A VLSI Architecture for a Real-Time Code Book Generator and Encoder of a Vector Quantizer," *IEEE Transactions on a Joint Publication of IEEE Circuits and Systems Society, the IEEE Computer Society, the IEEE Solid-State Circuits Council*, September 1994, Vol. 2, No. 3, pages 360-364.
	AB		Shin-ichi Uramoto et al., "An MPEG2 Video Decoder LSI with Hierarchical Control Mechanism," *IEEE 1997 Custom Integrated Circuits Conference*, April 26, 1995, pages 1697-1708.
	AC		Olivier Verscheure and Jean-Pierre Hubaux, "Perceptual Video Quality and Activity Metrics: Optimization of Video Service Based on MPEG-2 Encoding," *Multimedia Telecommunications and Applications*, November 1996, pages 249-265.
	AD		Andreas Vogel et al., "Distributed Multimedia and QOS: A Survey," *Multimedia*, Summer 1995, Vol. 2, No. 2, pages 10-19.
	AE		Marco Winzker et al., "Architecture and Memory Requirements for Stand-Alone and Hierarchical MPEG2 HDTV-Decoders with Synchronous DRAMs," *IEEE International Symposium on Circuits and Systems*, April 30-May 3, 1995, pages 609-612.
	AF		Andrew Wolfe et al., "Design Methodology for Programmable Video Signal Processors," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 26-31.
	AG		Lars C. Wolfe and Ralf Steinmetz, "Concepts for Resource Reservation in Advance," *Multimedia Tools and Applications*, 1997, pages 255-278.
	AH		Jeffrey J. Wong et al., "The H-Bus: A Media Acquisition Bus Optimized for Multiple Streams," *Multimedia Hardware Architectures 1997*, February 12-13, 1997, Vol. 3021, pages 40-50.
	AI		Dallas E. Wrege and Jorg Liebeherr, "Video Traffic Characterization for Multimedia Networks with a Deterministic Service," *IEEE Inforcom '96*, March 1996, Vol. 2, pages 537-544.
	AJ		Chen-Mie Wu et al., "A Function-Pipelined Architecture and VLSI Chip for MPEG Video Image Coding," *IEEE Transactions on Consumer Electronics*, November 1995, Vol. 41, No. 4, pages 1127-1137.
	AK		A. Yamada et al., "Real-time MPEG2 Encoding and Decoding with a Dual-Issue RISC Processor," *Proceedings of the IEEE 1997 Custom Integrated Circuits Conference*, May 5-8, 1997, pages 225-228.

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	AA		Katsuyuki Yamazaki et al., "ATM Networking and Video-Coding Techniques for QOS Control in B-ISDN," *IEEE Transactions on Circuits and Systems for Video Technology*, June 1993, Vol. 3, No. 3, pages 175-181.
	AB		Masahiko Yoshimoto et al., "ULSI Realization of MPEG2 Realtime Video Encoder and Decoder – An Overview," *IEICE Trans. Electron*, May 23, 1995, Vol. E78-C, No. 12, pages 1668-1681.
	AC		Frank Fran-Ko Yu et al., "Resource Management Issues of a Video Server," *Multimedia Storage and Archiving Systems*, November 18-19, 1996, Vol. 2916, pages 290-300.
	AD		Saif S. Zahir and Hussein Alnuweiri, "VBR MPEG-2 Encoded Video Over Broadband Network," *Proceedings of SPIE*, November 3-5, 1997, Vol. 3231, pages 372-381.
	AE		Hui Zhang and Edward W. Kightly, "Red-VBR: A New Approach to Support Delay-Sensitive VBR Video in Packet-Switched Networks," *Network and Operating System Support for Digital Audio and Video*, April 19-21, 1995, pages 258-272.
	AF		Subramaniam Ganesan, "A Dual-DSP Microprocessor System for Real-Time Digital Correlation," *Microprocessors and Microsystems*, September 1991, Vol. 15, No. 7, pages 29-37.
	AG		The Motorola MCD212 Video Decoder and System Controller ("MCD212")(as described in the Advance Information manual, published in the U.S. August 1995, at MOT-S 723153-723240)
	AH		Apple Macintosh Quadra 840AV when executing the "Fusionrecorder 1.0" application as described in the 1993 Developer Note entitled "Macintosh Quadra 840AV and Macintosh Centris 660AV Computers
	AI		C-Cube CL450 MPEG Video Decoder ("CL450") as described in the "CL450 MPEG Decoder User's Manual," C-Cube Microsystems, Milpitas, CA 1992 (MOT-S 721789-721874)
	AJ		S. Undy et al., "A low-cost graphics and multimedia workstation chip set," *IEEE Micro*, Vol. 14, No. 2, April 1994, Pages 10-22.
	AK		Bhed, H. and P. Srinivasan, "A High-Performance Cross-Platform MPEG Decoder," *Digital Video Compression on Personal Computers: Algorithms and Technologies, SPIE Proceedings*, February 7-8, 1994, Vol.2187, pp. 241-248

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INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	FILING DATE April 15, 2009	GROUP ART UNIT 2621

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	AA		Bursky D., "Highly Integrated Controller Eases MPEG-2 Adoption," *Electronic Design*, Vol. 43, No. 17, pp.141-142, August 21,1995.
	AB		Butler, B. and T. Mace, "The Great Leap Forward," *PC Magazine*, pp. 241-244, 246, 248, 250, 253-254, 256, 260-261, 264, 266-268, 273-275, 278, October 11, 1994.
	AC		Doquilo, J. "Symmetric Multiprocessing Servers: Scaling the Performance Wall," *Infoworld*, pp. 82-85, 88-92, March 27, 1995.
	AD		Galbi, D. et al., "An MPEG-1 Audio/Video Decoder with Run-Length Compressed Antialiased Video Overlays," *IEEE International Solid State Circuits Conference*, pp. 286-287, 381, 1995.
	AE		Giorgis, T., "SMP Network Operating Systems," *Computer Dealer News*, Vol. 12, No. 16, August 8,1996.
	AF		King, A., *Inside Windows 95*, Microsoft Press, Redmond Washington, pp.85-90, 1994.
	AG		Maturi, G., "Single Chip MPEG Audio Decoder, "*IEEE Transactions on Consumer Electronics*, Vol. 38, No. 3, pp. 348-356, August 1992.
	AH		"MPEG Video Overview," *SGS-Thomson Microelectronics Technical Note*, pp. 1-4, 1992.
	AI		Video Electronics Standards Association, "VESA Unified Memory Architecture Hardware Specifications Proposal," Version: 1.0p, pp. 1-38, October 31, 1995.
	AJ		Video Electronics Standards Association, "VESA Unified Memory Architecture VESA BIOS Extensions (VUMA-SBE Proposal), Version 1.0p, pp. 1-26, November 1, 1995.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	January 15, 2010

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Commissioner for Patents:

In response to the Office Action dated October 16, 2009, please enter the following response.

REMARKS

In the Office Action mailed October 16, 2009, the Examiner noted that a timely filed terminal disclaimer may be used to overcome the non-statutory double patenting rejection. The Examiner noted that the power of attorney was one of the older types which was in use some years ago and named more than ten practitioners in the power of attorney. Accordingly, applicants were referred to MPEP Sections 402 and 403 to correct the problem. Applicants' attorney has reviewed Sections 402 and 403 and in particular the first part of Section 402 which refers to 37 CFR 1.32(c)(3) and Section 403.01. Sub-part (3) of 37 CFR 1.32(c) indicates that a separate paper should be included which states which of the practitioners named in the power of attorney to be recognized by the Office as being of record in the application to which the power is directed. Further, MPEP 403.01 authorized an attorney appointed by an associate power of attorney to file such a request for associate powers dated before June 25, 2004. Accordingly, such a paper is included herewith.

The attached paper makes clear that only three persons are to be recognized as being of record in the application. Among those which are recognized in the application is David V. Carlson, who is signing the terminal disclaimer attached. Accordingly, it is believed that this terminal disclaimer attached can be validly entered in the present application.

It the Examiner believes that this approach is not correct, she is invited to call applicants' attorney at the number listed below to provide specific instructions as to the preferred course of action. Having reviewed MPEP Sections 402 and 403, it is believed that the present submission should be acceptable to satisfy the Examiner's request, and for this reason issuance of the patent to allowance is respectfully requested.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

DVC:lch

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
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Fax: (206) 682-6031

1542048_1.DOC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	January 15, 2010

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF ATTORNEYS TO BE RECOGNIZED

UNDER 37 CFR 1.32(c)(3)

Commissioner for Patents:

In accordance with 37 CFR 1.32(c)(3) and MPEP 403.01, applicants hereby state that the attorneys to be recognized by the Office as being of record in the application are the following individuals:

David V. Carlson – Reg. No. 31,153

Lisa K. Jorgenson – Reg. No. 34,845

E. Russell Tarleton – Reg. No. 31,800

The above statement is made based on the power of attorney provided to Lisa K. Jorgenson in August of 1996 and her subsequent appointment of an associate power of attorney on April 12, 1999 which includes all of the individuals listed above.

A copy of the power of attorney and appointment of the associate power is provided as set forth in MPEP 402. A copy of the associate power of attorney and the authority to file this request is set forth in MPEP 403.01, which has been followed.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

Enclosure:
Copy of Declaration and Power of Attorney

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1542032_1.DOC

This Declaration copy is intend. for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

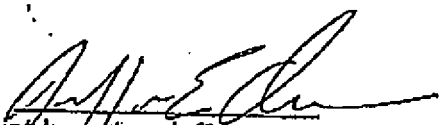
I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

Please send all correspondence to:

Lisa K. Jorgenson
Reg. No. 34,845
SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006
(214) 466-7414

Inventor's Signature: 
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: Aug 22, 1996
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
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Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
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Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
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Citizenship: United States of America

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Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: 8/20/96
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~~Stanford, CA 94305~~ 750 Montrose Avenue #25
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Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
98B Escondido Village
Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: Flavio Osvaldo
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: August 19, 1996
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

This Power of Attorney copy is intended for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson E. Owen et al.
Application No.	:	08/702,910
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY
Examiner	:	Glenn Gossage
Art Unit	:	2751
Docket No.	:	96-S-12 (850063.553)
Date	:	April 12, 1999

Assistant Commissioner for Patents
Washington, DC 20231

APPOINTMENT OF ASSOCIATE POWER OF ATTORNEY

Sir:

I, Lisa K. Jorgenson, attorney of record in the above-identified application, appoint as associate attorneys David V. Carlson, Reg. No. 31,153; Michael J. Donohue, Registration No. 35,859, Kevin S. Ross, Reg. No. 42,116; Dale C. Barr, Reg. No. 40,498; Kevin S. Costanza, Reg. No. 37,801, Brian L. Johnson, Reg. No. 40,033, Paul F. Rusyn, Reg. No. 42,118, Dennis M. de Guzman, Reg. No. 41,702; E. Russell Tarleton, Reg. No. 31,800, John M. Wechkin, Reg. No. 42,216; Robert D. McCutcheon, Reg. No. 38,717; and Theodore E. Galanthay, Reg. No. 24,122.

It is requested that correspondence continue to be addressed to Lisa K. Jorgenson at:

Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006-5039

Respectfully submitted,
STMicroelectronics, Inc.

Lisa K. Jorgenson
Lisa K. Jorgenson
Registration No. 34,845

LKJ:BLJ:jab1

1310 Electronics Drive
Carrollton, Texas 75006-5039
(972) 466-7414
Fax: (972) 466-7044-5039

u:\float\jab1\850063.553-Assocpoa

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	January 15, 2010

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FEE DEFICIENCY AUTHORIZATION FORM

Commissioner for Patents:

Applicants hereby authorize the Director to charge any deficiencies in fees due by way of the enclosed papers only under 37 CFR 1.16 and 1.17 to Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1542218_1.DOC

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 96-S-012C4 (850063.553C4)

In re Application of: Jefferson Eugene Owen

Application No.: 12/424,389

Filed: April 15, 2009

For: ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

The owner*, STMicroelectronics, Inc. of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** Nos. 7,321,368 and 7,542,045 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Registration No. 31,153

/David V. Carlson/ — Signature
January 15, 2010 — Date

David V. Carlson
Typed or printed name

(206) 622-4900
Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this statement. See MPEP § 324.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 1505651_1.DOC

Electronic Patent Application Fee Transmittal

Application Number:	12424389
Filing Date:	15-Apr-2009
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	David V. Carlson/Laura Hernandez
Attorney Docket Number:	96-S-012C4 (850063.553C4)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory disclaimer	1814	1	140	140
		Total in USD ($)		**140**

Electronic Acknowledgement Receipt

EFS ID:	6824826
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Laura Hernandez
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	15-JAN-2010
Filing Date:	15-APR-2009
Time Stamp:	19:11:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$140
RAM confirmation Number	5611
Deposit Account	191090
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		553C4_RESP.pdf	52357 d52fa361ffc6467b57e584b22c34068aa99c433d	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Applicant Arguments/Remarks Made in an Amendment		2	3	
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	553C4_STMT_ATTYS.pdf	124967 824f30c68b4838b2438a27930a4373d56a499692	no	7
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	553C4_FEE_DEF.pdf	48655 ba5571ee0218c8fd7971dc961ac7ef18757d040a	no	1
Warnings:					
Information:					
4	Terminal Disclaimer Filed	553C4_TERMINAL_DISCLAIMER.pdf	84712 399a1cdaefc743a0ffe908f8b628971f2750e0d6	no	1
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30584 807a1825bca2790ab0f43e62125b63872d394675	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	341275		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/424,389	OWEN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☐ APPROVED	☒ DISAPPROVED
Date Filed : 1/15/10	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

Felicia D. Roberts

See TD Checklist for explanation

U.S. Patent and Trademark Office

Rev. 05/19/09	Doc. Code: DISQ.CKLIST

TERMINAL DISCLAIMER INFORMAL CHECKLIST

APPL. S.N.: 12/424,389	**DATE:**
EXAMINER:	**ART UNIT:**
PARALEGAL: /FELICIA ROBERTS/	**MAIL ROOM DATE:**
NUMBER OF TD(s) FILED: 1	

INSTRUCTIONS: The paralegal has reviewed the submitted TD with the results as set forth below.
If you agree, please use the appropriate form paragraphs identified by this informal memo in your next Office action to notify applicant about the TD. If you disagree, please contact a QAS.

THIS CHECKLIST IS AN INFORMAL, INTERNAL CHECKLIST ONLY. IT MUST NOT BE MAILED TO APPLICANT. IT WILL BE SOFT SCANNED AND NOT VIEWABLE TO THE PUBLIC.

☐ The TD is PROPER and has been accepted and recorded. (See FP 14.23.)

☒ The TD is NOT PROPER and has not been accepted for the reason(s) checked below. (See FP 14.24.)

☐ The disclaimer fee under 37 CFR 1.20(d) in the amount of $ has not been submitted, nor is there any pre authorization in the application to charge to a deposit account. (See FP 14.24 and 14.26.07.)

☐ The LIE has not processed fee for TD (the Paralegal should ask LIE to process the fee).

☐ The TD does not satisfy 37 CFR 1.32(b) (3) in that the person who signed the TD has not stated either: (a) the extent of his/her ownership interest, or (b) the extent of the business/organization entity's ownership interest on whose behalf the person signed. (See FPs 14.26 and 14.26.01.)

☐ The TD lacks the – enforceable only during the period of common ownership – clause needed to overcome a double patenting 37 CFR 1.321(c). (See FP 14.27.01).

☐ The TD lacks 37 CFR 1.321(d) statement for joint research agreement under 35 U.S.C. 103(c) (2) & (3). It doesn't include the waiver and enforceability provisions of 37 CFR 1.321(d). (See FP 14.27.011.)

☐ TD is directed to a particular claim(s); this is not acceptable, since the disclaimer must be of a terminal portion of the entire patent to be granted, MPEP 1490. (See FPs 14.26 and 14.26.02).

☒ The person who signed the terminal disclaimer:

- ☐ failed to state his/her capacity to sign for the business/organization entity. (See FP 14.28.)
- ☐ is not recognized as an officer of the assignee. (See FP 14.29.)
- ☒ does not have power of attorney, and thus, is not of record. (See FP 14.29.01.)

(Note: PoA can be given to a customer number, wherein all practitioners listed under the customer number have PoA. If PoA is established by a list of practitioners, the list may not comprise more than 10 practitioners. A representative of the assignee, who is not of record, cannot sign the TD unless it is established that the representative is a party authorized to act on behalf of the assignee.)

☐ The TD is not supported by evidence of chain of title to the assignee signing the TD due to a failure to submit either: (a) documentary evidence of a chain of title from the original inventor(s) to the assignee and a statement affirming that the documentary evidence was, or concurrently is being, submitted for recordation; or (b) the reel and frame number(s) where such documentary evidence is recorded in the Office. 37 CFR 3.73(b). (See FPs 14.30 and 14.34)

NOTE: This documentary evidence or the specifying of the reel and frame number may be found in the TD or in a separate paper submitted by applicant.)

☐ The TD is not supported by adequate evidence of chain of title to the assignee signing the TD, because the person who signed the submission under 37 CFR 3.73(b):

☐ has failed to state his/her capacity to sign for the business entity. (See FPs 14.30.02 and 14.16.02

☐ is not recognized as an officer of the assignee. (See FP 14.30.02 and 14.16.03)

(Note: On the submission under 37 CFR 3.73(b), the signature of an attorney or agent registered to practice before the Office is not sufficient, unless the attorney or agent is authorized to act on behalf of the assignee.)

☐ The TD is not signed (See FPs 14.26 and 14.26.03)

☐ The serial number of the application (or the number of the patent) which forms the basis for the double patenting is not identified (i.e., missing or incorrect) in the TD. (See FP 14.32)

☐ The serial number of the application being examined (or the number of the patent under reexam or reissue) is not identified or incorrect. (See FPs 14.26 and 14.26.04 or 14.26.05)

☐ The TD is not signed by all owners. See FPs 14.26 and 14.26.06.

☐ The period disclaimed is incorrect or not specified. (See FPs 14.24, 14.27.02 or 14.27.03)

☐ Other

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	March 24, 2010

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Commissioner for Patents:

In response to a phone conference of today, March 24, 2010, please enter the following response.

REMARKS

Examiner Nguyen placed a phone call to the below signed attorney for applicant on March 24, 2010, requesting a different form for the power of attorney and that a new terminal disclaimer be submitted. During the phone conference Examiner Nguyen indicated that he would like to have a new power of attorney, the details of which were discussed.

Attached herewith is a new power of attorney based on the discussions with Examiner Nguyen. Also attached is a new terminal disclaimer. In October 16, 2009, office action the Examiner noted that a timely filed terminal disclaimer may be used to overcome the non-statutory double patenting rejection. The Examiner noted that the power of attorney was one of the older types which was in use some years ago and named more than ten practitioners in the power of attorney. Accordingly, applicants were referred to MPEP Sections 402 and 403 to correct the problem.

Applicants' attorney has reviewed Sections 402 and 403 and in particular the first part of Section 402 which refers to 37 CFR 1.32(c)(3) and Section 403.01. Sub-part (3) of 37 CFR 1.32(c) indicates that a separate paper should be included which states which of the practitioners named in the power of attorney to be recognized by the Office as being of record in the application to which the power is directed. Further, MPEP 403.01 authorized an attorney appointed by an associate power of attorney to file such a request for associate powers dated before June 25, 2004. Accordingly, such a paper is included herewith.

The new Power of Attorney, attached, makes clear that only three persons are to be recognized as being of record in the application. Among those which are recognized in the application is David V. Carlson, who is signing the terminal disclaimer attached. Accordingly, it is believed that this terminal disclaimer attached can be validly entered in the present application. A chain of documents showing that the undersigned, David V. Carlson, has the power of attorney to file these papers is also attached, which included the power of attorney from Lisa K. Jorgenson, also attached.

These documents are believed to fully comply with 37 C.F.R. 1.32(c)(3) and also are according to the instructions from the MPEP, sections cited above. If the Examiner believes that this approach is not correct, he is invited to call applicants' attorney at the number listed below to provide specific instructions as to the preferred course of action. Having reviewed MPEP Sections 402 and 403, it is believed that the present submission should be acceptable to

satisfy the Examiner's request, and for this reason issuance of the patent to allowance is respectfully requested.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

DVC:lch

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1587934_1.DOC

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 96-S-012C4 (850063.553C4)

In re Application of: Jefferson Eugene Owen

Application No.: 12/424,389

Filed: April 15, 2009

For: ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

The owner*, STMicroelectronics, Inc. of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** Nos. 7,321,368 and 7,542,045 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Registration No. 31,153

/David V. Carlson/	March 24, 2010
Signature	Date

David V. Carlson
Typed or printed name

(206) 622-4900
Telephone Number

☐ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this statement. See MPEP § 324.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. 1587931_1.DOC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Jefferson Eugene Owen et al.
Application No.	:	12/424,389
Filed	:	April 15, 2009
For	:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
Examiner	:	Hau H. Nguyen
Art Unit	:	2628
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	March 24, 2010

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NEW POWER OF ATTORNEY

UNDER 37 CFR 1.32(c)(3)

Commissioner for Patents:

In accordance with 37 CFR 1.32(c)(3) and MPEP 403.01, applicants hereby state that the attorneys to be recognized by the Office as being of record in the application are the following individuals:

David V. Carlson – Reg. No. 31,153

Lisa K. Jorgenson – Reg. No. 34,845

E. Russell Tarleton – Reg. No. 31,800

The above statement is made based on the power of attorney provided to Lisa K. Jorgenson in August of 1996 and her subsequent appointment of an associate power of attorney on April 12, 1999 which includes all of the individuals listed above.

A copy of the power of attorney and appointment of the associate power is provided as set forth in MPEP 402. A copy of the associate power of attorney and the authority to file this request is set forth in MPEP 403.01, which has been followed.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/
David V. Carlson
Registration No. 31,153

Enclosure:
Copy of Declaration and Power of Attorney

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

1587930_1.DOC

This Declaration copy is intended for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name,

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Video and/or Audio Decompression and/or Compression Device that Shares a Memory

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

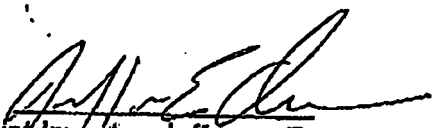
I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Lisa K. Jorgenson, Reg. No. 34,845 and Irena Lager, Reg. No. 39,260 to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

Please send all correspondence to:

Lisa K. Jorgenson
Reg. No. 34,845
SGS-Thomson Microelectronics, Inc.
1310 Electronics Drive
Carrollton, TX 75006
(214) 466-7414

Inventor's Signature: 
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: Aug 22, 1996
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
98B Escondido Village
Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: Raul Zegers Diaz
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: 8/20/96
Residence and Post Office Address:
~~98B Escondido Village~~
~~Stanford, CA 94305~~ 750 ~~E~~ Montrose Avenue #23
Palo Alto, CA 94303

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: _____
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

Inventor's Signature: _____
Full Name of First Joint Inventor: Jefferson Eugene Owen
Date of Signature: _____
Residence and Post Office Address:
44177 Bowers Court
Freemont, CA 94539

Citizenship: United States of America

Inventor's Signature: _____
Full Name of Second Joint Inventor: Raul Zegers Diaz
Date of Signature: _____
Residence and Post Office Address:
98B Escondido Village
Stanford, CA 94305

Citizenship: United States of America

Inventor's Signature: Flavio Osvaldo
Full Name of Third Joint Inventor: Osvaldo Colavin
Date of Signature: August 19, 1996
Residence and Post Office Address:
2820 Livsey Court
Tucker, Georgia 30084

Citizenship: France

This Power of Atto. , copy is intended for the attached Continuation application being submitted on April 15, 2009, attorney docket no 850063.553C4.

IN THE UNITE STATES PATENT AND TRADEMA. OFFICE

Applicants	:	Jefferson E. Owen et al.
Application No.	:	08/702,910
Filed	:	August 26, 1996
For	:	VIDEO AND/OR AUDIO DECOMPRESSION AND/OR COMPRESSION DEVICE THAT SHARES A MEMORY
Examiner	:	Glenn Gossage
Art Unit	:	2751
Docket No.	:	96-S-12 (850063.553)
Date	:	April 12, 1999

Assistant Commissioner for Patents
Washington, DC 20231

APPOINTMENT OF ASSOCIATE POWER OF ATTORNEY

Sir:

I, Lisa K. Jorgenson, attorney of record in the above-identified application, appoint as associate attorneys David V. Carlson, Reg. No. 31,153; Michael J. Donohue, Registration No. 35,859, Kevin S. Ross, Reg. No. 42,116; Dale C. Barr, Reg. No. 40,498; Kevin S. Costanza, Reg. No. 37,801, Brian L. Johnson, Reg. No. 40,033, Paul F. Rusyn, Reg. No. 42,118, Dennis M. de Guzman, Reg. No. 41,702; E. Russell Tarleton, Reg. No. 31,800, John M. Wechkin, Reg. No. 42,216; Robert D. McCutcheon, Reg. No. 38,717; and Theodore E. Galanthay, Reg. No. 24,122.

It is requested that correspondence continue to be addressed to Lisa K. Jorgenson at:

Lisa K. Jorgenson, Esq.
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006-5039

Respectfully submitted,
STMicroelectronics, Inc.

Lisa K. Jorgenson
Lisa K. Jorgenson
Registration No. 34,845

LKJ:BLJ:jab1

1310 Electronics Drive
Carrollton, Texas 75006-5039
(972) 466-7414
Fax: (972) 466-7044-5039

u:\float\jab1\850063.553-Assocpoa

Electronic Acknowledgement Receipt

EFS ID:	7279908
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Laura Hernandez
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	24-MAR-2010
Filing Date:	15-APR-2009
Time Stamp:	19:12:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		553C4_RESPONSE.pdf	53145 fad5347be29b1d52f9f239b5640e29edd4bcd76c	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Applicant Arguments/Remarks Made in an Amendment	2	3

Warnings:					
Information:					
2	Terminal Disclaimer Filed	553C4_TERMINAL_DIS.pdf	81641 c856685cb825e2696933e02e7e7c39e5f4a54d9f	no	1
Warnings:					
Information:					
3	Power of Attorney	553C4_NEW_POA.pdf	215297 b38f1e982f485bddbccb877c5dffbf9259b011ff	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	350083		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/424,389	04/15/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/24/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/BONNIE PHOENIX/

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/424,389	04/15/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/24/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/BONNIE PHOENIX/

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/424,389	OWEN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 3/24/10	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

Felicia D. Roberts

7,321,368 and 7,542,045

U.S. Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

30423 7590 04/09/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/09/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)	1455

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/09/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

30423 7590 04/09/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)	1455

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/09/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HAU H	2628	345-531000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)	1455

30423 7590 04/09/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/09/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/424,389	OWEN ET AL.	
	Examiner	Art Unit	
	HAU H. NGUYEN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *1/15/2010*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Hau H Nguyen/
Primary Examiner, Art Unit 2628

Allowable Subject Matter

1. Claims 1-17 are allowed.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

The prior art taken singly or in combination does not teach or suggest, an electronics system, *among other things*, comprising:

an arbiter circuit coupled to the processor and to the video circuit, the arbiter circuit configured to receive requests for access to the main memory from the video circuit and the processor and to control access to the main memory by:

providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state;

queuing a request for access to the main memory when the arbiter circuit is in a busy state; and

queuing a request for access to the main memory in an order based on a priority of the request and a priority of each of one or more other requests for access to the main memory that are currently queued when the arbiter circuit is in a queue state (claim 1);

an arbiter included in the memory interface circuit of the decoder and coupled to the memory interface circuit of the central processing unit, the arbiter configured to control access to the memory by determining a priority for requests to access the memory, each of the requests received from one of the decoder and the central processing unit, and providing access to the memory based on the determined priorities of the requests (claim 7);

for each of multiple requests for access to the shared memory received from the video decoder and one or more other devices, providing access to the shared memory for the request when the shared memory is not being accessed and no other requests to access the shared memory are currently pending;

queuing the request when the shared memory is being accessed; and

queuing the request in an order based on a priority of the request and a priority of each of one or more other requests that are currently pending when the shared memory is being accessed and the one or more other requests are currently pending (claim 13).

The closest prior art, Normile et al. (U.S Patent No. 5,461,679) in view of Gulick et al. (U.S. Patent No. 5,797,028) fails to teach the above features.

Conclusion

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12424389	OWEN ET AL.
	Examiner	**Art Unit**
	HAU H NGUYEN	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	04/05/2010								
	1	=								
	2	=								
	3	=								
	4	=								
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	16	=								
	17	=								

UNITED STATES PATENT AND TRADEMARK OFFICE

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BIB DATA SHEET

CONFIRMATION NO. 1455

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/424,389	04/15/2009	345	2628	96-S-012C4 (850063.553C4)

APPLICANTS

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Stanford, CA;
Osvaldo Colavin, Tucker, GA;

**** CONTINUING DATA ***************************

This application is a CON of 11/956,165 12/13/2007 PAT 7,542,045
which is a CON of 10/174,918 06/19/2002 PAT 7,321,368
which is a CON of 09/539,729 03/30/2000 PAT 6,427,194
which is a CON of 08/702,910 08/26/1996 PAT 6,058,459

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/01/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /HAU H NGUYEN/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	17	3

ADDRESS

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006
UNITED STATES

TITLE

ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	284	(decod$3 with (image frame) with (current and previous)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 18:58
L2	65	((arbiter arbitrat $3) with video with memory).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 18:59
L3	0	1 and 2	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 18:59
L4	793	(decod$3 with (image frame) near3 current).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:01
L5	4	2 and 4	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:01
L6	6369	(queu$3 with request).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:03
L7	6711	(priority with request).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:03
L8	1	4 and 6 and 7	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:03
L9	1118	6 and 7	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:03
L10	180	(request$3 with video near3 decod $3).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:04
L11	4	7 and 10	US-PGPUB; USPAT; UPAD	OR	ON	2010/04/05 19:05

4/5/10 7:05:53 PM
C:\Documents and Settings\HNguyen23\My Documents\EAST\workspaces\12_424389.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S128	104	S119 and S127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:49
S127	144481	access$3 with bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:49
S126	23	S119 and S125	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:47
S125	38578	(queue$3 fifo) with request	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:47
S124	12	S119 and S120	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:46
S123	1	(10/174918).APP.	USPAT; USOCR	OR	ON	2010/04/05 14:44
S122	4	S119 and S120 and S121	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:40
S121	26693	non adj image	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:40
S120	37396	priority with request	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:39

S119	1378	decod$3 with (current and previous) near2 (frame image)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 14:37
S118	12	S116 and S117	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 13:36
S117	1798	(arbiter arbitrat$3) with idle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 13:36
S116	378	(video near2 decod$3) with arbit$6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 11:00
S115	38	("4257095" | "4774660" | "4894565" | "5027400" | "5212742" | "5250940" | "5363500" | "5371893" | "5450542" | "5459519" | "5461679" | "5522080" | "5557538" | "5576765" | "5579052" | "5590252" | "5598525" | "5621893" | "5623672" | "5682484" | "5748203" | "5774206" | "5774676" | "5778096" | "5793384" | "5797028" | "5809245" | "5809538" | "5812789" | "5815167" | "5835082" | "5912676" | "5923665" | "5936616" | "5960464" | "6058459" | "6297832" | "6330644").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2010/04/05 10:56
S113	177	S111 and S112	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 10:52
S112	15243	memory near2 (main host system) with video	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 10:52

S111	399	S108 and S109 and S110	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 10:51
S110	6902	(arbiter arbitrat$3) with (cpu ((host main system) near2 processor) microprocessor)	US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB	OR	ON	2010/04/05 10:51
S109	81117	video with decod$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 10:50
S108	404320	memory near2 (main host system)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/05 10:49

4/5/10 6:56:46 PM
C:\Documents and Settings\HNguyen23\My Documents\EAST\workspaces\12_424389.wsp

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
12424389	OWEN ET AL.
Examiner	**Art Unit**
HAU H NGUYEN	2628

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
345	541	G 0 6 F 15 / 167 (2006.01.01)	
CROSS REFERENCE(S)		G 0 9 G 5 / 36 (2006.01.01)	
		G 0 9 G 5 / 39 (2006.01.01)	

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
345	542	531	547		

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	17	
/HAU H NGUYEN/ Primary Examiner.Art Unit 2628	04/05/2010	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12424389	OWEN ET AL.
	Examiner	Art Unit
	HAU H NGUYEN	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	541, 531, 542, 547, 555, 501, 519, 545	4/5/10	HN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Search US-PGPUB; USPAT; FPRS; EPO; JPO; IBM_TDB text search attached	4/5/10	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
345	541, 542, 531, 547	4/5/10	HN

	/HAU H NGUYEN/ Primary Examiner.Art Unit 2628

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

30423 7590 04/09/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	04/15/2009	Jefferson Eugene Owen	96-8-012C4 (STMI03-53804)	1455

TITLE OF INVENTION: ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	07/09/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HAU H	2628	345-531000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lisa K. Jorgenson
2 David V. Carlson
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: STMicroelectronics, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Carrollton, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☒ Publication Fee (No small entity discount permitted)

☒ Advance Order - # of Copies 1

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-1353 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature [signature] Date 3/3/2010

Typed or printed name Patrick C.R. Holmes Registration No. 46,380

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	12424389
Filing Date:	15-Apr-2009
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	Patrick C.R. Holmes/Angie Rodriguez
Attorney Docket Number:	96-S-012C4 (850063.553C4)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	1	3	3
		Total in USD ($)		**1813**

Electronic Acknowledgement Receipt

EFS ID:	7965641
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	Patrick C.R. Holmes/Angie Rodriguez
Filer Authorized By:	Patrick C.R. Holmes
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	07-JUL-2010
Filing Date:	15-APR-2009
Time Stamp:	13:16:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1813
RAM confirmation Number	12718
Deposit Account	191353
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	**Document Description**	**File Name**	**File Size(Bytes)/ Message Digest**	**Multi Part /.zip**	**Pages (if appl.)**
1	Issue Fee Payment (PTO-85B)	96-S-012C4.pdf	388652 b46eca336eb5cf4d15a5d84d73cd7887723df3e4	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	34018 edf4c04672a0f392f9f9159a9213219583ef7234	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	422670		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/424,389	08/17/2010	7777753	96-S-012C4 (850063.553C4)	1455

30423 7590 07/28/2010

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jefferson Eugene Owen, Freemont, CA;
Raul Zegers Diaz, Stanford, CA;
Osvaldo Colavin, Tucker, GA;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	7,777,753 B2
Issue Date	:	August 17, 2010
Inventors	:	Jefferson Eugene Owen et al.
Docket No.	:	96-S-012C4 (850063.553C4)
Date	:	August 26, 2010

Mail Stop Certificate of Correction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents:

A certificate of correction is respectfully requested in the above-identified patent. The following errors have been made:

Item (56) References Cited, Foreign Patent Documents, the reference, "EP 0827110 9/1998" is incorrect. As set forth in the Information Disclosure Statement filed with the United States Patent & Trademark Office on August 28, 2009, the correct reference should read, -- EP 0827110 3/1998 --.

In the claims, column 16, issued claim 9, line 53, "for a request received from the encoder when the request" is incorrect. The correct line should read, -- for a request received from the decoder when the request --.

In the claims, column 18, issued claim 15, line 16, "shared memory for a request received from the video encoder" is incorrect. The correct line should read, -- shared memory for a request received from the video decoder --.

The errors are of a clerical nature, are of minor character, would not constitute new matter or require reexamination, and were made in good faith.

Attached is the certificate of correction, which indicates the corrections to be made, by reference to the item or column and line numbers in the printed patent. The Director is hereby authorized to charge payment of any fees associated with this communication to Deposit Account No. 19-1090.

Respectfully submitted,
SEED Intellectual Property Law Group PLLC

David V. Carlson
Registration No. 31,153

DVC:djs

Enclosures:
Certificate of Correction

SEED Intellectual Property Law Group PLLC
701 Fifth Avenue, Suite 5400
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

1693138_1.DOCX

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,777,753 B2
DATED : August 17, 2010
INVENTOR : Jefferson Eugene Owen et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Item 56

"EP 0827110 9/1998" should read -- EP 0827110 3/1998 --.

Column 16, Line 53

"for a request received from the encoder when the request" should read -- for a request received from the decoder when the request --.

Column 18, Line 16

"shared memory for a request received from the video encoder" should read -- shared memory for a request received from a video decoder --.

MAILING ADDRESS OF SENDER:

David V. Carlson
Seed Intellectual Property Law Group PLLC
701 Fifth Avenue, Suite 5400
Seattle, Washington 98104

PATENT NO. 7,777,753 B2

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1693146_1.DOCX

Electronic Patent Application Fee Transmittal

Application Number:	12424389
Filing Date:	15-Apr-2009
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Filer:	David V. Carlson/Donald Saunderson
Attorney Docket Number:	96-S-012C4 (850063.553C4)

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Certificate of correction	1811	1	100	100
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**100**

Electronic Acknowledgement Receipt

EFS ID:	8301424
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Donald Saunderson
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	26-AUG-2010
Filing Date:	15-APR-2009
Time Stamp:	17:11:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$100
RAM confirmation Number	3970
Deposit Account	191090
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Certificate of Correction	850063_553C4_Request_for_Certificate_of_Correction.pdf	90833 328c541ea91678c606694180f6c5fccdc04c0a3c	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30370 d9ddedbb873e43037c847a491cdb8e9ee9bce004	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	121203		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,777,753 B2
APPLICATION NO. : 12/424389
DATED : August 17, 2010
INVENTOR(S) : Jefferson Eugene Owen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

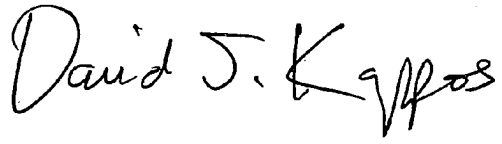
Title Page, Item 56 For. Pat. Doc.:
"EP 0827110 9/1998" should read -- EP 0827110 3/1998 --.

Column 16, Line 53
"for a request received from the encoder when the request" should read -- for a request received from the decoder when the request --.

Column 18, Line 16
"shared memory for a request received from the video encoder" should read -- shared memory for a request received from a video decoder --.

Signed and Sealed this

Twenty-eighth Day of September, 2010



David J. Kappos
Director of the United States Patent and Trademark Office

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	SOLICITOR JUN 23 2014 U.S. PATENT & TRADEMARK OFFICE

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00691	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	LG Electronics, Inc. and LG Electronics USA, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,542,045		
2 7,777,753		
3 8,054,315		
4 8,681,164		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00690	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	HTC Corporation and HTC America Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00689	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Motorola Mobility, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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4 8,681,164		
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AO 120 (Rev. 08/10)

SOLICITOR

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

JUN 23 2014
U.S. PATENT & TRADEMARK OFFICE

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00687	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Huawei Technologies Co., LTD, Huawei Technologies USA, Inc., and Huawei Device USA, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

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☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00930	10/1/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above--entitled case, the following patent(s)/ trademark(s) have been included:

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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2 7,777,753		
3 6,054,315		
4 8,681,164		
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DECISION/JUDGEMENT

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Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00902	9/22/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Samsung Electronics Co., LTD., Samsung Electronics America, Inc., and Samsung Telecommunications America LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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2 7,777,753		
3 8,054,315		
4 8,681,164		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:15-cv-00621	5/1/2015	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Apple Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC
4	7,542,045	6/2/2009	Parthenon Unified Memory Architecture LLC
5	7,777,753	8/17/2010	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 **CONTINUATION**

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6 8,054,315	11/8/2011	Parthenon Unified Memory Architecture LLC
7 8,681,164	3/25/2014	Parthenon Unified Memory Architecture LLC

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC AMERICA INC., HTC CORP., LG ELECTRONICS, INC.,
LG ELECTRONICS U.S.A., INC.,
LG ELECTRONICS MOBILECOMM U.S.A., INC.,
SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC
Patent Owner.

Case IPR2015-01501
Patent 7,777,753

Mailed: July 8, 2015

Before KAREN HILASKI, *Trial Paralegal*

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC's
MANDATORY NOTICES UNDER 37 C.F.R. 42.8(a)(2)

Patent Owner, Parthenon Unified Memory Architecture LLC, hereby files mandatory notices pursuant to 37 C.F.R. § 42.8(a)(2).

A. Real Party-In-Interest (37 C.F.R. § 42.8 (b)(1))

Parthenon Unified Memory Architecture LLC is the owner of the entire interest in U.S. Patent No. 7,777,753 ("the '753 Patent"), and thus is a real-party-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The Patent Owner identifies the following judicial and/or administrative matters that may affect, or may be affected by, a decision in this *Inter Partes* Review:

The '753 Patent is asserted by the Patent Owner in the following pending litigations in the U.S. District Court for the Eastern District of Texas: *Parthenon Unified Memory Architecture LLC v. Huawei Techs. Co., Ltd. et al.*, No. 2:14-cv-00687-JRG-RSP (E.D. Tex.) filed June 12, 2014; *Parthenon Unified Memory Architecture LLC v. Motorola Mobility, Inc.*, No. 2:14-cv-00689-JRG-RSP (E.D. Tex.) filed June 12, 2014; *Parthenon Unified Memory Architecture LLC v. HTC Corp. et al.*, No. 2:14-cv-00690-RSP (E.D. Tex.) filed June 12, 2014; *Parthenon Unified Memory Architecture LLC v. LG Elecs., Inc. et al.*, No. 2:14-cv-00691-JRG-RSP (E.D. Tex.) filed June 12, 2014; *Parthenon Unified Memory Architecture LLC v. Samsung Elecs. Co., Ltd. et al.*, No. 2:14-cv-00902-JRG-RSP (E.D. Tex.) filed September 22, 2014; *Parthenon Unified Memory Architecture*

LLC v. Qualcomm Inc. et al., No. 2:14-cv-00930-JRG-RSP (E.D. Tex.) filed October 1, 2014; *Parthenon Unified Memory Architecture LLC v. ZTE Corp. et al.*, No. 2:15-cv-00225-JRG-RSP (E.D. Tex.) filed February 17, 2015; and *Parthenon Unified Memory Architecture LLC v. Apple, Inc.*, No. 2:15-cv-00621-JRG-RSP (E.D. Tex) filed May 1, 2015.

Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

Patent Owner designates the following counsel:

Lead Counsel	Back-Up Counsel
Alisa Lipski Registration No. 55,386 (alipski@azalaw.com) Telephone: 713-655-1101	Amir Alavi Pending *Pro Hac Vice* Motion (aalavi@azalaw.com)

Address: AHMAD, ZAVITSANOS, ANAIPAKOS, ALAVI & MENSING P.C.
1221 McKinney, Suite 3460
Houston, TX 77010
(713) 655-1101 (Reception)
(713) 655-0062 (Facsimile)

C. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence regarding this proceeding to the counsel at the address listed above. Patent owner also consents to electronic service by email to the e-mail address listed above.

Respectfully Submitted,

Dated: July 15, 2015

By: */s/ Alisa Lipski*
Alisa Lipski
Reg. No. 55,386
Attorney for Patent Owner
Parthenon Unified Memory Architecture, LLC

AHMAD, ZAVITSANOS, ANAIPAKOS, ALAVI & MENSING, P.C.
1221 McKinney Street, Suite 3460
Houston, TX 77010
Telephone: 713-655-1101

CERTIFICATE OF SERVICE

I hereby certify that Parthenon Unified Memory Architecture LLC's Mandatory Notices Under 37 C.F.R. 42.8(a)(2) were served on July 15, 2015, by electronic mail to the following:

Lead Counsel for LG Electronics, Inc.	Back-up Counsel for LG Electronics, Inc.
Rajeev Gupta Reg. No. 55,873 Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. 901 New York Avenue, N.W. Washington, D.C. 20001-4413 Tel: (202) 408-4000 Fax: (202) 408-4400 Email: raj.gupta@finnegan.com	Darren M. Jiron Reg. No. 45,777 Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. 11955 Freedom Drive Reston, VA 20190-5675 Tel: (571) 203-2700 Fax: (202) 408-4400 Email: Darren.jiron@finnegan.com
Lead Counsel for HTC Corporation	Back-up Counsel for HTC Corporation
Joseph A. Micallef Reg. No. 39,772 Sidley Austin LLP 1501 K Street, N.W. Washington, DC 20005 Tel: (202) 736-8492 Email: jmicallef@sidley.com	Cameron A. Zinsli Reg. No. 70,028 Sidley Austin LLP 555 California Street, Suite 2000 San Francisco, CA 94104 Tel: (415) 772-7482 Email: czinsli@sidley.com
Lead Counsel for Samsung Electronics	Back-up Counsel for Samsung Electronics
Allan M. Soobert Reg. No. 36,284 Paul Hastings LLP 875 15th Street NW Washington, DC 20005 Tel: (202) 551-1990 Fax: (202)551-0490 Email: Samsung-PUMA-IPR@paulhastings.com	Naveen Modi Reg. No. 46,224 Paul Hastings LLP 875 15th Street NW Washington, DC 20005 Tel: (202) 551-1990 Fax: (202)551-0490 Email: Samsung-PUMA-IPR@paulhastings.com

Dated: July 15, 2015

By: */s/ Alisa Lipski*
Alisa Lipski
Reg. No. 55,386
Attorney for Patent Owner
Parthenon Unified Memory Architecture, LLC

AHMAD, ZAVITSANOS, ANAIPAKOS, ALAVI &MENSING, P.C.
1221 McKinney Street, Suite 3460
Houston, TX 77010
Telephone: 713-655-1101

4829-8170-2949, v. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC AMERICA INC., HTC CORP., LG ELECTRONICS, INC.,
LG ELECTRONICS U.S.A., INC.,
LG ELECTRONICS MOBILECOMM U.S.A., INC.,
SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC
Patent Owner.

Case IPR2015-01501
Patent 7,777,753

Mailed: July 8, 2015

Before KAREN HILASKI, *Trial Paralegal*

POWER OF ATTORNEY PURSUANT TO 37 C.F. R. § 42.10(b)

Pursuant to 37 C.F.R. § 42.10(b), Patent Owner, Parthenon Unified Memory Architecture LLC hereby appoints Alisa Lipski of AHMAD, ZAVITSANOS, ANAIPAKOS, ALAVI & MENSING P.C. as its attorney to transact all business in the United States Patent & Trademark Office and Patent Trial and Appeal Board associated with the above captioned *inter partes* review:

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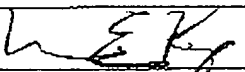
I am authorized to sign this document on behalf of the Patent Owner, Parthenon Unified Memory Architecture LLC.

FOR: Parthenon Unified Memory Architecture LLC

SIGNATURE: 

BY: Marvin E Key

TITLE: CEO

DATE: July 14, 2015

CERTIFICATE OF SERVICE

I hereby certify that Parthenon Unified Memory Architecture LLC's Power of Attorney Pursuant to 37 C.F.R. 42.10(b) was served on this Wednesday, July 15, 2015 by electronic mail to the following:

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Dated: July 15, 2015

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4813-6492-9829, v. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/424,389	04/15/2009	Jefferson Eugene Owen	96-S-012C4 (850063.553C4)

CONFIRMATION NO. 1455

OC000000076552506

30423
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Date Mailed: 07/29/2015

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed 07/15/2015 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☑ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(b) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____, a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.

Questions relating to this Notice should be directed to the Application Assistance Unit.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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MISCELLANEOUS NOTICE

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Date Mailed: 07/30/2015

A communication which cannot be delivered in electronic form has been mailed to the applicant.

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571-272-7822

Paper 12
Entered: January 6, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HTC CORPORATION,
HTC AMERICA, INC.,
LG ELECTRONICS, INC.,
SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioner,

v.

PARTHENON UNIFIED MEMORY ARCHITECTURE LLC,
Patent Owner.

Case IPR2015-01501
Patent 7,777,753 B2

Before JAMES B. ARPIN, MATTHEW R. CLEMENTS, and SUSAN L. C. MITCHELL, *Administrative Patent Judges*.

ARPIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

HTC Corporation; HTC America, Inc.; LG Electronics, Inc.; Samsung Electronics Co., Ltd.; and Samsung Electronics America, Inc. (collectively, "Petitioner") filed a Petition requesting *inter partes* review of claims 1–4, 7–10, and 12 ("the challenged claims") of Patent No. US 7,777,753 B2 (Ex. 1001, "the '753 patent"). Paper 1 ("Pet."). Parthenon Unified Memory Architecture LLC ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, and the accompanying evidence, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '753 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1–4 of the '753 patent.

A. Related Proceedings

The '753 patent is involved in several cases pending in the Eastern District of Texas. Pet. 2–3; Paper 5, 2–3. Petitioner also has filed other petitions seeking *inter partes* review of related patents. Pet. 3.

B. The '753 patent

The '753 patent relates generally "to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system." Ex. 1001, col. 1, ll. 36–41. As of the effective filing date of the '753 patent,[1] a typical decoder included a dedicated memory, which represented a significant percentage of the cost of the decoder and which went unused most of the time. *Id.* at col. 2, ll. 21–63, col. 4, ll. 43–60, Figs. 1a–1c.

To address these and other concerns, the '753 patent discloses an electronic system in which a first device and a video and/or audio decompression and/or compression device are coupled to a shared memory through a bus that may have bandwidth sufficient for the video and/or audio decompression and/or compression device to operate in real time. *Id.* at col. 4, l. 64–col. 5, l. 7. Figure 2 is reproduced below.

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[1] The '753 patent claims the benefit of a string of earlier-filed U.S. patent applications, the earliest of which was filed on August 26, 1996. Petitioner does not challenge the entitlement of the '753 patent to this earliest filing date and argues that the '753 patent will expire in August of 2016, presumably based on this earliest filing date. Pet. 10–11. Patent Owner implicitly claims the entitlement of the '753 patent to the benefit of this earliest filing date and expressly states that the '753 patent will expire on August 26, 2016. Paper 8, 1.

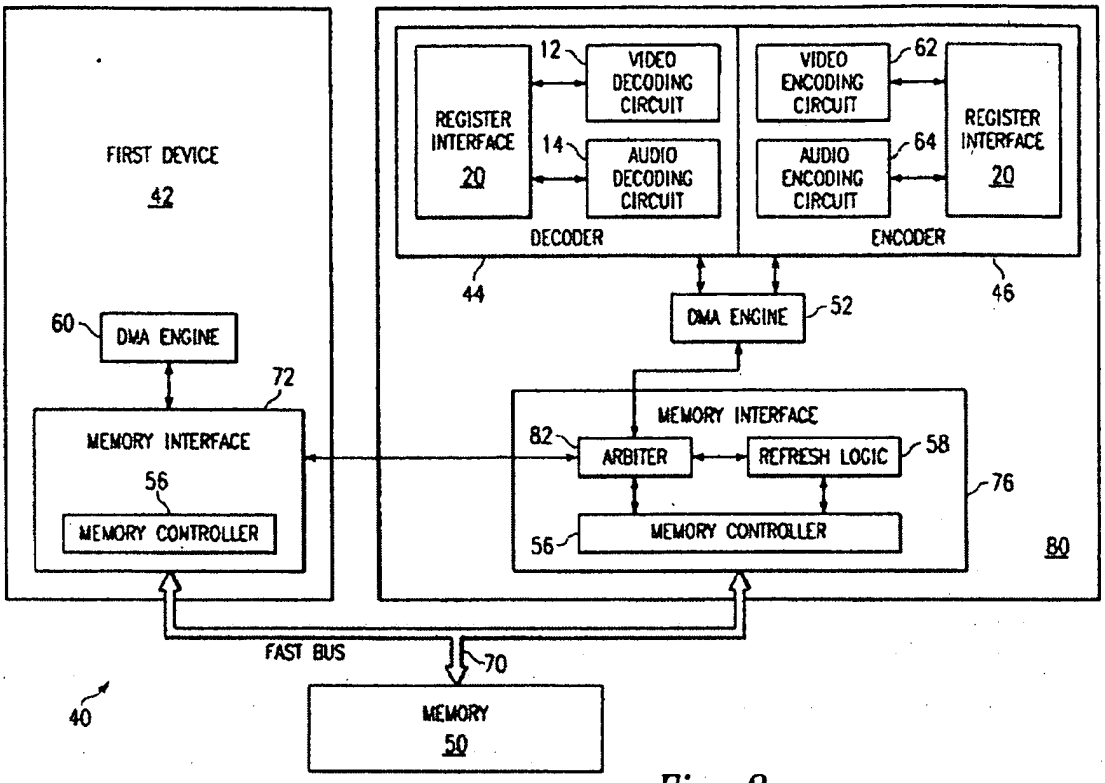

Fig. 2

Figure 2 is a block diagram of an electronic system that contains a device with a memory interface and an encoder and decoder. *Id.* at col. 6, ll. 3–5. "First device 42 can be a processor, a core logic chipset, a graphics accelerator, or any other device that requires access to the memory 50." *Id.* at col. 6, ll. 29–32. Both first device 42 and decoder/encoder 80 have access to memory 50 through memory interfaces 72 and 76, respectively, coupled to fast bus 70. *Id.* at col. 6, ll. 27–29, col. 7, ll. 26–28, 48–51. Fast bus 70 may have at least the bandwidth required for decoder/encoder 80 to operate in real time and, preferably, has a bandwidth of at least approximately twice the bandwidth required for decoder/encoder 80 to operate in real time. *Id.* at col. 7, ll. 48–51, col. 8, ll. 28–33.

During operation, decoder/encoder 80, first device 42, and refresh logic 58, if it is present, request access to memory 50 through arbiter 82. *Id.*

at col. 12, ll. 53–56. Arbiter 82 determines which of the devices may access memory 50. *Id.* at col. 12, ll. 57–58. Decoder/encoder 80 may get access to memory 50 in the first time interval, and first device 42 may get access to memory 50 in the second time interval. *Id.* at col. 12, ll. 58–61. Direct Memory Access (DMA) engine 52 of decoder/encoder 80 determines the priority of decoder/encoder 80 for access to memory 50 and the burst length when decoder/encoder 80 has access to memory 50. *Id.* at col. 12, ll. 61–67. DMA engine 60 of first device 42 determines its priority for access to memory 50 and the burst length when first device 42 has access to memory 50. *Id.* at col. 12, ll. 65–67.

When decoder/encoder 80 or one of the other devices generates a request to access memory 50, the request is transferred to arbiter 82, and access to memory 50 is determined based on the state of arbiter 82 and on a priority scheme. *Id.* at col. 13, ll. 1–30. In particular,

> The state of the arbiter 82 is determined. The arbiter typically has three states. *The first state is idle* when there is no device accessing the memory and there are no requests to access the memory. *The second state is busy* when there is a device accessing the memory and there is no other request to access the memory. *The third state is queue* when there is a device accessing the memory and there is another request to access the memory.

Id. at col. 13, ll. 3–10 (emphases added). The priority scheme can be any scheme that ensures decoder/encoder 80 gets access to memory 50 often enough to operate properly, but does not starve entirely other devices sharing memory 50. *Id.* at col. 13, ll. 31–37; *see id.* at col. 8, ll. 9–13 (describing a "starvation period").

C. Illustrative Claim

Of the challenged claims, claims 1 and 7 are independent. Ex. 1001, col. 15, ll. 32–59 (claim 1), col. 16, ll. 15–36 (claim 7). Claims 2–4 depend directly from claim 1, and claims 8–10 and 12 depend directly from claim 7. *Id.* at col. 15, l. 60–col. 16, l. 9, col. 16, ll. 37–59, 62–63. Claim 1 is illustrative and is reproduced below:

> 1. An electronic system comprising:
>
> a bus;
>
> a main memory coupled to the bus having stored therein data corresponding to video images;
>
> a video circuit coupled to the bus, the video circuit configured to receive data from the main memory corresponding to a current video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device, the current video image to be displayed adapted to be stored in the main memory;
>
> a processor coupled to the main memory, the processor for storing non-image data in the main memory and retrieving non-image data from the main memory; and
>
> an arbiter circuit coupled to the processor and to the video circuit, the arbiter circuit configured to receive requests for access to the main memory from the video circuit and the processor and to control access to the main memory by:
>
> providing access to the main memory for a request for access to the main memory when the arbiter circuit is in an idle state;
>
> queuing a request for access to the main memory when the arbiter circuit is in a busy state; and
>
> queuing a request for access to the main memory in an order based on a priority of the request and a priority of each of one or more other requests for access to the main memory that are currently queued when the arbiter circuit is in a queue state.

Ex. 1001, col. 15, ll. 32–59.

D. Applied References and Declarations

Petitioner relies upon the following references and declarations in support of its grounds for challenging the identified claims of the '753 patent:[2]

Exhibit	References and Declarations
1002	File History of Patent No. US 7,777,753 B2
1003	Patent No. US 5,546,547 ("Bowes")
1004	International Organization for Standardization, "ISO/IEC 11172-2: Information technology—Coding of moving pictures and associated audio for digital storage media at up to about 1,5 Mbit/s—Part 2: Video," (1st ed. Aug. 1, 1993) ("MPEG")
1006	Robert J. Gove, "The MVP: A Highly-Integrated Video Compression Chip," Proceedings of the IEEE Data Compression Conference (DCC '94), pp. 215–224 (March 29–31, 1994) ("Gove")
1007	Patent No. US 5,774,676 ("Stearns")
1008	Declaration of Santhana Chari, Ph.D.
1017	Patent No. US 5,748,983 ("Gulick")[3]
1018	International Patent Application Publication No. WO 96/11440, PCT/US95/12933 ("Whai")
1019	T. Shanley *et al.*, "PCI System Architecture," Addison-Wesley Publ'g Co. (3rd ed. Feb. 1995) ("Shanley")

[2] Our rules require that Petitioner number its exhibits "sequentially" in a range of 1001–1999. 37 C.F.R. § 42.63(c). By "reserving" Exhibit Nos. 1005, 1010–1013, 1015, 1016, 1021, 1022, and 1026–1028; Petitioner failed to follow this rule. Petitioner shall number all future exhibits sequentially starting with Exhibit No. 1031. We shall expunge any further exhibits filed by either party that are not numbered sequentially. 37 C.F.R. §§ 42.5(a), 42.7(a), and 24.12(a)(1) and (b)(2).

[3] Although Petitioner refers to this reference as "Gulick 983" (*see, e.g.*, Pet. vi), Patent Owner does not (*see, e.g.*, Prelim. Resp. 1). For consistency, we will refer to this reference only as "Gulick."

1020	H. Stone, "Microcomputer Interfacing," Addison-Welsey Publishing Co. (1982)
1030	Declaration of Harold S. Stone, Ph.D. (the "Stone Decl.")

Pet. vi–vii.

E. Asserted Grounds of Unpatentability

Petitioner argues that the challenged claims are unpatentable based on the following grounds (Pet. 5–6):

References	Basis	Claim(s) challenged
Gulick, MPEG, and Shanley	§ 103	1–4 and 7–10
Gulick, MPEG, Shanley, and Gove	§ 103	12
Bowes and MPEG	§ 103	1 and 2
Bowes, MPEG, and Stearns	§ 103	3
Bowes, MPEG, and Shanley	§ 103	4
Bowes, MPEG, and Whai	§ 103	7 and 8
Bowes, MPEG, Whai, and Shanley	§ 103	9 and 10
Bowes, MPEG, Whai, and Gove	§ 103	12

II. ANALYSIS

A. Claim Construction

Pursuant to 37 C.F.R. § 42.100(b), "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." Petitioner alleges that the '753 patent will expire in August of 2016. Pet. 10–11. Patent Owner states that the '753 patent will expire on August 26, 2016. Paper 8, 1. Thus, the '753 patent will expire before we are likely to issue a final written decision as to the patentability of the challenged claims.

Although Petitioner proposes a construction based on the broadest reasonable interpretation standard for one term, Petitioner argues that its

proposed construction will remain the same even if we apply the claim construction standard used by the U.S. district courts and set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). Pet. 11. Patent Owner proposes no construction for any term at this preliminary proceeding stage. In order to determine if Petitioner has demonstrated a reasonable likelihood that it will prevail in this initial proceeding, given the patent's pending expiration, we analyze Petitioner's arguments through the lens of the claim construction standard of *Phillips* that will apply to our final written decision. 37 C.F.R. §§ 42.5(b) and 42.100(b); *see Toyota Motor Corp. v. Cellport Sys., Inc.*, Case IPR2015-00633, slip op. at 8–10 (PTAB Aug. 14, 2015) (Paper 11); *cf. In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012) ("While claims are generally given their broadest possible scope during prosecution, the Board's review of the claims of an expired patent is similar to that of a district court's review.") (internal citation omitted).

"In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). The words of a claim generally are given their ordinary and customary meaning, and that is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *See Phillips*, 415 F.3d at 1312–13. Claims are not interpreted in a vacuum but are a part of and read in light of the specification. *See Slimfold Mfg. Co. v. Kinkead Indus., Inc.*, 810 F.2d 1113, 1116 (Fed. Cir. 1987). Although it is improper to read a limitation from the specification into the claims, the

claims still must be read in view of the specification of which they are a part. *See Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1347 (Fed. Cir. 2004).

1. "decoder"

Each of challenged claims 7, 8, and 12 recites a "decoder." *E.g.,* Ex. 1001, col. 16, ll. 18–25. Petitioner proposes to construe the term "decoder" to mean "hardware and/or software that translates data streams into video or audio information." Pet. 9–10 (citing Ex. 1001, col. 1, ll. 66–67 ("a video and/or audio decompression device (hereinafter 'decoder')"), col. 15, ll. 27–30 ("[a]ny conventional decoder complying to the MPEG-1, MPEG-2, H.261, or H.261 standards, or any combination of them, or any other conventional standard can be used as the decoder/encoder.")); *see Phillips*, 415 F.3d at 1312–13 (regarding a term's ordinary and customary meaning to a person of ordinary skill in the art, in the context of the entire patent, including the specification). Petitioner further relies upon a dictionary definition for "decoder" as evidence of the term's ordinary and customary meaning to a person of ordinary skill in the art as of the effective filing date of the '753 patent. *Id.* at 10 (citing Ex. 1014, 56 ("decoder (n). Any hardware or software system that translates data streams into video or audio information.").

In addition to its usage in the challenged claims, as noted above, the '753 patent uses the term "decoder" throughout the Specification. Moreover, we find nothing in the usage of the term "decoder" in dependent claim 8 or 12 that is inconsistent with the usage of the term elsewhere in the Specification of the '753 patent, with the dictionary definition of "decoder" in Exhibit 1014, or with the Petitioner's proposed construction. The '753

patent's definition of "decoder" to mean "a video and/or audio decompression device," and its disclosure that the "decoder/encoder" can be any conventional decoder complying to any conventional standard support a construction of "decoder" that encompasses both hardware and software, are persuasive of the term's proper construction, in the context of the entire '753 patent, including the Specification. *See, e.g.*, Ex. 1001, col. 1, ll. 66–67, col. 15, ll. 27–30.

Accordingly, on this record, and for purposes of this Decision, we adopt Petitioner's proposed construction of "decoder" as "hardware and/or software that translates data streams into video or audio information."[4]

2. Other Claim Terms

Petitioner offers no other constructions of any claim term in the challenged claims. *See* Pet. 8–11. Only terms which are in controversy in this proceeding need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). For purposes of this Decision, no other claim terms require express construction.

B. Obviousness

1. Overview

Petitioner argues that claims 1–4, 7–10, and 12 of the '753 patent are rendered obvious by Gulick, MPEG, and Shanley or Bowes and MPEG, alone or in combination with another reference. *See supra* Section I.E. A

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[4] On this record, we are persuaded that our construction of the term "decoder" set forth above would have been substantially the same had we applied the broadest reasonable interpretation standard.

patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are "such that the subject matter[,] as a whole[,] would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art;[5] and (4) objective evidence of nonobviousness, i.e., secondary considerations.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). On this record and for the reasons set forth below, we are persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 1–4 of the '753 patent are unpatentable.

2. Claims 1–4 and 7–10 — Obviousness over Gulick, MPEG, and Shanley (Ground A)

Petitioner argues that claims 1–4 and 7–10 are unpatentable under 35 U.S.C. § 103(a) as obvious over Gulick, MPEG, and Shanley. Pet. 12–36.

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[5] Petitioner proposes a definition for a person of ordinary skill in the art. Pet. 11 (citing Ex. 1030 ¶¶ 78–81). Patent Owner does not challenge Petitioner's proposed definition and does not propose an alternative. To the extent necessary and for purposes of this Decision, we adopt Petitioner's definition.

[6] Patent Owner does not contend in its Preliminary Response that such secondary considerations are present.

a. Gulick (Ex. 1017)

Gulick describes a computer system having a dedicated multimedia engine and multimedia memory having arbitration logic which grants main memory access to either the central processing unit (CPU) or the multimedia engine. Ex. 1017, Title, Abstract. Figure 1 of Gulick is reproduced below.

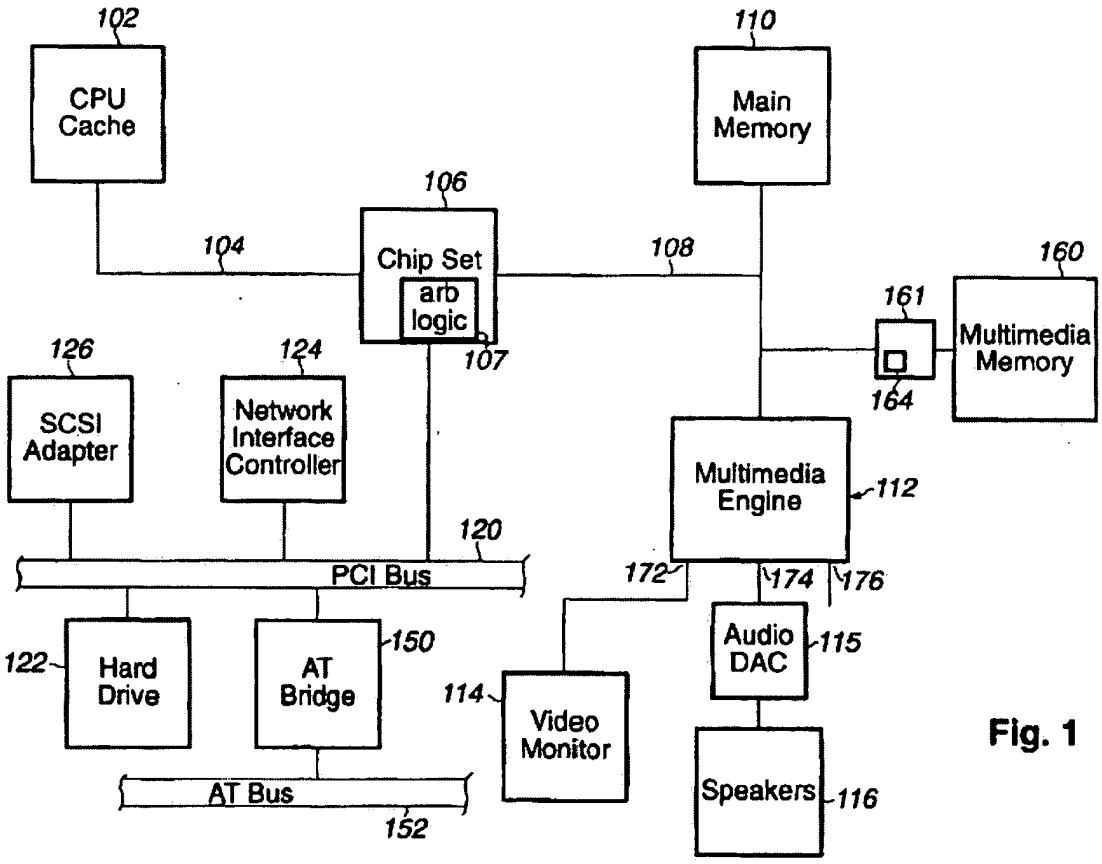

Fig. 1

Figure 1 is a block diagram of a computer system including main memory 110, multimedia engine 112, and multimedia memory 160. *Id.* at col. 3, ll. 29–31. The computer system includes CPU 102 coupled to chipset 106, which includes arbitration logic 107. *Id.* at col. 4, ll. 1–4. Chipset 106 is similar to known chipsets, but includes modifications to arbitration logic 107 in order to accommodate multimedia engine 112. *Id.* at col. 4, ll. 4–8.

Chipset 106 and main memory 110 couple to multimedia engine 112 through memory bus 108. *Id.* at col. 4, ll. 10–16.

Multimedia memory 160 also is coupled to memory bus 108 through arbitration block 161. *Id.* at col. 4, ll. 26–27. In a preferred embodiment, multimedia memory 160 is mapped to the main memory address space and, thus, is available to store non-multimedia data if, for example, main memory 110 becomes full and CPU 102 needs to store code and data. *Id.* at col. 4, ll. 31–40; *see id.* at col. 7, l. 65–col. 8, l. 3, Fig. 6; Pet. 13. Alternatively, multimedia memory 160 may be "comprised in the multimedia engine 112 instead of external to the multimedia engine 112." *Id.* at col. 6, ll. 4–7; *see id.* at Figs. 4 and 5. In either of these alternative embodiments, however, multimedia memory 160 remains distinct from the main memory in structure and priority in operation. *See id.* at col. 6, ll. 8–11 (referring to the embodiment of Figs. 4 and 5), col. 8, ll. 4–8 (referring to the embodiment of Fig. 6).

Multimedia engine 112 performs video and audio processing functions. *Id.* at col. 4, ll. 16–18. Those functions are performed by one digital signal processor (DSP) engine 210, as shown in Figure 2, reproduced below, or by two or more DSP engines, as shown in Figure 3, reproduced below.

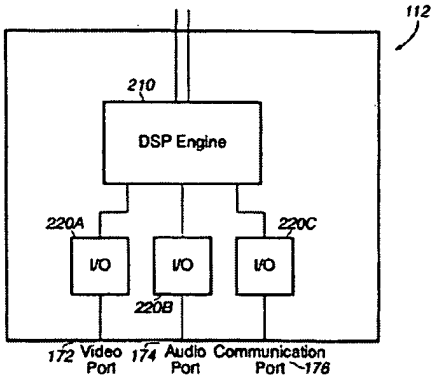

Fig. 2

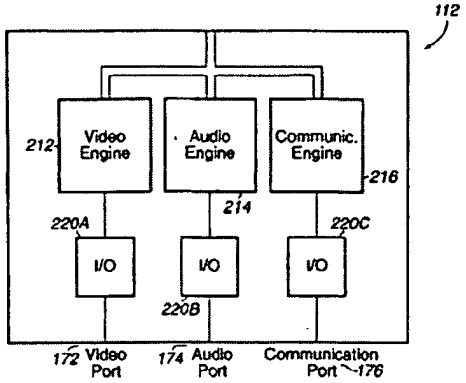

Fig. 3

Figures 2 and 3 are block diagrams of embodiments of multimedia engine 112. *Id.* at col. 3, ll. 32–35.

In operation, multimedia engine 112 and CPU 102 arbitrate for access to multimedia memory 160. *Id.* at col. 8, ll. 4–7. A priority based arbitration scheme may be used. *Id.* at col. 8, ll. 15–17.

b. MPEG (Ex. 1004)

MPEG describes the coded representation of video for digital storage media and specifies the decoding process for the MPEG-2 standard. Ex. 1004, 1. The MPEG standard was known and accessible at least as of August of 1993. Ex. 1008 ¶ 8.

c. Shanley (Ex. 1019)

In Shanley, simultaneously-received bus masters' requests are assigned one of two priority groups. Ex. 1019, 79–81. An arbiter may give greater priority to bus masters in the first group than the second group. *Id.* In particular, "[t]he arbiter can be programmed or designed to treat each group as rotational priority within the group and rotational priority between the two groups. This is pictured in figure 6-2." *Id.* at 80. "The masters in the first group are permitted to access the bus more frequently than those that reside in the second group." *Id.* at 81.

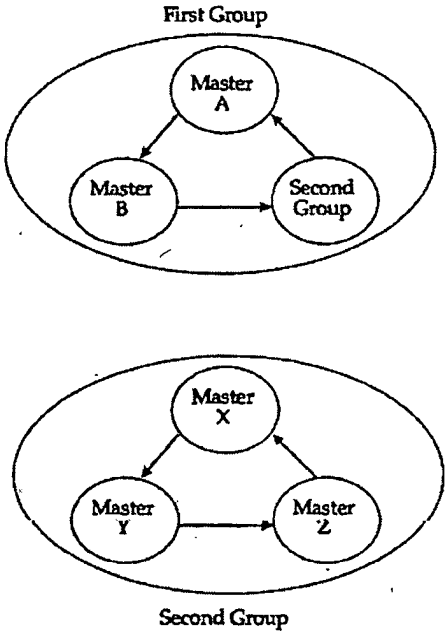

Figure 6-2. Example Arbitration Scheme

Shanley explains that Master A has priority over Master B and Master B has priority over the "Second Group," i.e., Masters X, Y, and Z. *Id.* at 80–81. Thus, in Shanley's exemplary arbitration scheme, the arbitration/priority sequence would be "A → B → X → A → B → Y→A → B → Z → A → B → X, and so on." Pet. 20 (citing Ex. 1019, 80).

d. Analysis

In light of the arguments and evidence of record, Petitioner has not established a reasonable likelihood that claims 1–4 and 7–10 are unpatentable as obvious over Gulick, MPEG, and Shanley.

Independent claim 1 recites "a main memory" that is shared by the "processor" and the "video circuit." Ex. 1001, col. 15, ll. 36–45. Similarly, independent claim 7 recites "a memory" that is shared by the "central processing unit" and the "decoder." *Id.* at col. 16, ll. 17–35. Petitioner

identifies Gulick's multimedia memory 160 and argues that it is "shared" because Gulick teaches that "arbiter block 161 performs arbitration between the CPU 102 and the multimedia engine 112 for the multimedia memory." Pet. 12–13 (claim 1) (citing Ex. 1017, col. 4, ll. 26–27); *see* Pet. 28 (claim 7). We are not persuaded, however, that Gulick's multimedia memory 160 is shared by the processing and video decoding components of claims 1 and 7.

The '753 patent describes decoder/encoder 80 and a first device using a single memory. *See, e.g.,* Ex. 1001, Figs. 2–4. Gulick, in contrast, describes main memory 110 in addition to multimedia memory 160. Ex. 1017, Figs. 1, 4, and 6. The system described in Gulick does not, therefore, realize the advantage of sharing a single memory described by the '753 patent. Ex. 1001, col. 5, ll. 13–15, 47–51.

> Gulick describes CPU 102 as using primarily main memory 110.
>
> Referring again to FIG. 1, in the preferred embodiment, the main memory 110 stores the operating system and applications software as well as driver software, including video drivers and audio drivers. The CPU 102 executes applications software and driver software from the main memory 110 and writes any associated video and audio data to the main memory 110. The CPU 102 then provides high level instructions directly to the multimedia memory 160 and/or to the DMA engine 164, or to the multimedia engine 112.

Ex. 1017, col. 6, ll. 13–22. Gulick further describes CPU 102 using multimedia memory 160 only in exceptional circumstances, such as when main memory 110 is full.

> Thus the multimedia memory 160 is available to store non-multimedia data as needed. In other words, if the main memory 110 becomes full and additional memory is needed, the CPU 102 can store code and data in the multimedia memory 160.

> Thus, the multimedia memory 160 is used for real-time or multimedia data and is also used by the CPU 102 as overflow memory space.

Id. at col. 4, ll. 34–40; *see also id.* at col. 8, ll. 2–3 ("Thus the multimedia memory 160 is available to store non-multimedia data as needed."). Further, even when the multimedia memory is carved out from the main memory, as depicted in Gulick's Figure 6, multimedia engine 112 preferably has priority access to multimedia memory 160. *Id.* at col. 8, ll. 7–8. Accordingly, in an embodiment, "the multimedia engine 112 simply writes one or more bits to a register in the arbiter 161 to gain control of the multimedia memory 160, and the CPU 102 is *only* granted access to the multimedia memory 160 *after a certain starvation period.*" *Id.* at col. 8, ll. 9–13 (emphases added). Because multimedia memory 160 exists in addition to main memory 110 and because CPU 102 uses multimedia memory 160 only in exceptional circumstances, we are not persuaded that multimedia memory 160 teaches or suggests the shared "main memory" of claim 1 or "memory" of claim 7.

Even assuming that multimedia memory 160 is shared, we still are not be persuaded that modifying Gulick's multimedia engine 112 to perform MPEG video decoding would have been obvious. Pet. 14–15. Independent claim 1 recites

> the video circuit configured to receive data from the main memory corresponding to a current video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device, the current video image to be displayed adapted to be stored in the main memory.

Ex. 1001, col. 15, ll. 36–42. Petitioner acknowledges that Gulick does not disclose that multimedia engine 112 is configured to receive data from the

main memory corresponding to a current video image to be decoded and to output decoded video data corresponding to the current video image to be displayed on a display device and stored in the main memory. Pet. 14. Nevertheless, Petitioner argues that a person of ordinary skill in the art would have reason to modify Gulick's "multimedia engine 112 in view of MPEG Standard to perform MPEG video decoding, *which would have resulted in the claimed elements*." *Id.* at 15 (emphasis added). In particular,

> when implementing MPEG video decoding, one of ordinary skill in the art would have understood that Gulick's multimedia engine 112 would be configured *to receive data from multimedia memory 160* corresponding to a current video image to be MPEG-video decoded and to output video data corresponding to the current video image to be displayed on video monitor 114 via video port 172, the current video image to be displayed adapted *to be stored in multimedia memory 160.*

Id. (emphases added) (citing Ex. 1030 ¶¶ 95–100). However, Petitioner fails to explain why a person of ordinary skill in the art would equate Gulick's multimedia memory 160 with main memory 110 for purposes of implementing MPEG standards on Gulick's system. Prelim. Resp. 10–11; *see* Ex. 1030 ¶ 99 ("Under Gulick 983, the multimedia memory 160 would serve as the previous and future picture stores shown above in Figure D.7 [of MPEG]."). Further, Petitioner does not adequately explain why a person of ordinary skill in the art would have reason to modify Gulick to disclose "storing a decoded video image in a 'main memory' (independent claim 1)/'memory' (independent claim 7) that is shared by a video circuit/decoder and a processor/central processing unit." *Id.* at 15; *see* Ex. 1030 ¶ 100. Petitioner argues that modification of Gulick's multimedia engine 112 to perform MPEG video decoding "would constitute a combination of familiar elements according to known methods to yield predictable results." Pet. 15–

16 (citing *KSR*, 550 U.S. at 401). We are not persuaded that such a conclusory statement and citation to *KSR* amount to more than impermissible hindsight and are sufficient to support Petitioner's arguments for the combination of the cited references in the manner proposed to achieve the recited systems.

On this record, Petitioner does not explain adequately how Gulick would have been modified in view of MPEG and Shanley. Pet. 15–16. Dr. Stone's testimony is equally insufficient. In paragraph 101, for example, Dr. Stone testifies that "[a]t the time of the alleged invention of the '753 Patent, the MPEG-1 and MPEG-2 standards were 'currently in use.' [Ex. 1001, col. 1, ll. 53–58.] Indeed, the '753 Patent admits that '[t]he MPEG standards [were] currently well accepted standards.' [*Id.* at col. 2, ll. 6–9.]" Ex. 1030 ¶ 101. Neither Petitioner nor its declarant explains in sufficient detail why or how a person of ordinary skill in the art would have modified Gulick's system in view of MPEG to provide the recited structures for accessing Gulick's "main memory" or to perform the functions recited for video decoding or decompression.

e. Conclusion

On this record, we are not persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–4 and 7–10 are unpatentable as obvious over Gulick, MPEG, and Shanley.

3. Claim 12 – Obviousness over Gulick, MPEG, Shanley, and Gove (Ground B)

Petitioner argues that claim 12 is unpatentable under 35 U.S.C. § 103(a) as obvious over Gulick, MPEG, Shanley, and Gove. Pet. 36–38.

a. Gove (Ex. 1006)

Gove describes Texas Instruments, Inc.'s Multimedia Video Processor (MVP). The MVP is a "highly-integrated processing chip for performing a variety of functions" and is "particularly well suited for video compression algorithms." Ex. 1006, 215 (Abstract).

b. Analysis

Claim 12 depends from independent claim 7. Petitioner relies upon its analysis Gulick, MPEG, and Shanley to teach the limitations of independent claim 7, and relies upon Gove only for the additional limitations recited in the dependent claim 12. *See, e.g.,* Pet. 36 ("*Gulick 983*, in view of *MPEG Standard* and *Shanley*, discloses all claimed elements of claim 7."). As discussed above, we are not persuaded that Petitioner has established a reasonable likelihood that independent claim 7 would have been obvious over Gulick, MPEG, and Shanley. *See supra* Section II.B.2. In these grounds, Petitioner relies upon Gove only for the additional limitations recited in claim 12. Accordingly, Petitioner does not argue that Gove cures the deficiencies noted above with respect to the ground asserted against claim 7.

c. Conclusion

On this record, Petitioner has not established a reasonable likelihood that it would prevail in showing that claim 12 is unpatentable as obvious over the combination of Gulick, MPEG, Shanley, and Gove.

4. Claims 1 and 2 — Obviousness over Bowes and MPEG (Ground C)

Petitioner argues that claims 1 and 2 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes and MPEG. Pet. 38–47.

a. Bowes (Ex. 1003)

Bowes describes a memory bus arbiter for a computer system having a DSP co-processor. Ex. 1003, Title. According to Bowes,

> In prior art computer systems, because of the high bandwidth required for real-time processing by a DSP, it has not been possible for the DSP to run off of the computer system's DRAM in the way the CPU 10 utilizes it without adversely affecting the rest of the computer system. Thus, there has been provided a large block of SRAM 24 for use by the DSP 20. . . .
>
> A significant disadvantage to the prior art computer architecture of FIG. 1 is the requirement of a substantial block of static random access memory 24. SRAMs are significantly more expensive than DRAM which greatly increases the cost of computer systems which incorporate SRAM.

Id. at col. 2, ll. 36–48. Thus, it is an object of Bowes "to provide a mechanism and method for arbitrating the memory bus bandwidth to efficiently allow the use of a digital signal processor and a CPU over a common memory bus sharing the system's dynamic random access memory subsystem without requiring an expensive block static random access." *Id.* at col. 2, ll. 57–63.

Figure 2 of Bowes is reproduced below.

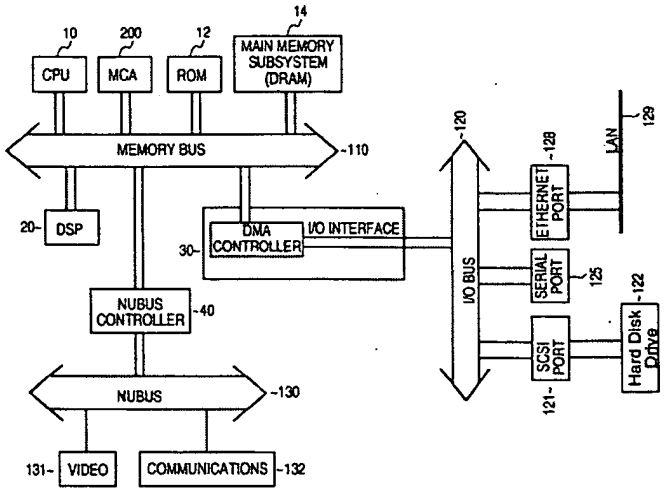

Figure 2

Figure 2 illustrates a block diagram of a computer architecture incorporating the arbitration scheme described in Bowes. *Id.* at col. 3, ll. 62–64. "The scheme is implemented such that the DSP is provided with sufficient bandwidth to perform real-time digital signal processing using the system's dynamic random access memory (DRAM) and not requiring the incorporation of an expensive block of static random access memory (SRAM)." *Id.* at col. 4, ll. 55–60.

As shown in Figure 2, the system includes CPU 10, memory controller and arbiter (MCA) 200, main memory subsystem 14, and DSP 20. *Id.* Fig. 2. "Unlike prior art computer systems, the [system of Bowes] provides for the DSP 20 to reside on the system's memory bus and operate from the computer systems' main memory subsystem 14." *Id.* at col. 6, ll. 22–26. "[T]his greatly reduces system cost by eliminating the need for an expensive block of SRAM." *Id.* at col. 6, ll. 26–29. In a preferred embodiment, MCA 200 "is an application specific integrated circuit (ASIC)

for arbitrating memory bus 110 between the various bus masters subject to the constraints each imposes to provide optimal bandwidth for each, particularly the DSP which is responsible for a significant amount of real-time signal processing." *Id.* at col. 6, ll. 46–52.

b. Analysis

In light of the arguments and evidence of record, Petitioner has established a reasonable likelihood that claims 1 and 2 are unpatentable as obvious over Bowes and MPEG.

With respect to challenged claims 1 and 2, we are persuaded by Petitioner's citations that the combination of Bowes and MPEG teaches or suggests each of the recited limitations. Pet. 38–47. In particular, Bowes discloses supporting video applications (Ex. 1003, col. 1, ll. 24–41), and specifically discloses video controllers 131 coupled to memory bus 110 (*id.* at col. 6, ll. 6–18). Pet. 39. Moreover, DSP 20 performs "image processing." *Id.* (citing Ex. 1003, col. 6, ll. 33–38). Thus, Petitioner argues that Bowes discloses that both CPU 10 (i.e., the "processor" of claim 1) and DSP 20 (i.e., the "video circuit" of claim 1) are attached to memory bus 110, from which they access main memory subsystem 14. Pet. 39. In addition, Petitioner argues that Bowes discloses an arbiter (i.e., MCA 200) and each of the arbiter functions of "providing access" in an idle state (Ex. 1003, col. 7, l. 64–col. 8, l. 10, col. 8, ll. 28–35), "queuing a request for access" in a busy state (*id.* at col. 8, ll. 50–55, 63–65), and "queuing a request for access . . . in an order based on a priority " in a queue state (*id.* at col. 8, ll. 50–55, col. 9, ll. 2–6, 11–14). Pet. 44–46 (citing Ex. 1030 ¶¶ 168–170).

Patent Owner contends that MPEG was considered during prosecution and may not be asserted properly here. *See* Prelim. Resp. 9. Even assuming

that the Examiner considered MPEG during prosecution of the application that led to the '753 patent, we are not precluded from considering it as a basis for unpatentability in an *inter partes* review. *See* 35 U.S.C. § 325(d) (consideration of a previously considered reference is within the Board's discretion).

We also are not persuaded by Patent Owner's contention that the proposed combination does not disclose a decoder receiving an image to be decoded and a previously decoded image from main memory. Prelim. Resp. 21–23. Patent Owner contends that Bowes's "block read" operation relates only to instructions, not to image data. *Id.* at 22–23. Bowes teaches that "the DSP will utilize the memory bus 110 [] to read a large block memory from the DRAM 14 into its internal SRAM." Ex. 1003, col. 7, ll. 3–5. It does not follow from Bowes's discussion of whether "code" is divisible into discrete blocks for block read operations that such "blocks" may contain *only* code, and not data. *See* Prelim. Resp. 22–23 (citing Ex. 1003, col. 6, l. 54–col. 7, l. 12). Moreover, a "block read" is only one mode of operation described in Bowes. Bowes also states that "there may be situations in which the DSP requires only a single piece of data from the DRAM. These types of read operation[s] are referred to as 'scattered-single reads.'" Ex. 1003, col. 7, ll. 23–26. Therefore, on this record, we are persuaded that Bowes teaches or suggests reading image data from main memory. *See* Pet. 40–41 (citing Ex. 1003, col. 6, ll. 33–38).

Patent Owner also contends that the chip of the preferred embodiment—an AT&T DSP3210—has an 8K cache, and that image data is read from that cache rather than from main memory. Prelim. Resp. 24–25. Thus, Patent Owner contends that, like known systems, Bowes teaches the

use of a dedicated memory, instead of a shared memory. *Id.* at 25. This contention is also unavailing. Petitioner identifies DSP 20 as the decoder, and Bowes explicitly describes DSP 20 accessing the DRAM—i.e., the recited "main memory." *See, e.g.,* Ex. 1003, col. 7, ll. 3–5 ("[T]he DSP will utilize the memory bus 110 [] to read a large block memory from the DRAM 14 into its internal SRAM."). Thus, even assuming that Bowes's DSP 20 subsequently uses the data in its cache to decode an image, it can do so only because it previously received that image to be decoded from main memory.

We also are not persuaded by Patent Owner's contention that the proposed combination does not disclose an arbiter that controls access to the main memory. Prelim. Resp. 26–28. Patent Owner contends that "MCA (200) merely controls access to the memory bus (110) of Bowes, not the main/system memory as recited in the claims." *Id.* at 26. Patent Owner does not explain, however, why controlling access to the memory bus does not, in turn, teach or suggest controlling access to the main/system memory. Specifically, Patent Owner asserts that "Bowes' alleged disclosure of a central arbiter that controls access to an internal bus **does not** satisfy the limitation of independent claim 1which recites an arbiter that controls access to the main memory," but does not explain why. *Id.* at 28. On this record, Patent Owner's contention is not persuasive.

Further, we are not persuaded by Patent Owner's contention, with respect to claim 1, that the proposed combination does not disclose an arbitration circuit that receives signals from the microprocessor. *Id.* at 28–31. Patent Owner's contention relies on Bowes' teaching that "to save a pin on the CPU, the CPU *does not* utilize the means for requesting the memory bus" (*id.* at 30 (citing Ex. 1003, col. 3, ll. 34–36)), but that teaching relates

only to a preferred embodiment. Elsewhere, Bowes discloses that MCA 200 receives a request to access memory bus from CPU 10. *See, e.g.,* Ex. 1003, col. 7, l. 64–col. 8, l. 3, col. 8, ll. 45–56.

Petitioner argues that a person of ordinary skill in the art would have found it obvious to combine the teachings of Bowes and MPEG to achieve the recited limitations of challenged claims 1 and 2:

> *Bowes* contemplates supporting video applications, Ex. 1003 at 1:24-41, and discloses video controllers 131 coupled to memory bus 110, *id.*, 6:6-18. One of ordinary skill in the art would have been motivated to modify *Bowes'* DSP 20 in view of *MPEG Standard* to perform MPEG video decoding. At the time of the alleged invention of the '753 patent, the MPEG-1 and MPEG-2 standards were "currently in use." Ex. 1001, 1:53-58. Indeed, the '753 patent admits that "[t]he MPEG standards [were] currently well accepted standards." Ex. 1001, 2:6-9. Thus, modifying *Bowes'* DSP 20 to perform MPEG video decoding per *MPEG Standard* would constitute a combination of familiar elements according to known methods to yield predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007); *see also* Ex. 1030, Stone Decl. ¶¶ 157-61. Indeed, the *MPEG Standard* "was developed in response to the growing need for a common format representing compressed video on various digital storage media" . . . . Ex. 1004 at 4 (§ 0.1). In fact, it was well known in the art at the time of the alleged invention to employ a DSP for MPEG video processing. *See* Ex. 1017, 5:15-21; Ex. 1007, 1:62-67, Fig. 5. One of ordinary skill in the art would have understood that *Bowes*'s DSP 20, as modified by *MPEG Standard*, would be configured to receive data from main memory subsystem 14 corresponding to a current video image to be MPEG-video decoded and to output video data corresponding to the current video image to be displayed via video controllers 131, the current video image to be displayed adapted to be stored in main memory subsystem 14. Ex. 1030, Stone Decl. ¶¶ 162-63.

Pet. 41–42.

Patent Owner contends that Petitioner has not articulated sufficiently a reason to combine Bowes and MPEG, and that Bowes is incompatible with MPEG. Prelim. Resp. 31–37. Specifically, Patent Owner contends that "the available bandwidth for the DSP (20) of Bowes at 2.4 microseconds is *orders of magnitude* less than the required bandwidth for implementing encoding/decoding using the MPEG Standard." *Id.* at 34 (emphasis added). Patent Owner's contention, however, relies on a description in Bowes of "Alternative DSP Operation Modes." Prelim. Resp. 32–33; *see* Ex. 1003, col. 9, ll. 19–53. Moreover, Patent Owner does not provide persuasive argument that the "required bandwidth for implementing encoding/decoding using the MPEG Standard" is "orders of magnitude" (Prelim. Resp. 34) greater than what is available in Bowes. In addition, the bandwidths, upon which Patent Owner relies, are those required "[t]o operate in real time" and to avoid "noticeable" frame dropping "to the movie viewer." Prelim. Resp. 33–34 (citing Ex. 1001, col. 7, l. 59–col. 8, l. 2); *see* Ex. 1001, col. 9, ll. 35–45 (describing different decoding and encoding standards). Neither challenged claim 1 nor challenged claim 2 recites operation in "real time" or the function of generating a decoded image, from which a human viewer is unable to detect any delay in decoding or encoding. Ex. 1001, col. 15, ll. 32–67 (claims 1 and 2); *see id.* at col. 7, l. 59–col. 8, l. 2. In the absence of such recitations, we do not construe the claims narrowly to incorporate the particular bandwidth limits discussed in the Specification. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). On this record, therefore, we are persuaded that Petitioner has provided articulated reasoning with some rational underpinning sufficient to support the legal conclusion of

obviousness. *See KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

d. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1 and 2 are unpatentable as obvious over the combination of Bowes and MPEG.

5. Claim 3 — Obviousness over Bowes, MPEG, and Stearns (Ground D)

Petitioner argues that claim 3 is unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Stearns. Pet. 47–49.

a. Stearns (Ex. 1007)

Stearns describes a computer architecture in which MPEG accelerator functionality is integrated with a graphics accelerator. Ex. 1007, 6:14–23, Fig. 4.

b. Analysis

Claim 3 depends directly from independent claim 1. As discussed above, we are persuaded that Petitioner has established a reasonable likelihood that independent claim 1 would have been obvious over the combination of Bowes and MPEG. *See supra* Section II.B.4. Petitioner relies upon Stearns only for the additional limitations recited in dependent claim 3. Pet. 47–49. Patent Owner does not dispute that Stearns teaches or suggests the additional limitations of claim 3 or that a person of ordinary skill in the art would have reason to combine Stearns's teachings with those of Bowes and MPEG. Instead, Patent Owner contends that Stearns does not teach or suggest the limitations of claim 1 allegedly missing from Bowes and MPEG. Prelim. Resp. 37–38. Petitioner, however, provides a

sufficiently detailed explanation regarding the teachings of the combination of Bowes, MPEG, and Stearns and the reasons for combining the teachings of those references to achieve the limitations of claim 3. Pet. 47–49.

On this record, Petitioner has established a reasonable likelihood that it would prevail in showing that claim 3 is unpatentable as obvious over the combination Bowes, MPEG, and Stearns.

6. Claim 4 — Obviousness over Bowes, MPEG, and Shanley (Ground E)

Petitioner argues that claim 4 is unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Shanley. Pet. 49–50.

Claim 4 depends directly from independent claim 1. As discussed above, we are persuaded that Petitioner has established a reasonable likelihood that independent claim 1 would have been obvious over the combination of Bowes and MPEG. *See supra* Section II.B.4. Petitioner relies upon Shanley only for the additional limitations recited in dependent claim 4. Pet. 49–50. Patent Owner does not dispute that Shanley teaches or suggests the additional limitations of claim 4 or that a person of ordinary skill in the art would have reason to combine Shanley's teachings with those of Bowes and MPEG. Instead, Patent Owner contends that Shanley does not teach or suggest the limitations of claim 1 allegedly missing from Bowes and MPEG. Prelim. Resp. 38. Petitioner, however, provides a sufficiently detailed explanation regarding the teachings of the combination of Bowes, MPEG, and Shanley and the reasons for combining the teachings of those references to achieve the limitations of claim 4. Pet. 49–50.

On this record, Petitioner has established a reasonable likelihood that it would prevail in showing that claim 4 is unpatentable as obvious over the combination Bowes, MPEG, and Shanley.

7. Claims 7 and 8 — Obviousness over Bowes, MPEG, and Whai (Ground F)

Petitioner argues that claims 7 and 8 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bowes, MPEG, and Whai. Pet. 50–55.

a. *Whai (Ex. 1018)*

Whai describes shared memory system 10 that interfaces between each of the peripherals 1–N, including processor bus 20 and shared memory bus 14. Ex. 1018, Abstract, Fig. 1. Whai's Figure 1, including our annotation, is reproduced below.

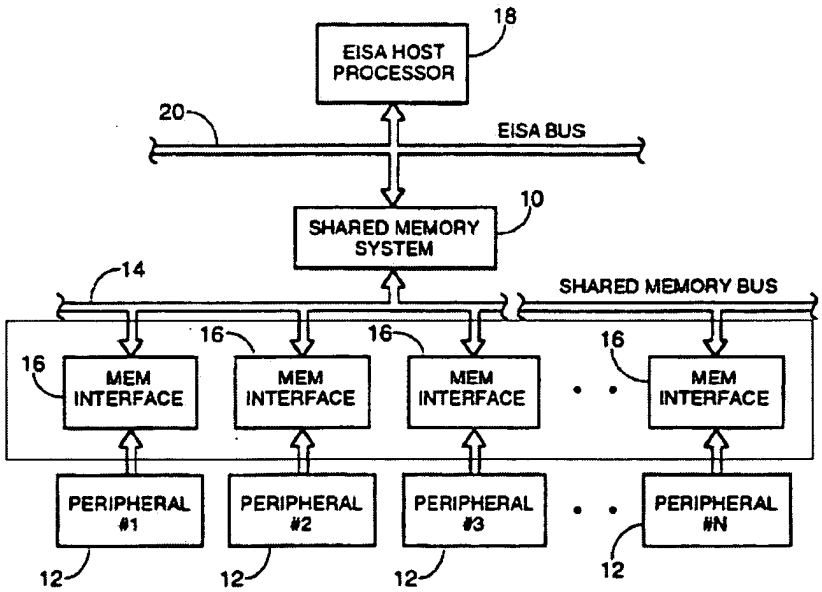

FIG. 1

Whai's Figure 1 depicts shared memory system 10 including arbitration logic circuit 78 that services bus requests from *each* of a plurality of memory interfaces coupled to shared memory bus 14. *Id.* at Abstract, Fig. 4. "In the

arbitration function, the shared memory system 10 determines via various bus signals generated by the shared memory interfaces 16 to determine how to service these requests and which one is serviced at a given time." *Id.* at 8:20–23. "A memory interface device is disposed *between each of the peripheral devices and the centrally located memory system* and is operable to control the transmittal of addresses from the associated peripheral device to the centrally located memory and transfer of data therebetween." *Id.* at 3:11–15 (emphasis added).

b. Analysis

Independent claim 7 recites "the decoder having a memory interface circuit" and "the central processing unit having a memory interface circuit." Ex. 1001, col. 16, ll. 24–25, 27–28. Moreover, independent claim 7 recites "an arbiter included in the memory interface circuit of the decoder and coupled to the memory interface circuit of the central processing unit." *Id.* at col. 16, ll. 29–31. Petitioner argues that Bowes and MPEG teach or suggest all of the limitations of claims 7 and 8, except for the recited, memory interface circuits. Pet. 51–53; *see id.* at 38–46 (claim 1). Accordingly, Petitioner argues that "one of ordinary skill would have been motivated to apply Whai's memory interface circuits to Bowes given Whai's teaching that such memory interface circuits help an arbitration function to determine 'how to service [] requests and which one is serviced at a given time.'" Pet. 52 (citing Ex. 1018, 8:18–23); *see id.* at 53 (citing Ex. 1030 ¶ 187).

With respect to the arbiter, however, Petitioner argues that "MCA 200, memory bus 110, and DSP 20's interface to memory bus 110 *together* form a memory interface circuit, which includes MCA 200, for DSP 20."

Pet. 54 (citing Ex. 1030 ¶ 188). Thus, Petitioner argues that Bowes, MPEG, and Whai teach or suggest "an arbiter included in the memory interface circuit of the decoder and coupled to the memory interface circuit of the central processing unit." Ex. 1001, col. 16, ll. 29–31. Because Whai teaches that "[a] memory interface device is disposed between *each* of the peripheral devices and the centrally located memory system" (Ex. 1018, 3:11–15 (emphasis added)), we are not persuaded that Whai teaches that several peripherals may be combined to form together a single memory interface. Thus, the combination of Bowes, MPEG, and Whai fails to teach or suggest all of the limitations of claim 7 or of claim 8, which depends from claim 7.

c. Conclusion

On this record, Petitioner has failed to establish a reasonable likelihood that it would prevail in showing that claims 7 and 8 are unpatentable as obvious over the combination Bowes, MPEG, and Whai.

8. Claims 9, 10, and 12 — Obviousness over Bowes, MPEG, Whai, and Shanley or Gove (Grounds G and H)

Each of claims 9, 10, and 12 depends directly from independent claim 7. As discussed above, we are not persuaded that Petitioner has established a reasonable likelihood that independent claim 7 would have been obvious over the combination of Bowes, MPEG, and Whai. Petitioner relies upon Shanley only for the additional limitations recited in dependent claims 9 and 10 and upon Gove only for the additional limitations recited in dependent claim 12. Pet. 55–58. Patent Owner does not dispute that Shanley teaches or suggests the additional limitations of claims 9 and 10 or that Gove teaches or suggests the additional limitation of claim 12. Prelim. Resp. 40–41. Further, Patent Owner does not contend that a person of ordinary skill in the

art would have reason to combine Shanley's or Gove's teachings with those of Bowes and MPEG to achieve the limitations of these dependent claims. *Id.* Instead, Patent Owner contends that neither Shanley nor Gove teaches or suggests the limitations of claim 7 allegedly missing from Bowes, MPEG, and Whai. *Id.* We agree.

On this record, Petitioner has failed to establish a reasonable likelihood that it would prevail in showing that claim 9, 10, or 12 is unpatentable as obvious over the combination of Bowes, MPEG, Whai, and either Shanley or Gove.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–4 of the '753 patent.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted on the following grounds:

Claims 1 and 2 under 35 U.S.C. § 103 as obvious over Bowes and MPEG;

Claim 3 under 35 U.S.C. § 103 as obvious over Bowes, MPEG, and Stearns; and

Claim 4 under 35 U.S.C. § 103 as obvious over Bowes, MPEG, and Shanley;

FURTHER ORDERED that review is not instituted on any other ground; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(d) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial on the grounds of unpatentability authorized above; the trial commences on the entry date of this Decision.

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Doc Code: PET.POA.WDRW
Document Description: Petition to withdraw attorney or agent (SB83)

PTO/AIA/83 (04-13)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	12/424389
Filing Date	April 15, 2009
First Named Inventor	Jefferson Eugene Owen
Art Unit	2628
Examiner Name	Hau H. Nguyen
Practitioner Docket Number	850063.553C4

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above-identified patent application, and

☐ all the practitioners of record;

☐ the practitioners (with registration numbers) of record listed on the attached paper(s); or

☑ the practitioners of record associated with Customer Number: 30423

NOTE: The immediately preceding box should only be marked when the practitioners were appointed using the listed Customer Number.

The reason(s) for this request are those described in 37 CFR:

☐ 11.116(a)(1) ☐ 11.116(a)(2) ☑ 11.116(a)(3)
☑ 11.116(b)(1) ☐ 11.116(b)(2) ☐ 11.116(b)(3)
☐ 11.116(b)(4) ☐ 11.116(b)(5) ☐ 11.116(b)(6)
☐ 11. 116(b)(7) Please explain below:

This patent has been sold by our client to Acacia Research Group, LLC. The new owner has engaged new, different counsel. All of our files have been transferred from our firm to the new owner. We have not been asked to take any action associated with these matters after the sale of the patents. We are informed that the new counsel is Alisa Lipsky of Ahmad, Zavitsanos, Anaipakos, Alavi & Mensing, P.C., reg.number, 55,386. A copy of this withdrawal notice is being sent to Acacia Research Group and to this patent attorney.

Certifications

Check each box below that is factually correct. WARNING: If a box is left unchecked, the request will likely not be approved.

1. ☑ I/We have given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intend to withdraw from employment.

2. ☑ I/We have delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled.

3. ☑ I/We have notified the client of any responses that may be due and the time frame within which the client must respond.

Please provide an explanation, if necessary:

This is an issued patent that is the subject of litigation and an IPR and the new owner has selected new counsel for these matters.

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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Complete the following section only when the correspondence address will change. *Changes of address will only be accepted to an applicant.*

Change the correspondence address and direct all future correspondence to:

A. ☐ The address of the applicant associated with Customer Number: _____

OR

B. ☑ Applicant

Address Alisa Lipski, AZA for Parthenon, 1221 McKinney Street, Suite 3460

City	State	Zip	Country
Houston	TX	77010	US

Telephone 713-655-1101 Email alipski@azalaw.com

I am authorized to sign on behalf of myself and all withdrawing practitioners.

Signature /David V. Carlson/

Name David V. Carlson Registration No. 31153

Address Seed IP Law Group PLLC, 701 5th Avenue, Suite 5400

City	State	Zip	Country
Seattle	WA	98104	USA

Date March 10, 2016 Telephone No. 206-622-4900

NOTE: Withdrawal is effective when approved rather than when received.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	25157729
Application Number:	12424389
International Application Number:	
Confirmation Number:	1455
Title of Invention:	ELECTRONIC SYSTEM AND METHOD FOR SELECTIVELY ALLOWING ACCESS TO A SHARED MEMORY
First Named Inventor/Applicant Name:	Jefferson Eugene Owen
Customer Number:	30423
Filer:	David V. Carlson/Jacque Shepherd
Filer Authorized By:	David V. Carlson
Attorney Docket Number:	96-S-012C4 (850063.553C4)
Receipt Date:	10-MAR-2016
Filing Date:	15-APR-2009
Time Stamp:	12:55:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	850063_553C4_RequestWithdrawCounselChangeAddress.pdf	306000 a923615da05a9097513a5d717269918658bee2d8	no	3

Warnings:	
Information:	

Total Files Size (in bytes):	306000

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:14-cv-00689	6/12/2014	Eastern District of Texas

PLAINTIFF	DEFENDANT
Parthenon Unified Memory Architecture LLC	Motorola Mobility, Inc.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	5,812,789	9/22/1998	Parthenon Unified Memory Architecture LLC
2	5,960,464	9/28/1999	Parthenon Unified Memory Architecture LLC
3	6,058,459	5/2/2000	Parthenon Unified Memory Architecture LLC
4	6,427,194	7/30/2002	Parthenon Unified Memory Architecture LLC
5	7,321,368	1/22/2008	Parthenon Unified Memory Architecture LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
All claims and counterclaims between Plaintiff Parthenon Unified Memory Architecture LLC ("PUMA") and Defendant Motorola Mobility LLC ("Motorola") are DISMISSED WITH PREJUDICE. PUMA and Motorola each shall bear its own attorneys' fees, costs, and other expenses.

CLERK	(BY) DEPUTY CLERK	DATE
David A. O'Toole	Nakisha Love	2/9/16

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 **CONTINUATION**

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
6	7,542,045	6/02/2009	Parthenon Unified Memory Architecture LLC
7	7,777,753	8/17/2010	Parthenon Unified Memory Architecture LLC
8	8,054,315	11/8/2011	Parthenon Unified Memory Architecture LLC
9	8,681,164	3/25/2014	Parthenon Unified Memory Architecture LLC