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United States Patent [19]

Papworth et al.

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[54] **ENTRY ALLOCATION IN A CIRCULAR BUFFER USING WRAP BITS INDICATING WHETHER A QUEUE OF THE CIRCULAR BUFFER HAS BEEN TRAVERSED**

[75] Inventors: **David B. Papworth**, Beaverton; **Andrew F. Glew; Michael A. Fetterman**, both of Hillsboro; **Glenn J. Hinton; Robert P. Colwell**, both of Portland; **Steven J. Griffith**, Aloha; **Shantanu R. Gupta; Narayan Hegde**, both of Beaverton, all of Oreg.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **633,905**

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Related U.S. Application Data

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[51] Int. Cl.^{6} G06F 12/00

[52] U.S. Cl. 395/800; 364/251; 364/244.4; 364/DIG. 1; 395/437; 395/250

[58] Field of Search 395/800, 375, 395/437, 250

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Primary Examiner—Eric Coleman
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

An allocator assigns entries for a circular buffer. The allocator receives requests for storing data in entries of the circular buffer, and generates a head pointer to identify a starting entry in the circular buffer for which circular buffer entries are not allocated. In addition to pointing to an entry in the circular buffer, the head pointer includes a wrap bit. The allocator toggles the wrap bit each time the allocator traverses the linear queue of the circular buffer. A tail pointer is generated, including the wrap bit, to identify an ending entry in the circular buffer for which circular buffer entries are allocated. In response to the request for entries, the allocator sequentially assigns entries for the requests located between the head pointer and the tail pointer. The allocator has application for use in a microprocessor performing out-of-order dispatch anti speculative execution. The allocator is coupled to a reorder buffer, configured as a circular buffer, to permit allocation of entries. The allocator utilizes an all or nothing allocation policy, such that either all or no incoming instructions are allocated during an allocation period.
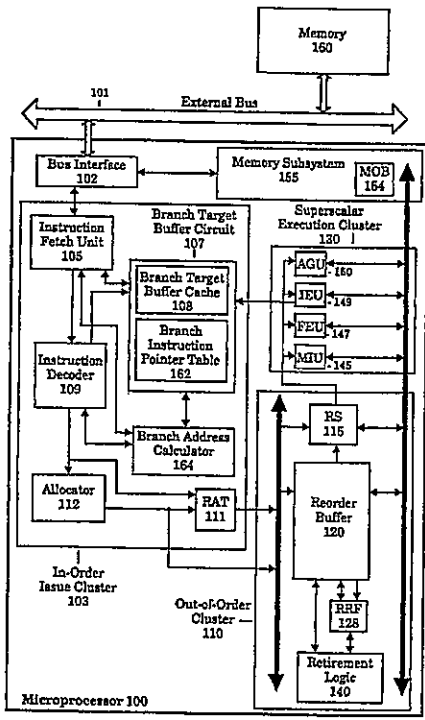
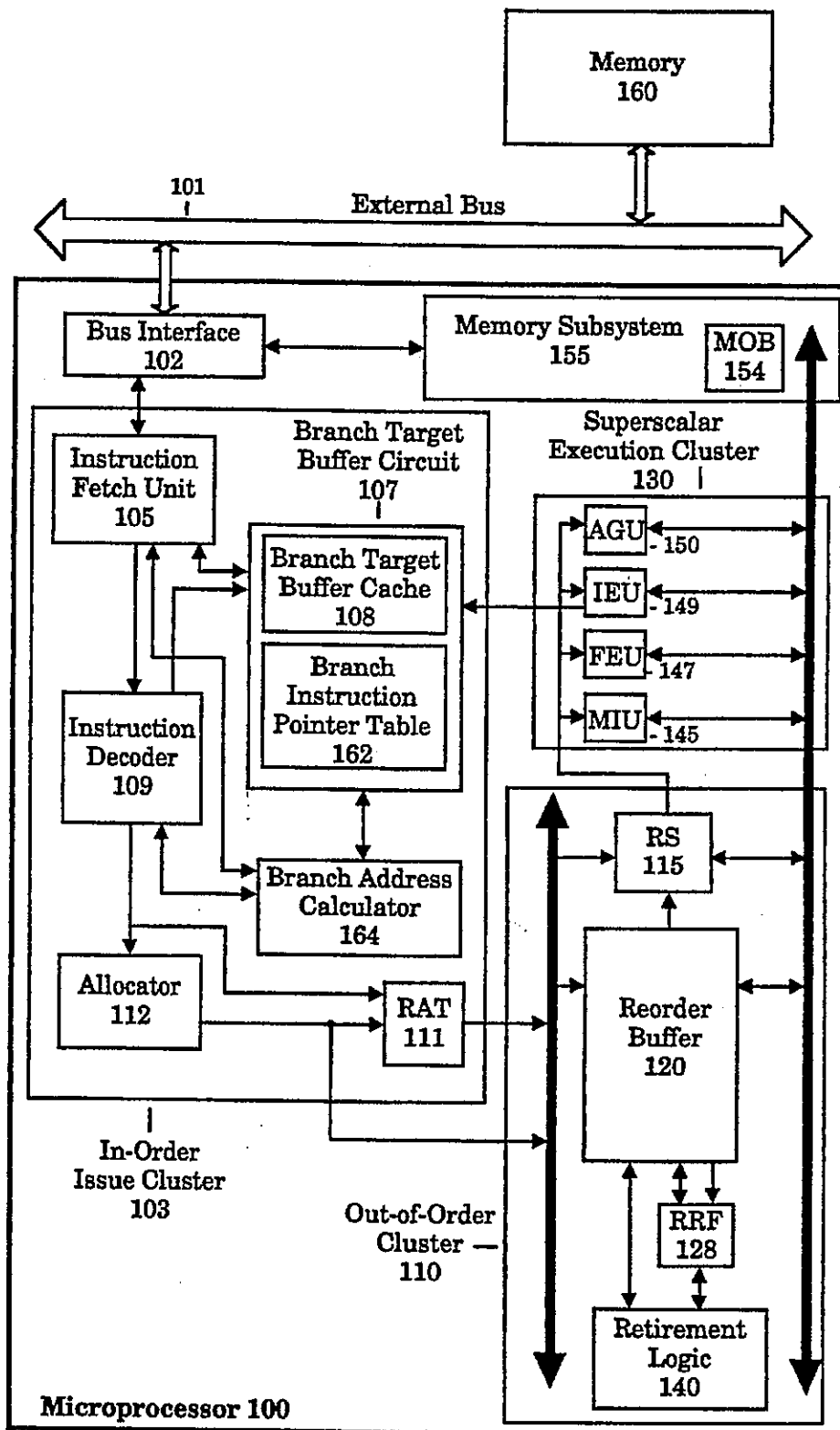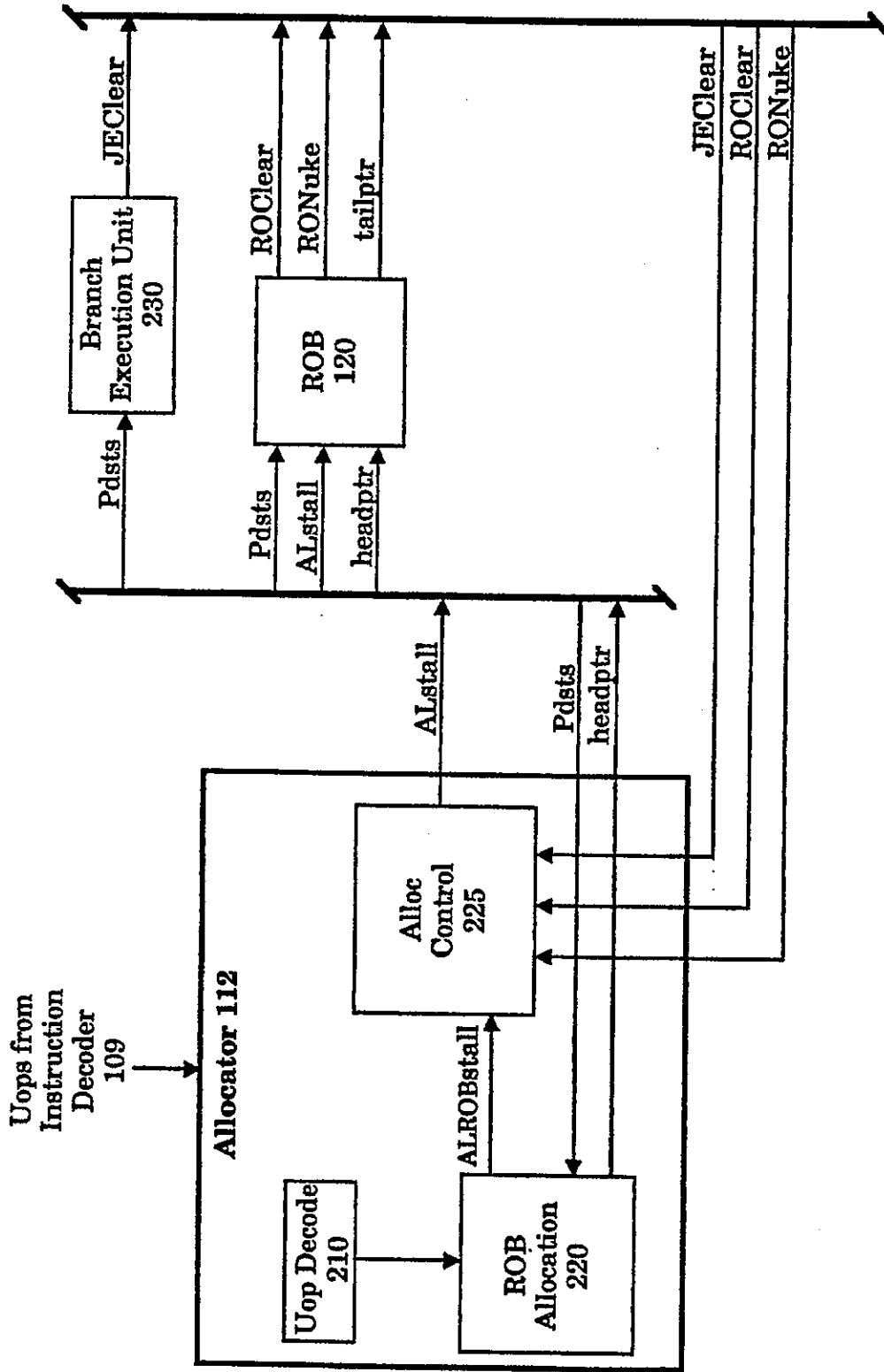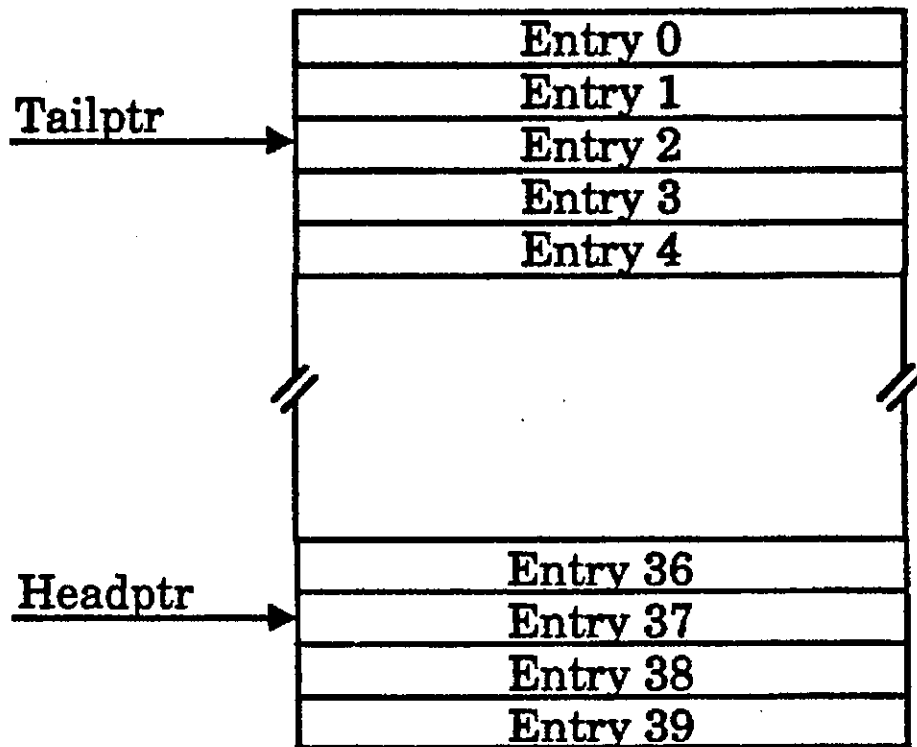**8 Claims, 8 Drawing Sheets**

EXHIBIT 4
Witness:

Figure 1

Figure 2

Entry 0
Entry 1
Entry 2
Entry 3
Entry 4
Entry 36
Entry 37
Entry 38
Entry 39

Tailptr →

Headptr →
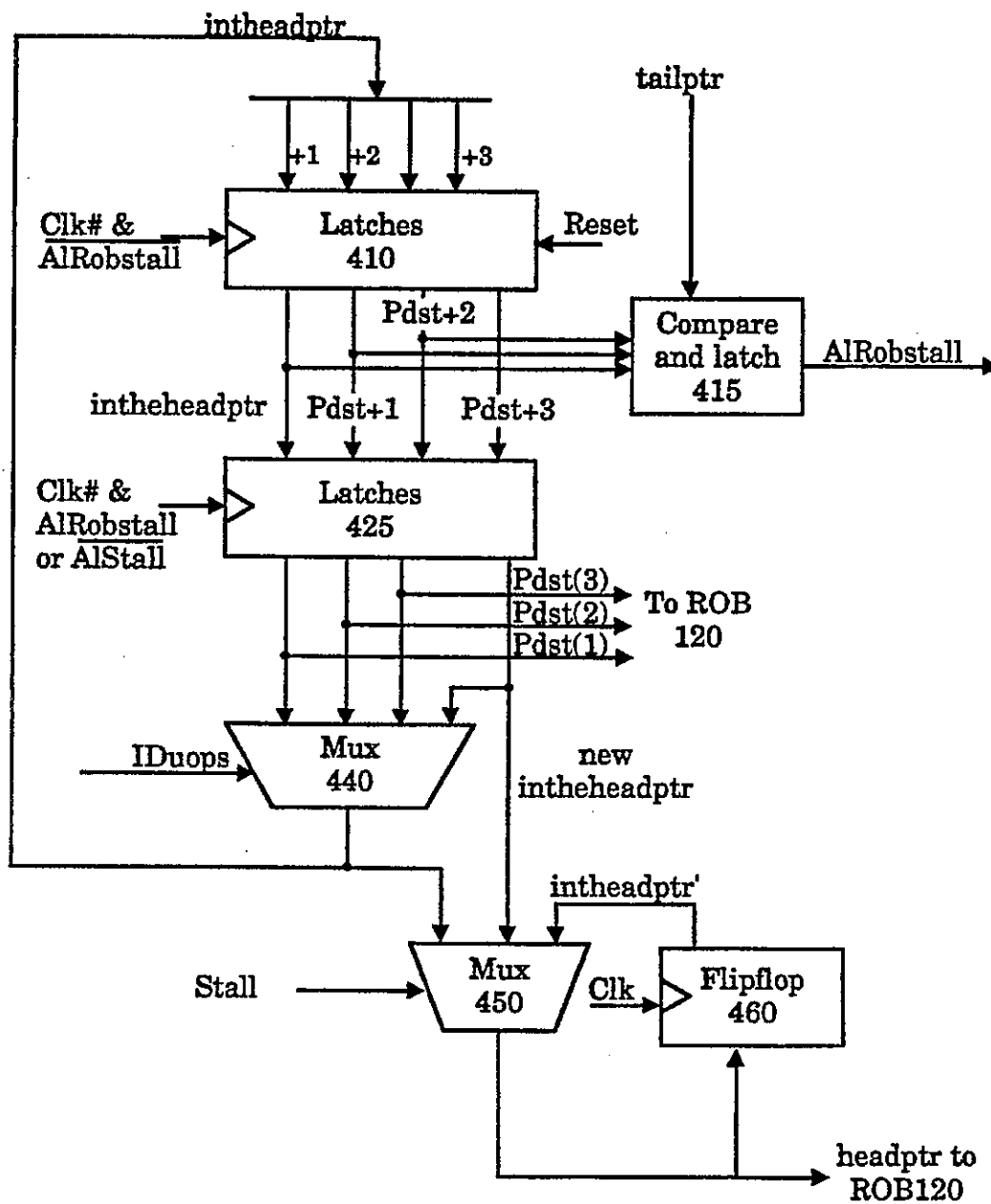
Figure 3

Figure 4

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