



US005757385A

United States Patent [19]**Narayanaswami et al.**[11] **Patent Number:** **5,757,385**[45] **Date of Patent:** **May 26, 1998**[54] **METHOD AND APPARATUS FOR
MANAGING MULTIPROCESSOR
GRAPHICAL WORKLOAD DISTRIBUTION**[75] Inventors: **Chandrasekhar Narayanaswami;**
Avijit Saha, both of Austin, Tex.[73] Assignee: **International Business Machines
Corporation**, Armonk, N.Y.[21] Appl. No.: **629,500**[22] Filed: **Jan. 30, 1996****Related U.S. Application Data**

[63] Continuation of Ser. No. 286,711, Jul. 21, 1994.

[51] **Int. Cl.⁶** **G06F 15/80**[52] **U.S. Cl.** **345/505; 395/675**[58] **Field of Search** 395/126-133,
395/501, 502, 505, 507, 515, 675; 345/24,
27, 28, 133, 185, 189, 203, 505, 501, 502,
507, 515[56] **References Cited****U.S. PATENT DOCUMENTS**

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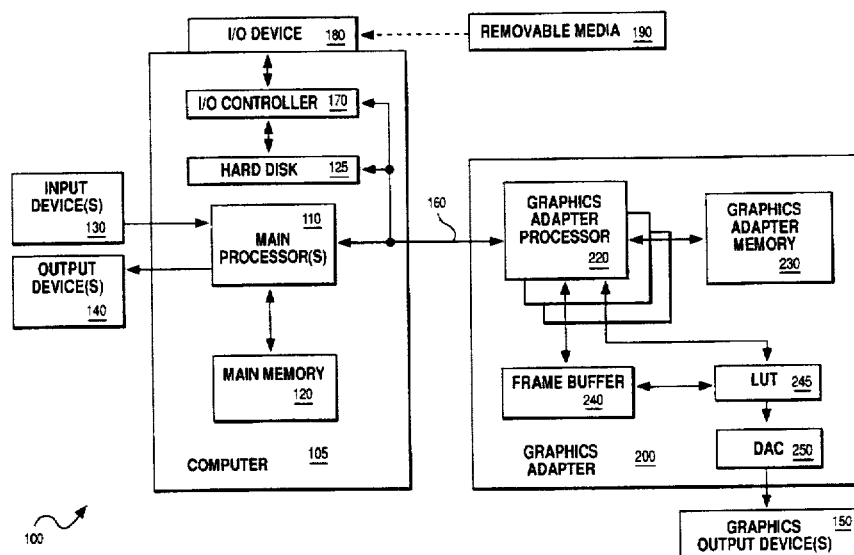
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Primary Examiner—Kee M. Tung*Attorney, Agent, or Firm*—Volel Emile; Alan L. Carlson;
Andrew J. Dillon[57] **ABSTRACT**

An apparatus for utilizing multiple processors to render
graphical objects for display including apparatus for storing
in memory a list of pixel locations assigned to each of the
processors, apparatus for scan converting each received
graphical object into pixels, and each processor including
apparatus for rendering graphical object pixels at pixel
locations assigned to the processor. In addition, a method of
utilizing multiple processors to render graphical objects for
display including the steps of storing in memory a list of
pixel locations assigned to each of the processors, scan
converting each received graphical object into pixels, and
each processor rendering graphical object pixels at pixel
locations assigned to the processor.

18 Claims, 6 Drawing Sheets

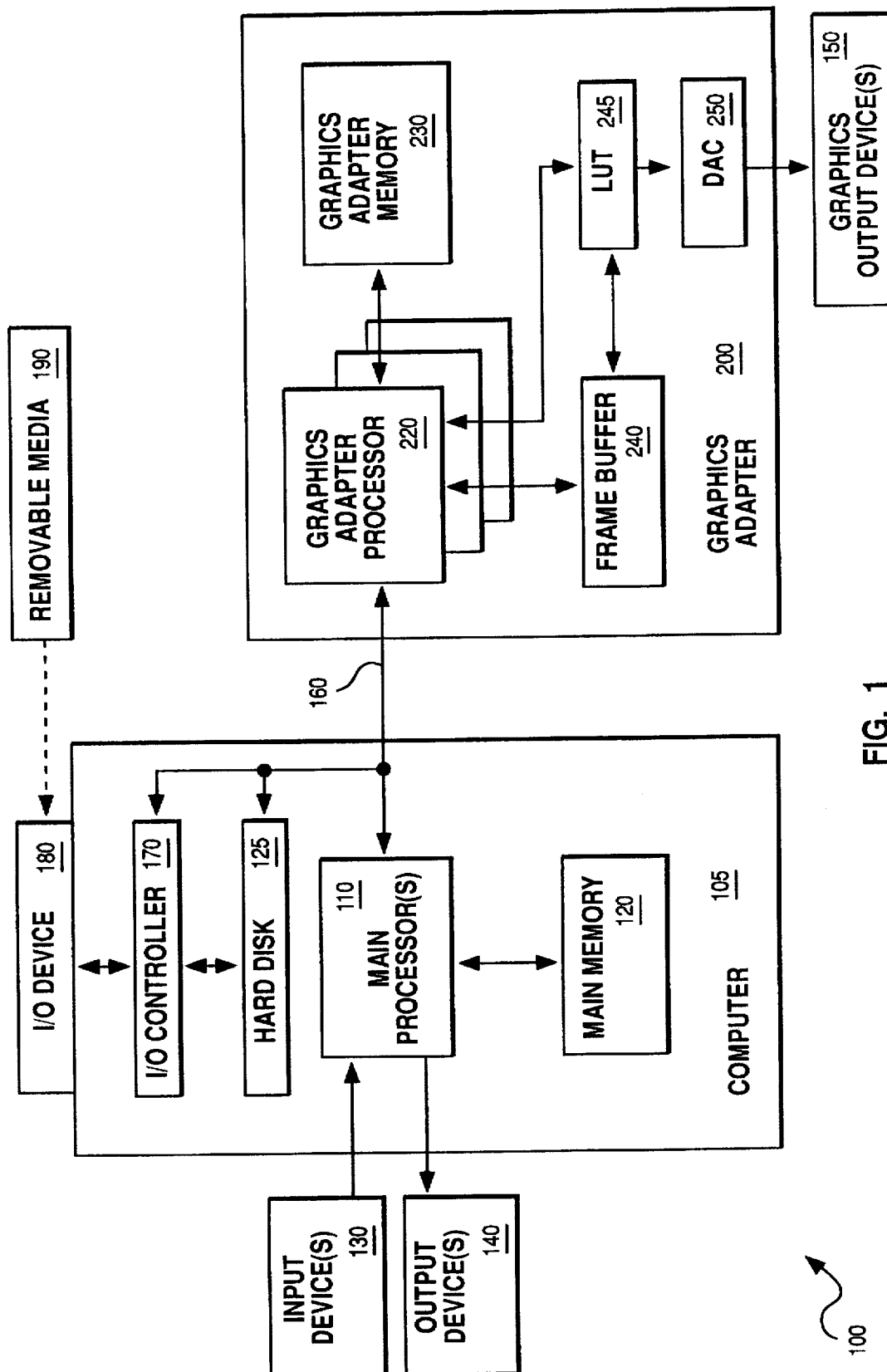


FIG. 1

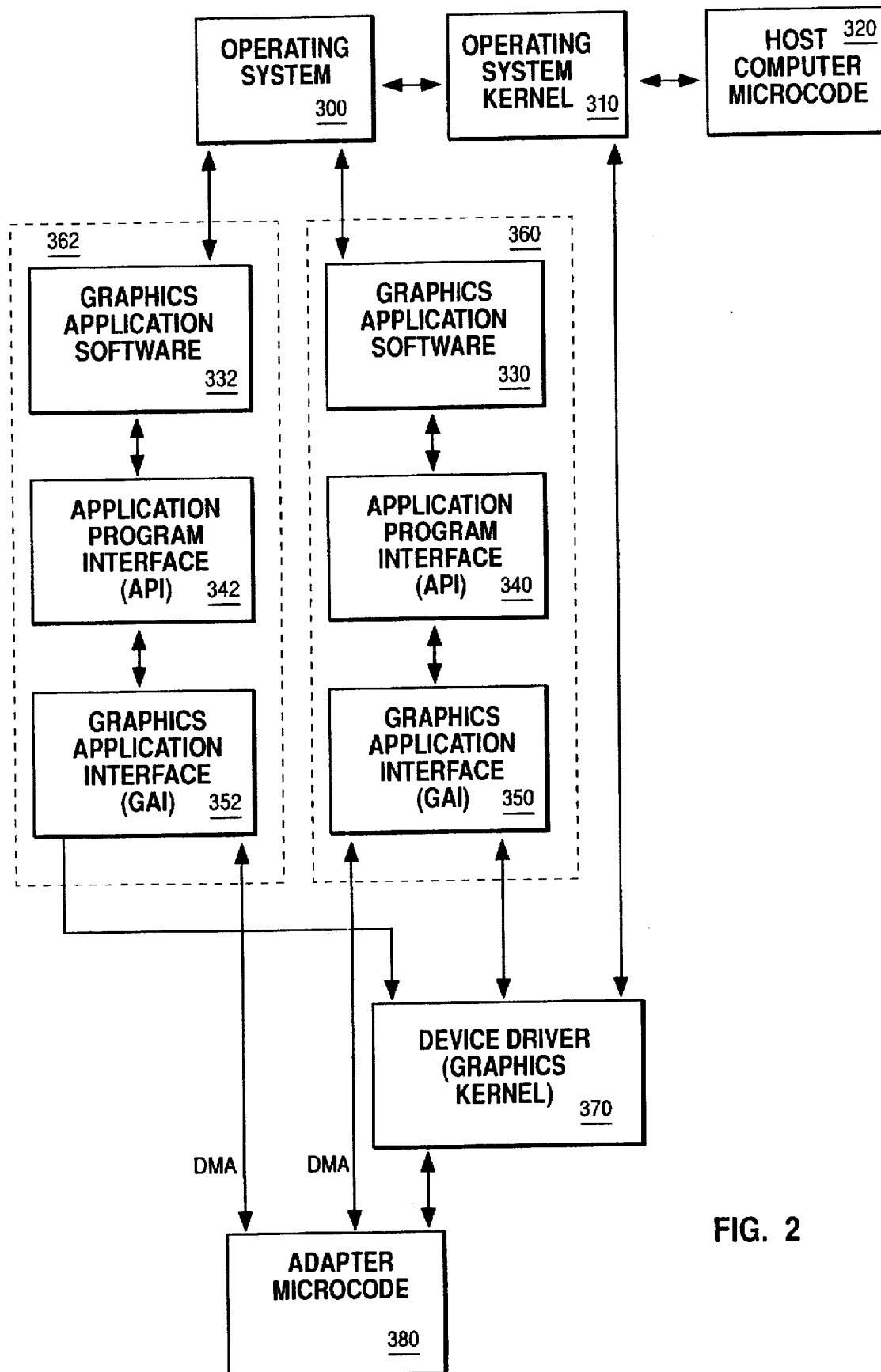


FIG. 2

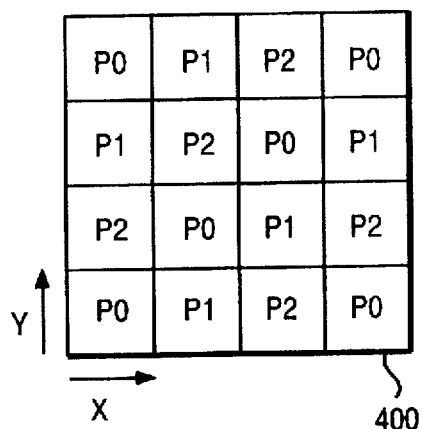


FIG. 3A

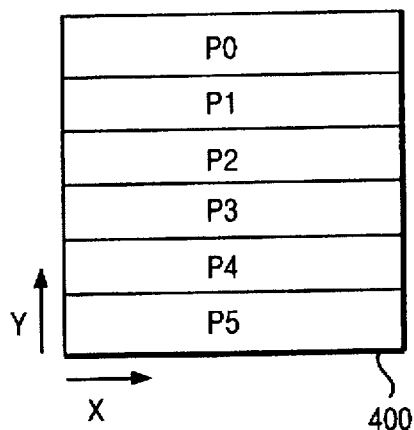


FIG. 3B

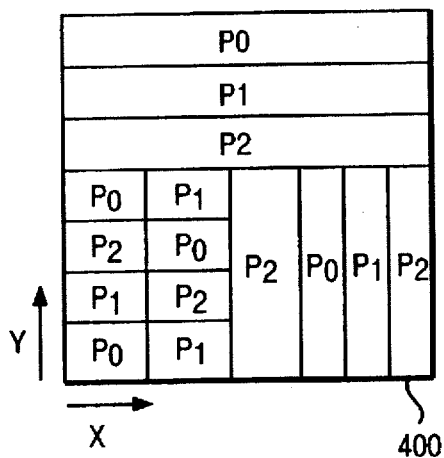


FIG. 3C

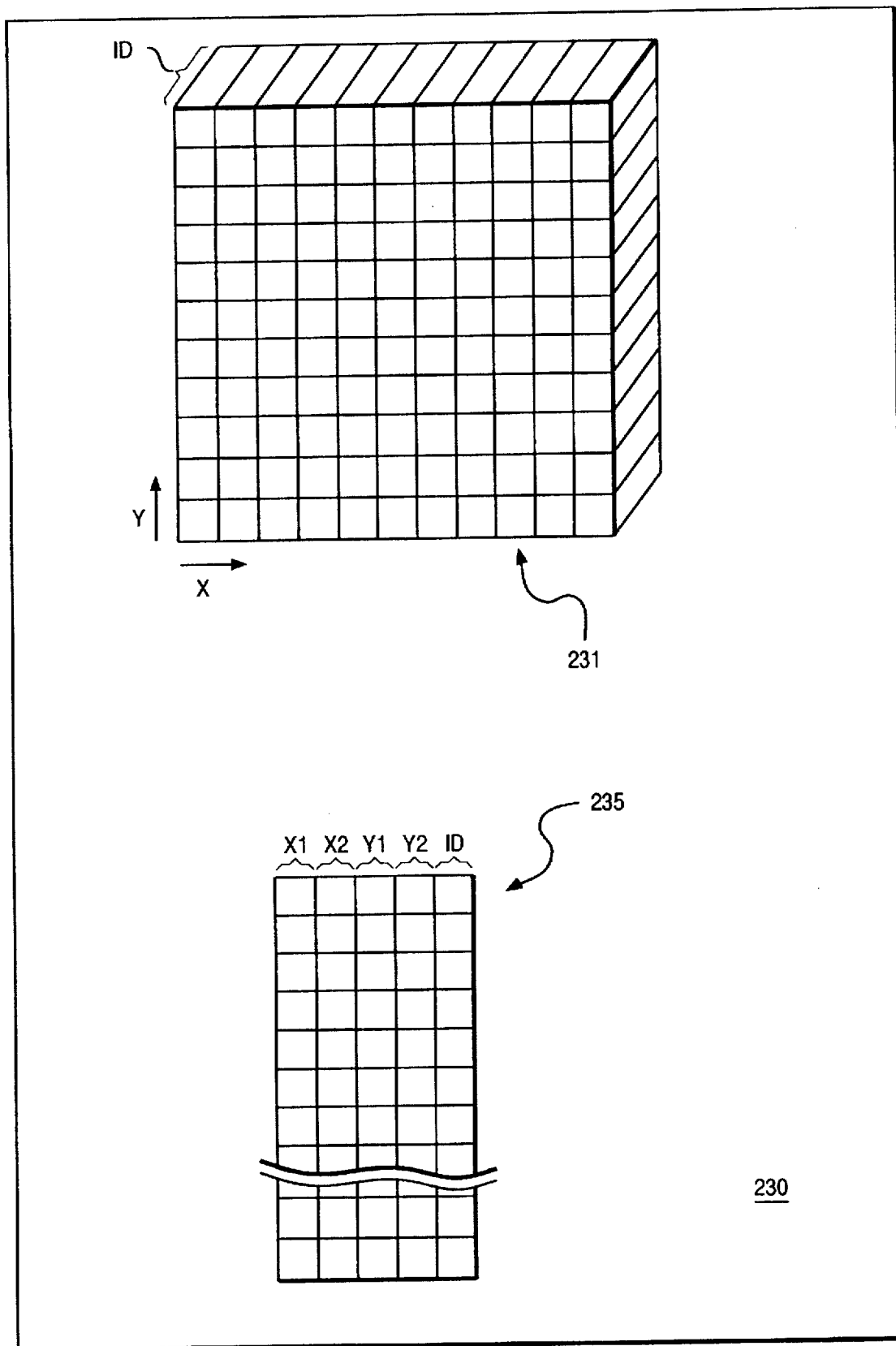


FIG. 4

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