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Perego

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(54) **SCALABLE UNIFIED MEMORY ARCHITECTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 396 days.

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(51) **Int. Cl.**⁷ **G06F 15/167**

(52) **U.S. Cl.** **345/542; 345/543; 345/544**

(58) **Field of Search** 345/421, 542, 345/519, 536, 522, 506, 505, 531, 532, 520, 535, 543, 544; 710/26; 712/201; 711/209, 120, 170, 111, 105, 103; 341/51; 375/240.12

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Primary Examiner—Matthew C. Bella

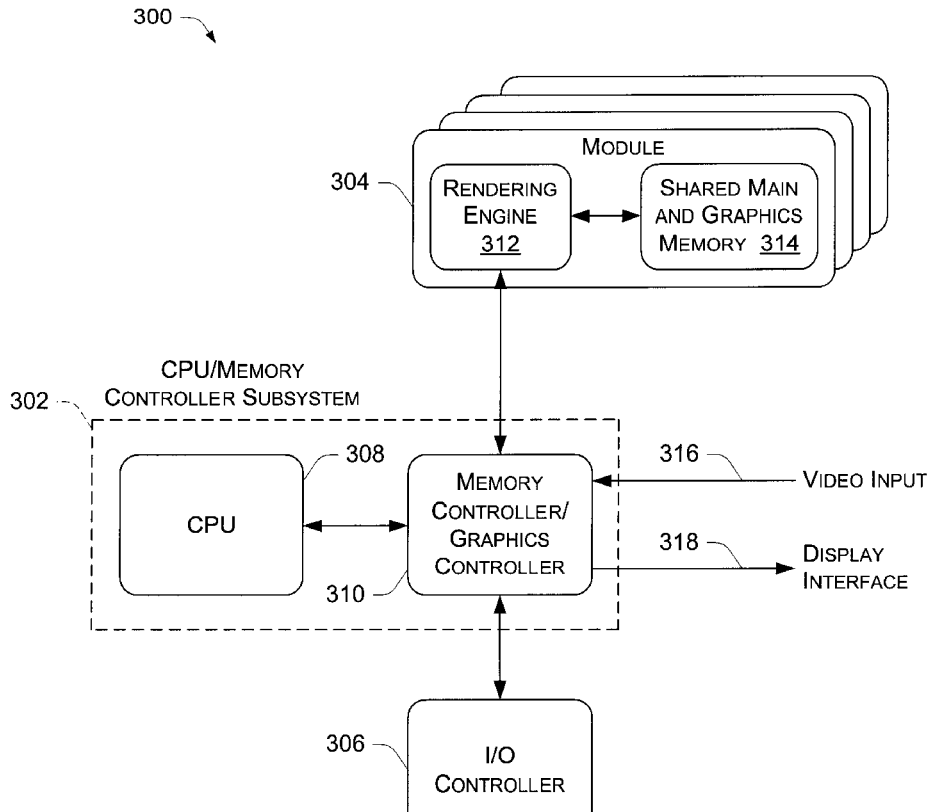
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(57) **ABSTRACT**

A memory architecture includes a memory controller coupled to multiple modules. Each module includes a computing engine coupled to a shared memory. Each computing engine is capable of receiving instructions from the memory controller and processing the received instructions. The shared memory is configured to store main memory data and graphical data. Certain computing engines are capable of processing graphical data. The memory controller may include a graphics controller that provides instructions to the computing engine. An interconnect on each module allows multiple modules to be coupled to the memory controller.

34 Claims, 7 Drawing Sheets



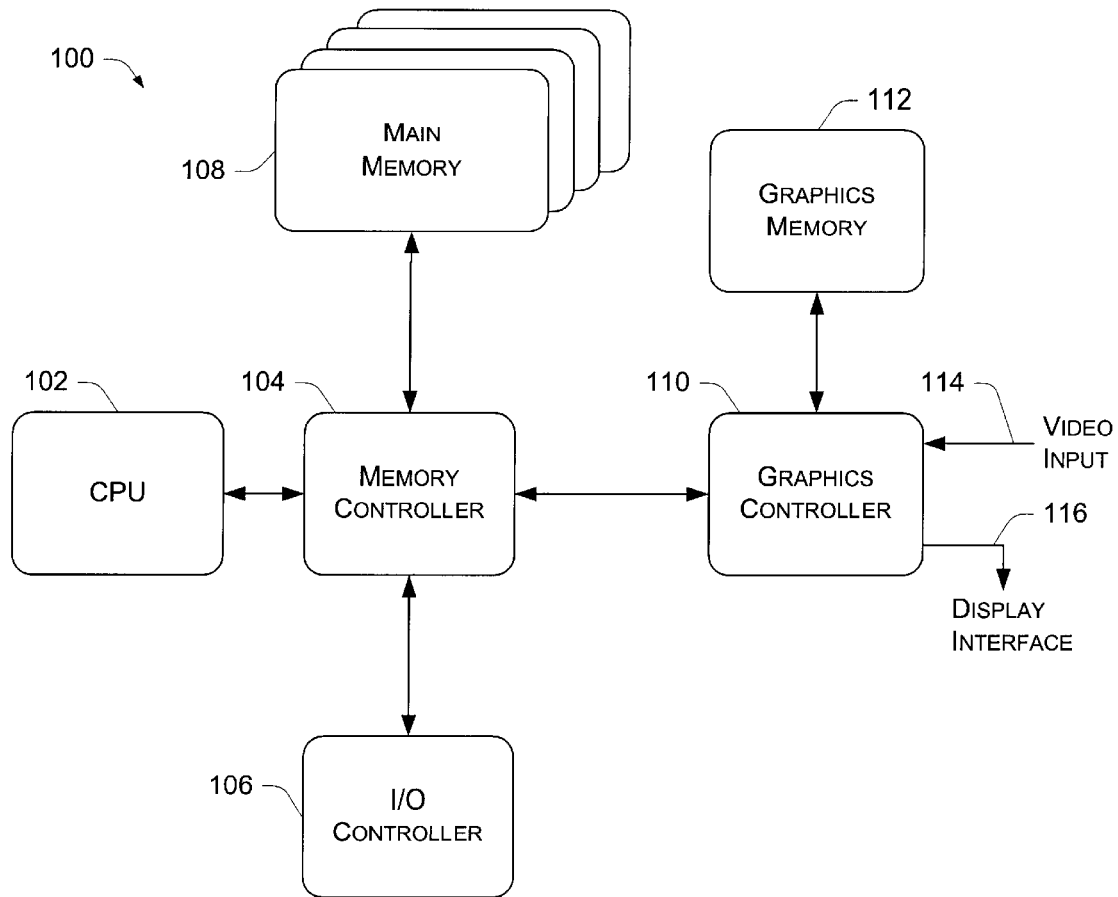


Fig. 1
(Prior Art)

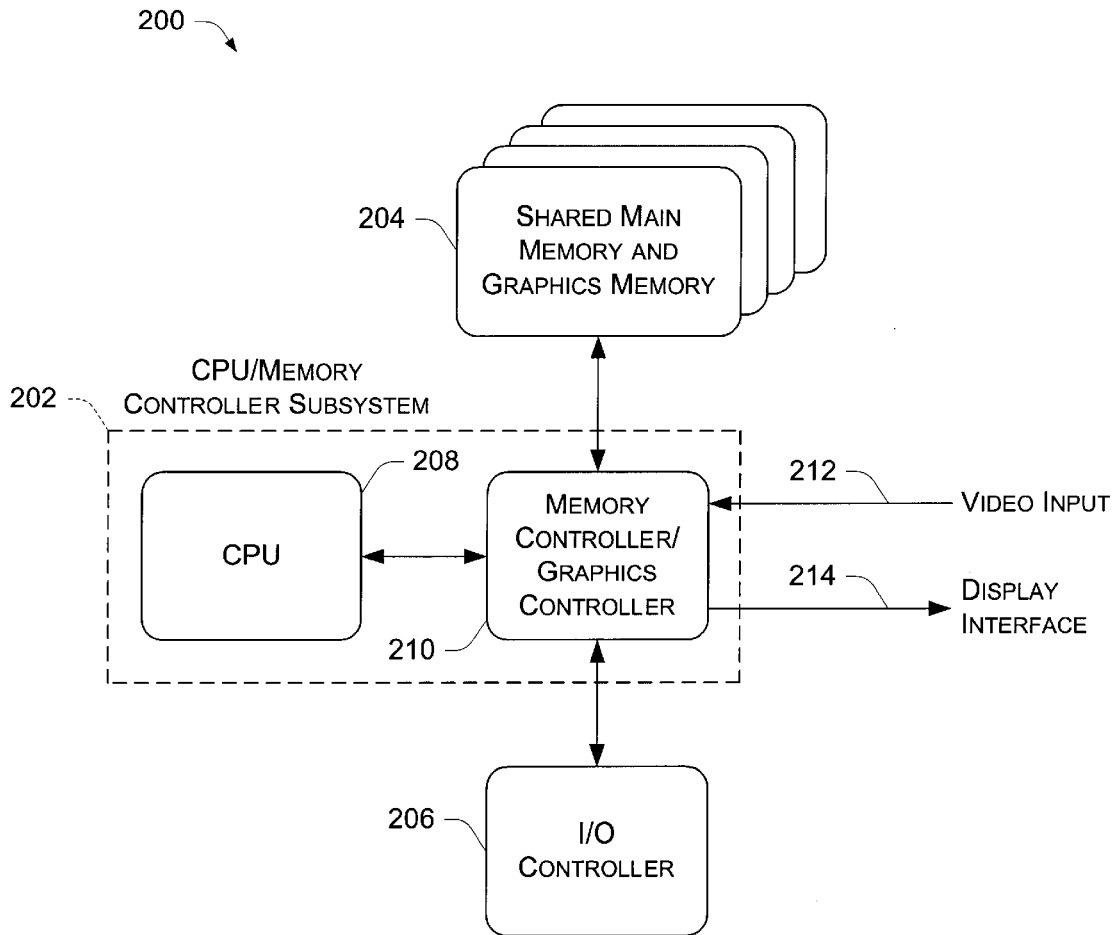


Fig. 2
(Prior Art)

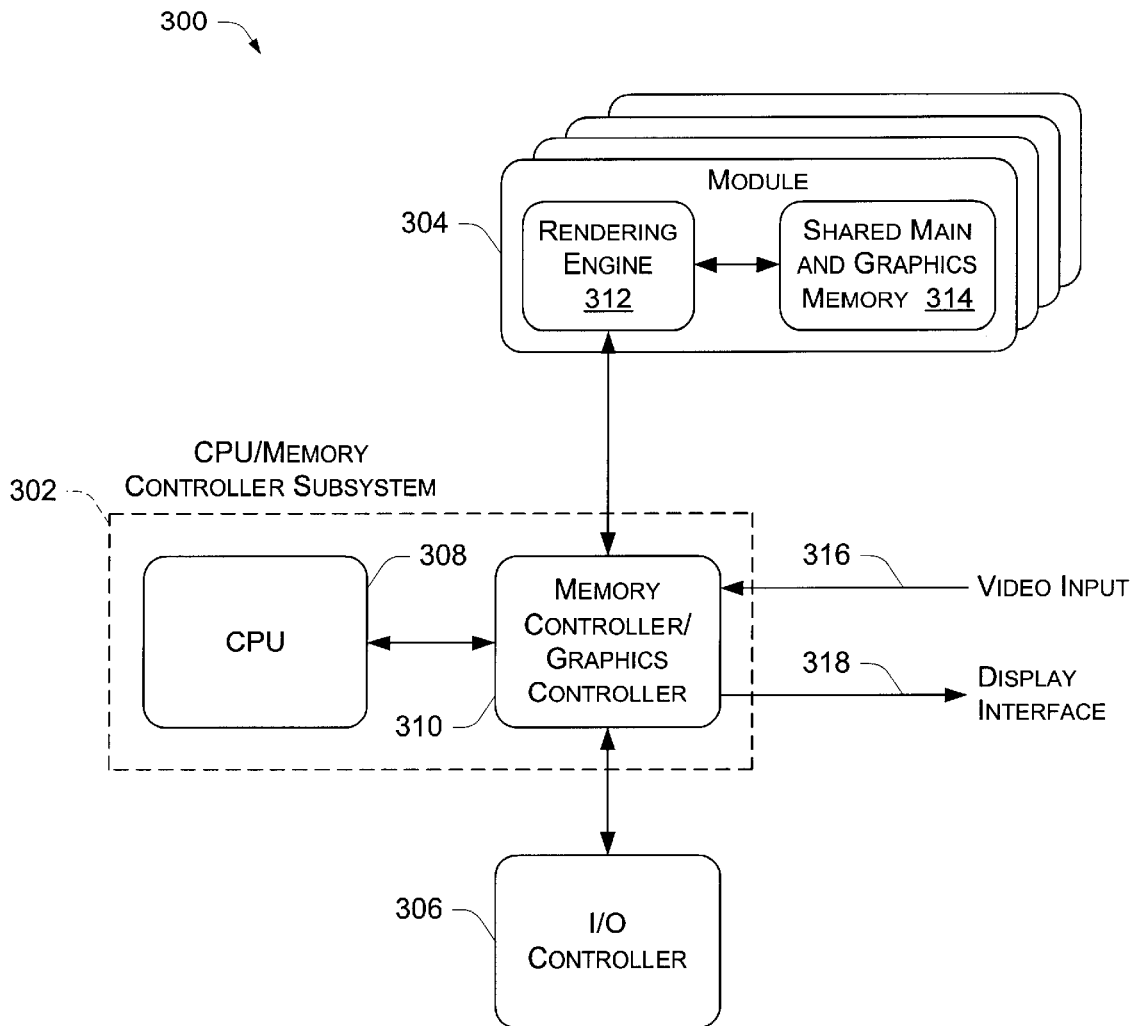


Fig. 3

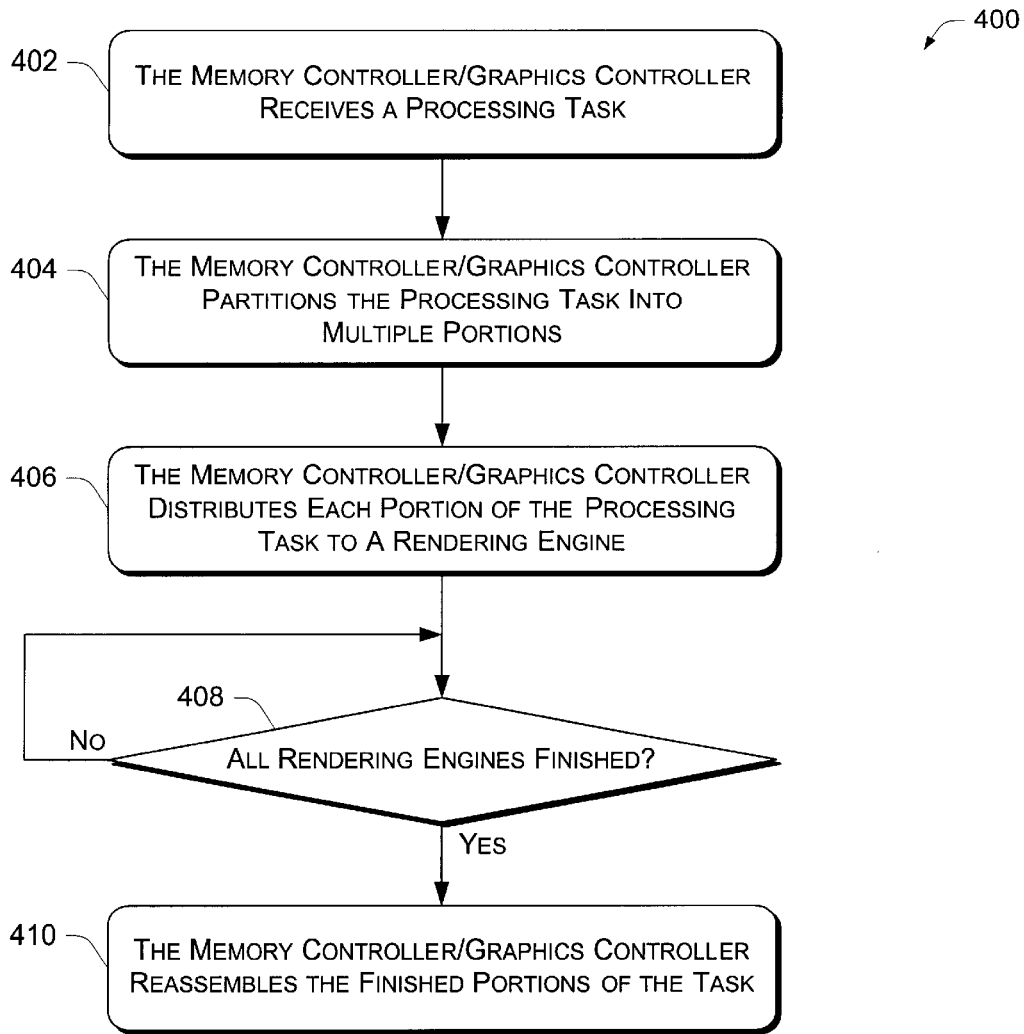


Fig. 4

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