06-13-3

10459797 .061203

A 4 B

PTO/SB/05 (05-03)
Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control numbe

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	00100.02.0053
First Inventor	Mark M. Leather
Title	Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique
Express Mail Label No.	EV 063310627 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria VA 22313-1450**

1. [x] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [x] Specification [*Total Pages* 21] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [x] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 5]
5. Oath or Declaration [*Total Sheets* 2]
   a. [x] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Reader Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [x] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [x] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1499 [ ] Copies of IDS Citations
13. [x] Preliminary Amendment
14. [x] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other: .....

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

For CONTINUATION OF DIVISIONAL APPS only; The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* OR [x] *Correspondence address below*

Name	Christopher J. Reckamp				
Address	Vedder, Price, Kaufman & Kammholz 222 North LaSalle Street				
City	Chicago	*State*	IL	*Zip Code*	60601
Country	U.S.A.	*Telephone*	312-609-7599	*Fax*	312-609-500

Name (Print/Type)	Christopher J. Reckamp	*Registration No. (Attorney/Agent)*	34,414
Signature	C. J. Reckamp	*Date*	06/12/03

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

1083973

[redacted]

10159797_061203

06/12/03 17611 U.S. PTO

PTO/SB/17 (01-03)
Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 862.00

Complete if Known	
Application Number	
Filing Date	6/12/03
First Named Inventor	Mark M. Leather
Examiner Name	
Art Unit	
Attorney Docket No.	00100.02.0053

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0441

Deposit Account Name: ATI Technologies Inc.

The Commissioner is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	750.00
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 750.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims	Fee from below	Fee Paid
Total Claims	24	-20** = 4	X 18	= 72.00
Independent Claims	3	- 3** = 0	X 0	= 0.00
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 72.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	40.00
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Christopher J. Reckamp	*Registration No. (Attorney/Agent)*	34,414	*Telephone*	312-609-7598
Signature	Christopher J. Reckamp			*Date*	6/12/03

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

1084014

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

[redacted]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Leather et al. Examiner:

Serial No.: Art Group:

Filing Date: June 12, 2003 Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Express Mail
I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10, on the date indicated and is addressed to Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450,
Express Mail No. EV 063310627 US.

06/12/03 Winona K. Jackson
Date *Winona K. Jackson*

PRELIMINARY AMENDMENT

Dear Sir:

Prior to examination, Applicants respectfully request that the above-identified application be amended as follows:

In The Specification:

Please add the following new paragraph directly below the invention title on page 1 of the specification as follows:

This application claims the benefit of U. S. Provisional Application Ser. No. 60/429,641 filed November 27, 2002, entitled "Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique", having as inventors Mark M. Leather and Eric Demers, and owned by instant assignee.

REMARKS

Applicants submit that the specification is fully supported by the original provisional application, and the claims are fully supported by the originally filed provisional application.

Respectfully submitted,

By: _____
Christopher J. Reckamp
Reg. No. 34,414

Dated: June 12, 2003

Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
Telephone: (312) 609-7500
Facsimile: (312) 609-5005

[redacted]

10459797 .061203

020053

PATENT APPLICATION
ATTY. DOCKET NO. 00100.02.0053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

INVENTORS:

Mark M. Leather 12187 Woodside Drive Saratoga, California 95070	Eric Demers 901 Sycamore Drive Palo Alto, California 94303

ATTORNEY OF RECORD:
CHRISTOPHER J. RECKAMP
REGISTRATION NO. 34,414
VEDDER PRICE KAUFMAN & KAMMHOLZ
222 NORTH LASALLE STREET, SUITE 2600
CHICAGO, ILLINOIS 60601
PHONE (312) 609-7500
FAX (312) 609-5005

Express Mail Label No.: EV 063310627 US

Date of Deposit: June 12, 2003

I hereby certify that this paper is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to: Mail Stop Patent Application, Commissioner of Patents, P. O. Box 1450, Alexandria, VA, 22313-1450.

Name of Depositor: Winona K. Jackson

Signature: Winona K. Jackson

[redacted]

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

RELATED CO-PENDING APPLICATION

[0001] This is a related application to a co-pending application entitled "Parallel Pipeline Graphics System" having docket number 010025, having serial number _____, having Leather et al. as the inventors, filed on even date, owned by the same assignee and hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0001] The present invention generally relates to graphics processing circuitry and, more particularly, to dividing graphics processing operations among multiple pipelines.

BACKGROUND OF THE INVENTION

[0002] Computer graphics systems, set top box systems or other graphics processing systems typically include a host processor, graphics (including video) processing circuitry, memory (e.g. frame buffer), and one or more display devices. The host processor may have a graphics application running thereon, which provides vertex data for a primitive (e.g. triangle) to be rendered on the one or more display devices to the graphics processing circuitry. The display device, for example, a CRT display includes a plurality of scan lines comprised of a series of pixels. When appearance attributes (e.g. color, brightness, texture) are applied to the pixels, an object or scene is presented on the display device. The graphics processing circuitry receives the vertex data and generates pixel data including the appearance attributes which may be presented on the display device according to a particular protocol. The pixel data is typically stored in the frame buffer in a manner that corresponds to the pixels location on the display device.

[0003] FIG. 1 illustrates a conventional display device 10, having a screen 12 partitioned into a series of vertical strips 13-18. The strips 13-18 are typically 1-4 pixels in width. In like manner, the frame buffer of conventional graphics processing systems is partitioned into a series of vertical strips having the same screen space width.

Alternatively, the frame buffer and the display device may be partitioned into a series of horizontal strips. Graphics calculations, for example, lighting, color, texture and user viewing information are performed by the graphics processing circuitry on each of the primitives provided by the host. Once all calculations have been performed on the primitives, the pixel data representing the object to be displayed is written into the frame buffer. Once the graphics calculations have been repeated for all primitives associated with a specific frame, the data stored in the frame buffer is rendered to create a video signal that is provided to the display device.

[0004] The amount of time taken for an entire frame of information to be calculated and provided to the frame buffer becomes a bottleneck in graphics systems as the calculations associated with the graphics become more complicated. Contributing to the increased complexity of the graphics calculation is the increased need for higher resolution video, as well as the need for more complicated video, such as 3-D video. The video image observed by the human eye becomes distorted or choppy when the amount of time taken to render an entire frame of video exceeds the amount of time in which the display device must be refreshed with a new graphic or frame in order to avoid perception by the human eye. To decrease processing time, graphics processing systems typically divide primitive processing among several graphics processing circuits where, for example, one graphics processing circuit is responsible for one vertical strip (e.g. 13) of the frame while another graphics processing circuit is responsible for another vertical strip (e.g. 14) of the frame. In this manner, the pixel data is provided to the frame buffer within the required refresh time.

[0005] Load balancing is a significant drawback associated with the partitioning systems as described above. Load balancing problems occur, for example, when all of the primitives 20-23 of a particular object or scene are located in one strip (e.g. strip 13) as illustrated in FIG. 1. When this occurs, only the graphics processing circuit responsible strip 13 is actively processing primitives; the remaining graphics processing circuits are idle. This results in a significant waste of computing resources as at most only half of the graphics processing circuits are operating. Consequently, graphics processing system performance is decreased as the system is only operating at a maximum of fifty percent capacity.

[0006] Changing the width of the strips has been employed to counter the system performance problems. However, when the width of a strip is increased, the load balancing problem is enhanced as more primitives are located within a single strip; thereby, increasing the processing required of the graphics processing circuit responsible for that strip, while the remaining graphics processing circuits remain idle. When the width of the strip is decreased (e.g. four bits to two bits), cache (e.g. texture cache) efficiency is decreased as the number of cache lines employed in transferring data is reduced in proportion to the decreased width of the strip. In either case, graphics processing system performance is still decreased due to the idle graphics processing circuits.

[0007] Frame based subdivision has been used to overcome the performance problems associated with conventional partitioning systems. In frame based subdivision, each graphics processor is responsible for processing an entire frame, not strips within the same frame. The graphics processors then alternate frames. However, frame subdivision introduces one or more frames of latency between the user and the screen, which is unacceptable in real-time interactive environments, for example, providing graphics for a flight simulator application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention and the related advantages and benefits provided thereby, will be best appreciated and understood upon review of the following detailed description of a preferred embodiment, taken in conjunction with the following drawings, where like numerals represent like elements, in which:

[0009] FIG. 1 is a schematic block diagram of a conventional display partitioned into several vertical strips:

[0010] FIG. 2 is a schematic block diagram of a graphics processing system employing an exemplary multi-pipeline graphics processing circuit according to one embodiment of the present invention;

[0011] FIG. 3 is a schematic block diagram of a memory partitioned into an exemplary super-tile pattern according to the present invention;

[0012] FIG. 4 is a schematic block diagram of a memory partitioned into a super-tile pattern according to an alternate embodiment of the present invention;

[0013] FIG. 5 is a schematic block diagram of an exemplary multi-pipeline graphics processing circuit used in a multi processor configuration according to an alternate embodiment of the present invention;

[0014] FIG. 6 is a flow chart of the operations performed by the graphics processing circuit according to the present invention;

[0015] FIG. 7 is a diagram illustrating a polygon bounding box to determine which, if a polygon fits in a tile or super tile; and

[0016] FIG. 8 is a schematic block diagram of an exemplary multi-pipeline graphics processing circuit used in a multi processor configuration according to an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0017] A multi-pipeline graphics processing circuit includes at least two pipelines operative to process data in a corresponding tile of a repeating tile pattern, a respective one of the at least two pipelines is operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. The multi-pipeline graphics processing circuit may be coupled to a frame buffer that is subdivided into a replicating pattern of square regions (e.g. tiles), where each region is processed by a corresponding one of the at least two pipelines such that load balancing and texture cache utilization is enhanced.

[0018] A multi-pipeline graphics processing method includes receiving vertex data for a primitive to be rendered, generating pixel data in response to the vertex data, determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines. An exemplary embodiment of the present invention will now be described with reference to Figures 2-6.

[0019] FIG. 2 is a schematic block diagram of an exemplary graphics processing system 30 employing an example of a multi-pipeline graphics processing circuit 34 according to one embodiment of the present invention. The graphics processing system 30 can be implemented with a single graphics processing circuit 34 or with two or more graphics processing circuits 34, 54. The components and corresponding functionality of the graphics processing circuits 34, 54 are substantially the same. Therefore, only the structure and operation of graphics processing circuit 34 will be described in detail. An alternate embodiment, employing both graphics processing circuits 34 and 54 will be discussed in greater detail below with reference to FIGS. 4-5.

[0020] Graphics data 31, for example, vertex data of a primitive (e.g. triangle) 80 (FIG. 3) is transmitted as a series of strips to the graphics processing circuit 34. As used herein, graphics data 31 can also include video data or a combination of video data and graphics data. The graphics processing circuit 34 is preferably a portion of a stand-alone graphics processor chip or may also be integrated with a host processor or other circuit, if

desired, or part of a larger system. The graphics data 31 is provided by a host (not shown). The host may be a system processor (not shown) or a graphics application running on the system processor. In an alternate embodiment, an Accelerated Graphics Port (AGP) 32 or other suitable port receives the graphics data 31 from the host and provides the graphics data 31 to the graphics processing circuit 34 for further processing.

[0021] The graphics processing circuit 34 includes a first graphics pipeline 101 operative to process graphics data in a first set of tiles as discussed in greater detail below. The first pipeline 101 includes front end circuitry 35, a scan converter 37, and back end circuitry 39. The graphics processing circuit 34 also includes a second graphics pipeline 102, operative to process graphics data in a second set of tiles as discussed in greater detail below. The first graphics pipeline 101 and the second graphics pipeline 102 operate independently of one another. The second graphics pipeline 102 includes the front end circuitry 35, a scan converter 40, and back end circuitry 42. Thus, the graphics processing circuit 34 of the present invention is configured as a multi-pipeline circuit, where the back end circuitry 39 of the first graphics pipeline 101 and the back end circuitry 42 of the second graphics pipeline 102 share the front end circuitry 35, in that the first and second graphics pipelines 101 and 102 receive the same pixel data 36 provided by the front end circuitry 35. Alternatively, the back end circuitry 39 of the first graphics pipeline 101 and the back end circuitry 42 of the second pipeline 102 may be coupled to separate front end circuits. Additionally, it will be appreciated that a single graphics processing circuit can be configured in similar fashion to include more than two graphics pipelines. The illustrated graphics processing circuit 34 has the first and second pipelines 101-102 present on the same chip. However, in alternate embodiments, the first and second graphics pipelines 101-102 may be present on multiple chips interconnected by suitable communication circuitry or a communication path, for example, a synchronization signal or data bus interconnecting the respective memory controllers.

[0022] The front end circuitry 35 may include, for example, a vertex shader, set up circuitry, rasterizer or other suitable circuitry operative to receive the primitive data 31 and generate pixel data 36 to be further processed by the back end circuitry 39 and 42, respectively. The front end circuitry 35 generates the pixel data 36 by performing, for example, clipping, lighting, spatial transformations, matrix operations and rasterizing

operations on the primitive data 31. The pixel data 36 is then transmitted to the respective scan converters 37 and 40 of the two graphics pipelines 101-102.

[0023] The scan converter 37 of the first graphics pipeline 101 receives the pixel data 36 and sequentially provides the position (e.g. x, y) coordinates 60 in screen space of the pixels to be processed by the back end circuitry 39 by determining or identifying those pixels of the primitive, for example, the pixels within portions 81-82 of the triangle 80 (FIG. 3) that intersect the tile or set of tiles that the back end circuitry 39 is responsible for processing. The particular tile(s) that the back end circuitry 39 is responsible for is determined based on the tile identification data present on the pixel identification line 38 of the scan converter 37. The pixel identification line 38 is illustrated as being hard wired to ground. Thus, the tile identification data corresponds to a logical zero. This corresponds to the back end circuitry 39 being responsible for processing the tiles labeled "A" (e.g. 72 and 75) in FIG. 3. Although the pixel identification line 38 is illustrated as being hard wired to a fixed value, it is to be understood and appreciated that the tile identification data can be programmable data, for example, from a suitable driver and such a configuration is contemplated by the present invention and is within the spirit and scope of the instant disclosure.

[0024] Back end circuitry 39 may include, for example, pixel shaders, blending circuits, z-buffers or any other circuitry for performing pixel appearance attribute operations (e.g. color, texture blending, z-buffering) on those pixels located, for example, in tiles 72, 75 (FIG. 3) corresponding to the position coordinates 60 provided by the scan converter 37. The processed pixel data 43 is then transmitted to graphics memory 48 via memory controller 46 for storage therein at locations corresponding to the position coordinates 60.

[0025] The scan converter 40 of the second graphics pipeline 102, receives the pixel data 36 and sequentially provides position (e.g. x, y) coordinates 61 in screen space of the pixels to be processed by the back end circuitry 42 by determining those pixels of the primitive, for example, the pixels within portions 83-84 of the triangle 80 (FIG. 3) that intersect the tiles that the back end circuitry 42 is responsible for processing. Back end circuitry 42 tile responsibility is determined based on the tile identification data present on the pixel identification line 41 of the scan converter 41. The pixel

identification line 41 is illustrated as being hard wired to V_{CC}; thus, the tile identification data corresponds to a logical one. This corresponds to the back end circuitry 42 being responsible for processing the tiles labeled "B" (e.g. 73-74) in FIG. 3. Although the pixel identification line 41 is illustrated as being hard wired to a fixed value, it is to be understood and appreciated that the tile identification data can be programmable data, for example, from a suitable driver and such configuration is contemplated by the present invention and is within the spirit and scope of the instant disclosure.

[0026] Back end circuitry 42 may include, for example, pixel shaders, blending circuits, z-buffers or any suitable circuitry for performing pixel appearance attribute operations on those pixels located, for example, in tiles 73 and 74 (FIG. 3) corresponding to the position coordinates 61 provided by the scan converter 40. The processed pixel data 44 is then transmitted to the graphics memory 48, via memory controller 46, for storage therein at locations corresponding to the position coordinates 61.

[0027] The memory controller 46 is operative to transmit and receive the processed pixel data 43-44 from the back end circuitry 39 and 42; transmit and retrieve pixel data 49 from the graphics memory 48; and in a single circuit implementation, transmit pixel data 50 for presentation on a suitable display 51. The display 51 may be a monitor, a CRT, a high definition television (HDTV) or any other device or combination thereof.

[0028] Graphics memory 48 may include, for example, a frame buffer that also stores one or more texture maps. Referring to FIG. 3, the frame buffer portion of the graphics memory 48 is partitioned in a repeating tile pattern of horizontal and vertical square regions or tiles 72-75, where the regions 72-75 provide a two dimensional partitioning of the frame buffer portion of the memory 48. Each tile is implemented as a 16 x 16 pixel array. The repeating tile pattern of the frame buffer 48 corresponds to the partitioning of the corresponding display 51 (FIG. 2). When rendering a primitive (e.g. triangle) 80, the first graphics pipeline 101 processes only those pixels in portions 81, 82 of the primitive 80 that intersects tiles labeled "A", for example, 72 and 75, as the back end circuitry 39 is responsible for the processing of tiles corresponding to tile identification 0 present on pixel identification line 38 (FIG. 2). In corresponding fashion, the second graphics pipeline 102 processes only those pixels in portions 83, 84 of the

primitive 80 that intersects tiles labeled "B", for example 73-74, as the back end circuitry 42 (FIG. 2) is responsible for the processing of tiles corresponding to tile identification 1 present on pixel identification line 41 (FIG. 2).

[0029] By configuring the frame buffer 48 according to the present invention, as the primitive data 31 is typically written in strips, the tiles (e.g. 72 and 75) being processed by the first graphics pipeline 101 and the tiles (e.g. 73 and 74) being processed by the second graphics pipeline 102 will be substantially equal in size, notwithstanding the primitive 80 orientation. Thus, the amount of processing performed by the first graphics pipeline 101 and the second graphics pipeline 102, respectively, are substantially equal; thereby, effectively eliminating the load balance problems exhibited by conventional techniques.

[0030] FIG. 4 is a schematic block diagram of a frame buffer 68 partitioned into a super-tile pattern according to an alternate embodiment of the present invention. Such a partitioning would be used, for example, in conjunction with a multi-processor implementation to be discussed below with reference to FIG. 5. As illustrated, the frame buffer 68 is partitioned into a repeating tile pattern where the tiles, for example, 92-99 that form the repeating tile pattern are the responsibility of and processed by a corresponding one of the graphics pipelines provided by the multi-processor implementation.

[0031] FIG. 5 is a schematic block diagram of a graphics processing circuit 54 which may be coupled with the graphics processing circuit 34 (FIG. 2), for example, by the AGP 32 or other suitable port, to form one embodiment of a multi-processor implementation. The graphics processing circuit 54 is preferably a portion of a stand-alone graphics processor chip or may also be integrated with a host processor or other circuit, if desired, or port of a larger system. The multi-processor implementation exhibits an increased fill rate of, for example, 9.6 billion pixels/sec with a triangle rate of 300 million triangles/sec. This represents a tremendous performance increase as compared to conventional graphics processing systems. The triangle rate is defined as the number of triangles the graphics processing circuit can generate per second. The fill rate is defined as the number of pixels the graphics processing circuit can render per second.

[0032] Referring briefly to FIG. 2, in the multi-processor implementation, processed pixel data 52 from the graphics processing circuit 34 is provided as a first of two inputs to a high speed switch 70. The second input to the high speed switch 70 is the processed pixel data 55 from the graphics processing circuit 54. The high speed switch 70 has a switching frequency (f) sufficient to provide the pixel information 71 to a suitable display device without any detectable latency.

[0033] Returning to FIG. 5, the graphics processing circuit 54 includes a third graphics pipeline 201 operative to process graphics data in a third set of tiles. The third graphics pipeline 201 includes front end circuitry 135, which may be the front end circuitry 35 discussed with reference to FIG. 2, a scan converter 137 and back end circuitry 139. The graphics processing circuit 54 also includes a fourth graphics pipeline 202, operative to process graphics data in a fourth set of tiles. The fourth graphics pipeline 202 includes the front end circuitry 135, a scan converter 140 and back end circuitry 142. The third graphics pipeline 201 and the fourth graphics pipeline 202 also operate independently of one another. Thus, the graphics processing circuit 54 is configured as a multi-pipeline circuit, where the back end circuitry 139 of the third graphics pipeline 201 and the back end circuitry 142 of the fourth graphics pipeline 202 share the front end circuitry 135, in that the respective back end circuitry 139 and 142 receives the same pixel data from the front end circuitry 135. As illustrated, the components of the third and fourth graphics pipelines are present on a single chip. Additionally, the back end circuitry 139 and the back end circuitry 142 may be configured to share the front end circuitry 35 of the graphics processing circuit 34. Alternatively, the third and fourth graphics pipelines may be configured to be on multiple chips interconnected by a communication path, for example, a synchronization signal or data bus.

[0034] The front end circuitry 135 may include, for example, a vertex shader, set up circuitry, rasterizer or other suitable circuitry operative to receive the primitive data 31 from the AGP 32 and generate pixel data 136 to be processed by the third graphics pipeline 201 and fourth graphics pipeline 202, respectively. The front end circuitry 135 generates the pixel data 136 by performing, for example, clipping, lighting, spatial transformations, matrix operations, rasterization or any suitable primitive operations or

combination thereof on the primitive data 31. The pixel data 136 is then transmitted to the respective scan converters 137 and 140 of the two graphics pipelines 201-202.

[0035] The scan converter 137 of the third graphics pipeline 201 receives the pixel data 136 and sequentially provides the position (e.g. x, y) coordinates 160 in screen space of the pixels to be processed by the back end circuitry 139, based on the tile identification data present on pixel identification line 138. In corresponding fashion, scan converter 140 of the fourth graphics pipeline 202 receives the pixel data 136 and sequentially provides the position (e.g. x, y) coordinates 161 in screen space of the pixels to be processed by the back end circuitry 143, based on the tile identification data present on pixel identification line 141.

[0036] Referring to FIG. 4, in the multi-processor implementation, when a logical zero or other suitable value is present on pixel identification line 138 (e.g. corresponding to the pixel identification line 138 being tied to ground), the back end circuitry 139 is responsible for processing, for example, tiles labeled "A0" (e.g. 92 and 95). In corresponding manner, when a logical one or other suitable value is present on pixel identification line 141 (e.g. corresponding to pixel identification line 142 being tied to V_{CC}), the back end circuitry 142 will be responsible for processing the tiles labeled "B0" (e.g. 93 and 94). When a logical zero or other suitable value is present on pixel identification line 38 (FIG. 2), the back end circuitry 39 is responsible for processing, for example, the tiles labeled "A1" (e.g. 96 and 99). When a logical one or other suitable value is present on pixel identification line 41 (FIG. 2), the back end circuitry 42 is responsible for processing, for example, the tiles labeled "B1" (e.g. 97 and 98). The tile pattern illustrated in FIG. 4 is referred to as a super-tile pattern 68.

[0037] As illustrated, the super-tile pattern 68 is formed of a horizontally and vertically repeating pattern of regions or tiles 92-99, where each tile is a 16 x 16 pixel array. With this frame buffer configuration, as the primitive data 31 is typically written in strips, at least one tile (e.g. 92) being processed by the third graphics pipeline 201 and at least one tile (e.g. 93) being processed by the fourth graphics pipeline 202 will be intersected or contain at least a portion of the primitive data 31, notwithstanding the primitive orientation; thereby achieving substantially equal load balancing between the pipelines.

[0038] Thus, in the multi-processor implementation, each of the graphics pipelines is responsible for processing 1/(MxN) of the tiles present in the partitioned graphics memory 68, where M represents the number of pipelines per circuit and N represents the number of graphics processing circuits being used. Thus, in an embodiment where graphics processing circuit 34 and graphics processing circuit 54 are combined, for example, through AGP 32 (FIG. 2), each graphics pipeline 101, 102, 201 and 202 will be responsible for processing one-fourth of the tiles 92-99 of the repeating tile pattern. This results in increased graphics processing performance as each graphics pipeline is responsible for processing one-quarter of total pixels maintained in the frame buffer 68.

[0039] FIG. 6 is a flow chart of the operations performed by the graphics processing circuit 34 according to the present invention. In the multi-processor implementation, graphics processing circuits 34 and 54 perform substantially the same operations. In step 100, the front end circuitry 35 receives the graphics data 31 (FIG. 2), for example, vertex data of an object to be rendered and generates corresponding pixel data 36 (FIG. 2) in response to the primitive data 31 in step 102. The pixel data may be generated by performing, for example, clipping, lighting, spatial transformations. matrix transformations and rasterizing operations on the graphics data 31.

[0040] In step 104, the pixels within a set of tiles of the repeating tile pattern to be processed by a corresponding one of the at least two graphics pipelines in response to the pixel data is determined. This is accomplished, for example, in step 105 by the scan converter 37 determining which of tiles (e.g. 72 and 75) of the repeating tile pattern are to be processed by the back end circuitry 39 based on the tile identification data present on the pixel identification line 38. Next, in step 106, the scan converter 37 provides the position coordinates 60 of the pixels within portions 81-82 of the triangle 80 that intersect the tiles (e.g. 72 and 75) to the back end circuitry 39.

[0041] In step 108, pixel operations are performed on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines is performed. This is accomplished, for example, by the back end circuitry 39 performing color, shading, blending, texturing and/or z-buffering operations on the pixels within the portions (e.g. 81-82) of the tiles (e.g. 72 and 75) they are responsible for.

[0042] In step 109, a determination is made as to whether the processing is complete. If the processing is complete, the process proceeds to step 100 where vertex data for a new primitive is received. Otherwise, the process ends. In the multi-processor implementation, graphics processing circuit 54 performs substantially the same operations as discussed above, in conjunction with graphics processing circuit 34.

[0043] As noted above, a rasterizer setup unit manages the distribution of polygons to the different rasterizer pipelines within a chip. The design divides the screen into multiple square tiles. Each pipeline is responsible for a subset of the tiles. In our design, the tile sizes are 8 x 8 pixels, 16x16 pixels (default) or 32x32 pixels. However, any number of square pixels or even non-square tiles could be done. It will be recognized that the number of pixels in the tiles be a common divisor of the number of pixels on the screen, in both X and Y directions.

[0044] Vertices are given by the application currently executing on the host. The vertices are converted from object space three-dimensional homogeneous coordinate system to a screen based coordinate system. This conversion can be done on the host processor or in the front end section of the graphics chip (i.e. vertex transformation). The screen based coordinate system has at least X and Y coordinates for each vertex.

[0045] As shown in FIG. 7, the setup unit creates a bounding box based on the screen space X, Y coordinates of each vertex. This bounding box is then compared against the current tile pattern. This tiling pattern is based on the number of graphics pipelines currently active. In the one pipe configuration, the tiles just repeat and are all mapped to the same pipeline. In the two pipe configuration, a "checkerboard" pattern is created for the pipes and the patterns repeat over the full screen.

[0046] The bounding boxes' four corners are mapped to the tile pattern, simply by discarding the lower bits of X & Y. The four corners map to the same or different tiles. If they all map to the same tile, then only the pipeline that is associated with that tile receives the polygon. If it maps to only tiles that are associated with only one pipeline, then again only that pipeline receives the polygon. If it maps to tiles that are associated with multiple pipelines, then the entire polygon is sent to all pipelines. In our implementation, we broadcast the polygon to all pipelines, masking the pipelines that

should not receive it. Consequently, polygons can be sent to only one pipe or up to all the pipes, depending on the coverage of the tiles by the polygon.

[0047] For super tiling when using multiple graphics chips, the rasterizer setup unit manages the distribution of polygons to different graphics chips. The super tiles, which are a square assembly of pixels, are used to perform load balancing between each processor. Basically, each processor is responsible for generating all of the pixels in its subset of super tiles. The tiles are distributed evenly across all processors, in a checkerboard pattern. The tile size is variable, but one implementation may be 32x32 pixels, or 2x2 tiles. This amount can be changed through programming registers. Super tiles do not have to be of a size which is a common divisor of the screen resolution, but it's more efficient if it is. The number of chips in use should be a power of two.

[0048] FIG. 8 shows some examples of super tile configurations for various numbers of chips (super tile size or STS). As shown, C# represents the tile that chip # controls. The patterns repeat across the whole screen, in both X & Y directions, until the full screen is fully covered. For odd powers of 2 (STS=2, STS=8), a simple square pattern of different chips cannot be made, so a secondary pattern of checkerboard is applied to generate a square arrangement.

[0049] In operation, an application generates vertex data, which assembles into polygons (i.e. 2 vertices for a line, 3 for a triangle). Each vertex's homogeneous object space coordinate (generated by the application) is transformed into screen space coordinates by either the host or the front end of the graphics chip (transform unit or vertex processor). The screen space coordinates hold X, Y coordinates (in screen pixels) for each of the vertices. The polygons coming from an application are all broadcast to all chips. Each chip processes the vertices as needed to generate the same X, Y coordinates for all vertices. Then, each chip creates a bounding box around the polygon as shown in FIG. 7. The X, Y coordinates of each corner of the bounding box is checked against the super tiles that belongs to each processor. If the bounding box overlaps a super tile assigned to a given processor, then that processor must render some or the entire polygon. The setup unit then sends the whole polygon to the various raster pipe(s). If the bounding box does not overlap any of the tiles associated with a processor, then the setup unit rejects the whole polygon and processes the next one.

[0050] In this way, triangle setup performance does not scale with each processor (since all polygons go through all setup units), but fill rate (defined as the number of pixels output total) does scale with each processor added.

[0051] The above detailed description of the invention and the examples described therein have been provided for the purposes of illustration and description. Although an exemplary embodiment of the present invention has been described in detail herein with reference to the accompanying drawings, it is to be understood that the present invention is not limited to the precise embodiment disclosed, and that various changes and modifications to the invention are possible in light of the above teaching. Accordingly, the scope of the present invention is to be defined by the claims appended hereto.

CLAIMS

What is claimed is:

1. A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics pipeline, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory.

10. The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the pixel data only in a second set of tiles in the repeating tile pattern.

13. The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

24. A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles or the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry. operative to receive transmit and receive the processed pixel data.

DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

ABSTRACT

A graphics processing circuit includes at least two pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. A graphics processing method includes receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data; determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

DIVIDING WORK AM ONG MULTIPLE GRAPHICS PIPELINES
USING A SUPER-TILING TECHNIQUE
Inventor: Leather, et al.

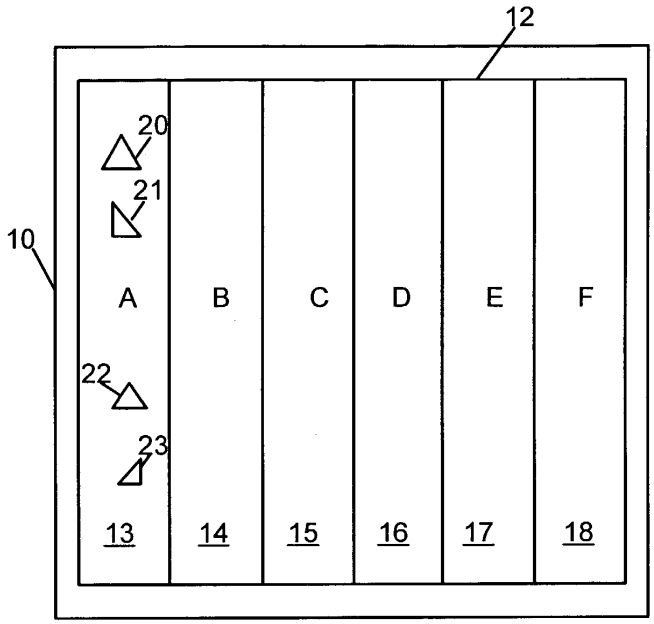


FIG. 1
PRIOR ART

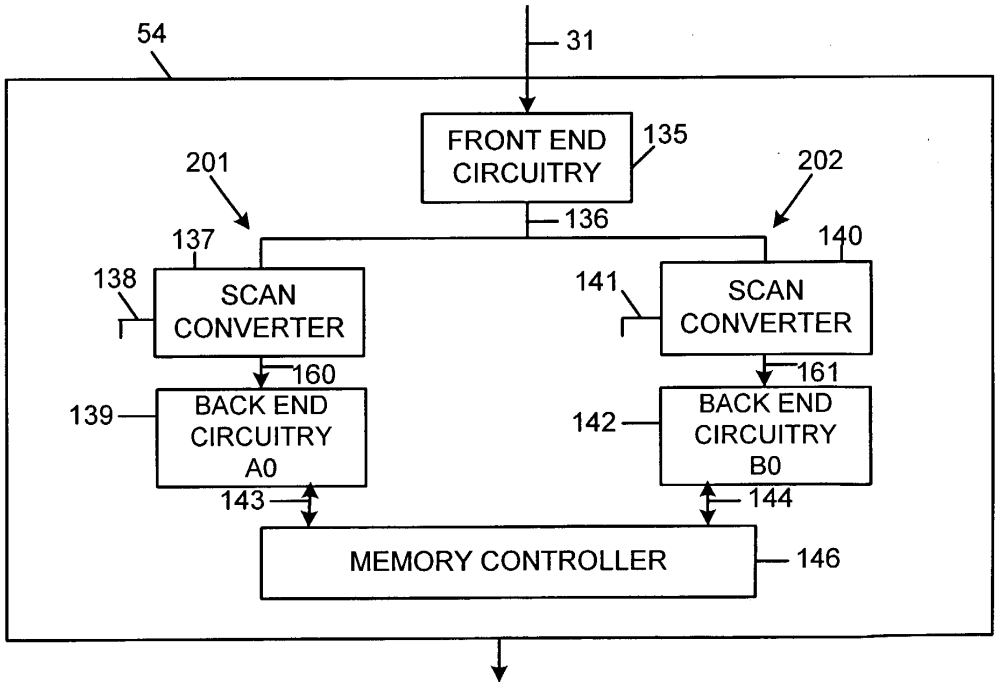


FIG. 5

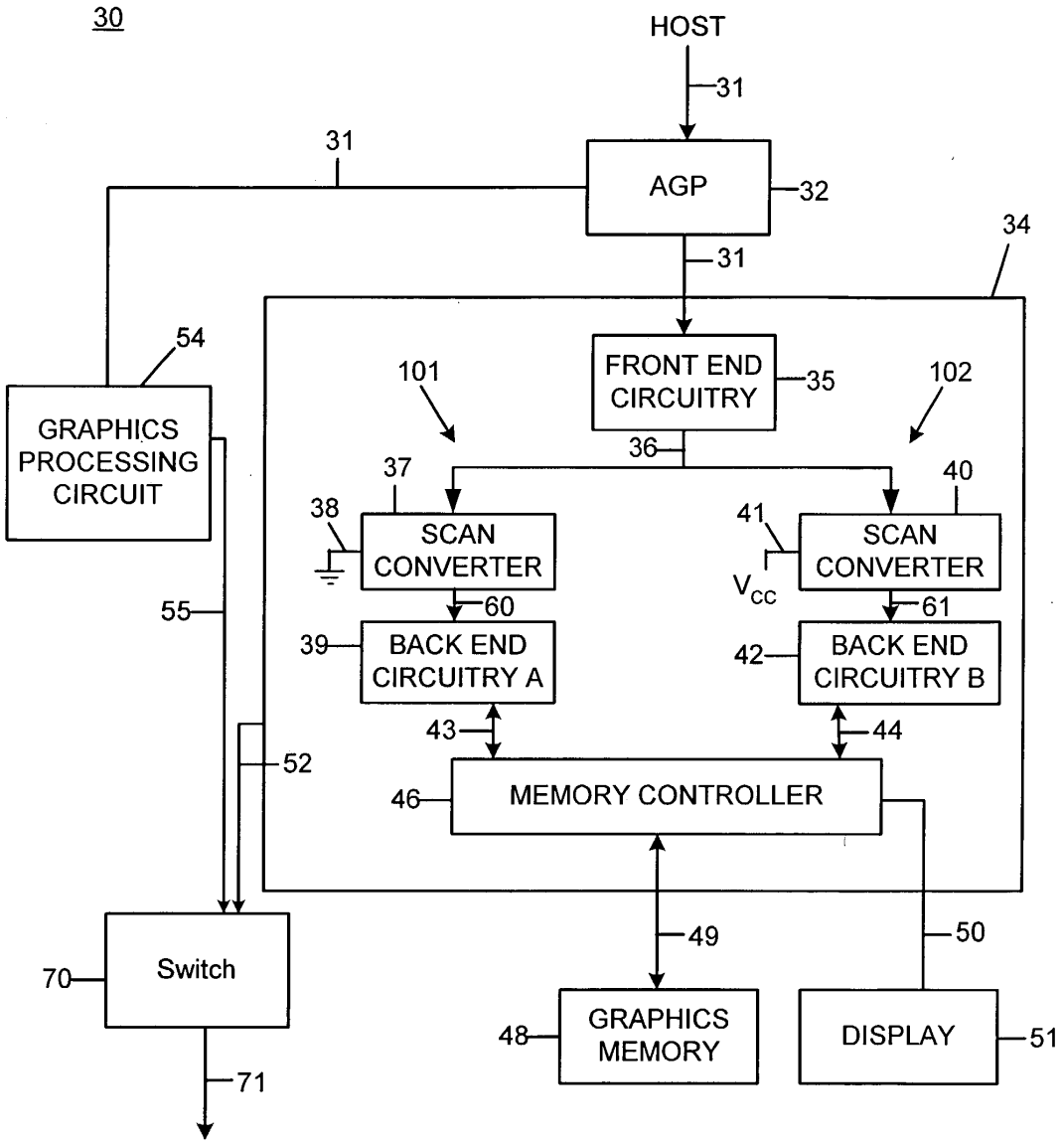

30
HOST
31
AGP
32
34
54
GRAPHICS PROCESSING CIRCUIT
101
FRONT END CIRCUITRY
35
102
36
37
40
38
SCAN CONVERTER
41
SCAN CONVERTER
V_{CC}
55
60
61
39
BACK END CIRCUITRY A
42
BACK END CIRCUITRY B
43
44
52
46
MEMORY CONTROLLER
49
50
70
Switch
71
48
GRAPHICS MEMORY
DISPLAY
51

FIG. 2

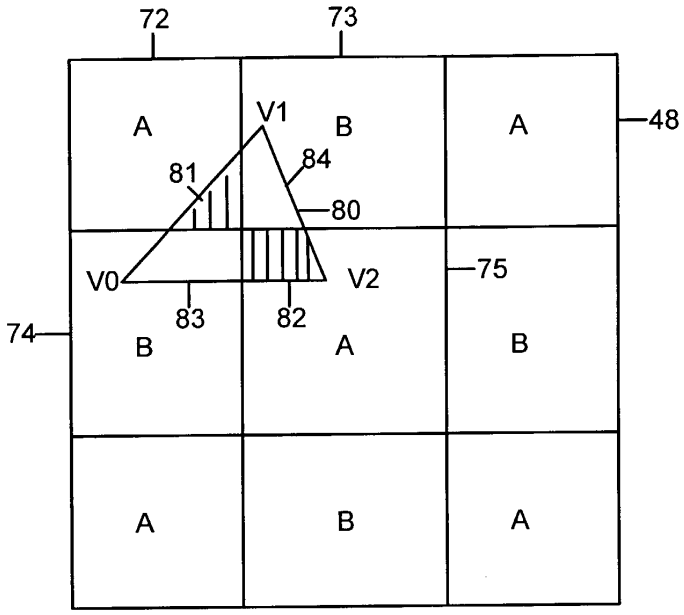

72
73
A
V1
B
A
48
81
84
80
V0
V2
75
83
82
74
B
A
B
A
B
A

FIG. 3

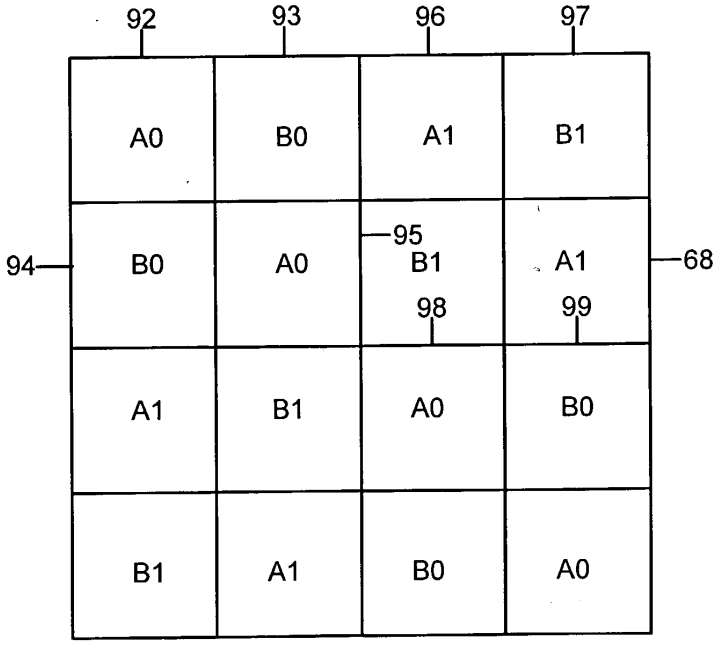

92
93
96
97
A0
B0
A1
B1
95
94
B0
A0
B1
A1
68
98
99
A1
B1
A0
B0
B1
A1
B0
A0

FIG. 4

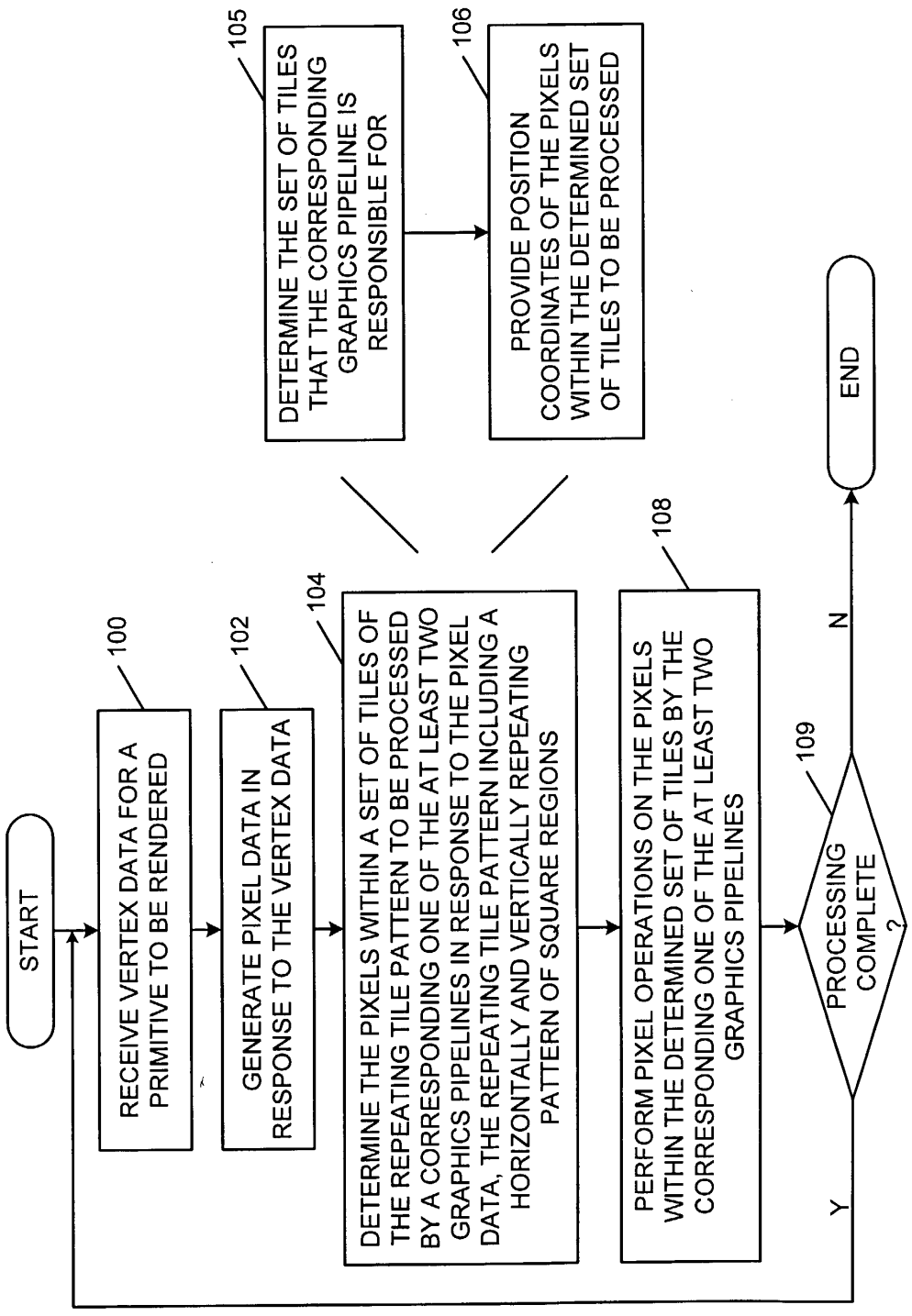

START
RECEIVE VERTEX DATA FOR A PRIMITIVE TO BE RENDERED
100
GENERATE PIXEL DATA IN RESPONSE TO THE VERTEX DATA
102
DETERMINE THE PIXELS WITHIN A SET OF TILES OF THE REPEATING TILE PATTERN TO BE PROCESSED BY A CORRESPONDING ONE OF THE AT LEAST TWO GRAPHICS PIPELINES IN RESPONSE TO THE PIXEL DATA, THE REPEATING TILE PATTERN INCLUDING A HORIZONTALLY AND VERTICALLY REPEATING PATTERN OF SQUARE REGIONS
104
DETERMINE THE SET OF TILES THAT THE CORRESPONDING GRAPHICS PIPELINE IS RESPONSIBLE FOR
105
PROVIDE POSITION COORDINATES OF THE PIXELS WITHIN THE DETERMINED SET OF TILES TO BE PROCESSED
106
PERFORM PIXEL OPERATIONS ON THE PIXELS WITHIN THE DETERMINED SET OF TILES BY THE CORRESPONDING ONE OF THE AT LEAST TWO GRAPHICS PIPELINES
108
PROCESSING COMPLETE ?
109
Y
N
END

FIG. 6

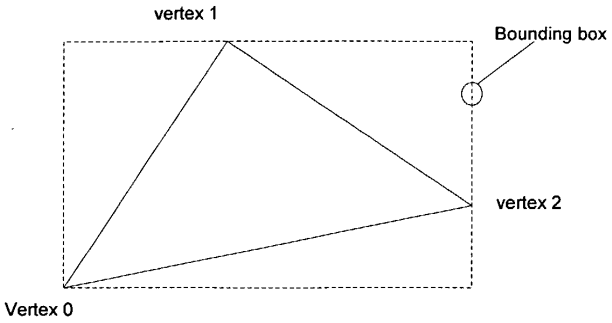

vertex 1
Bounding box
vertex 2
Vertex 0

FIG. 7

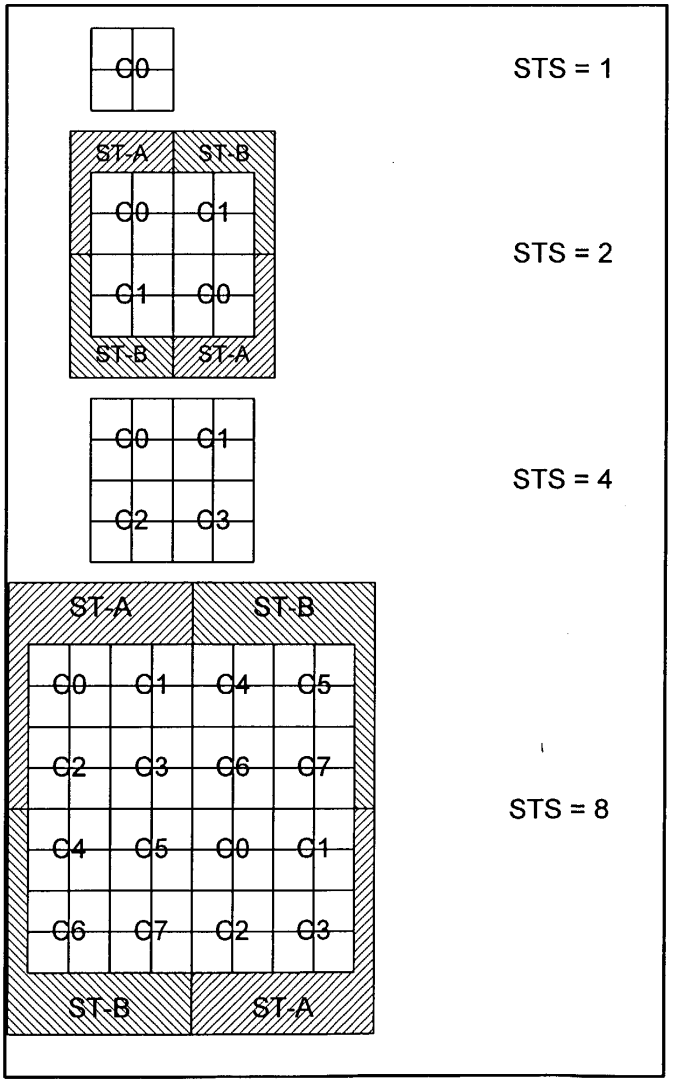

C0
STS = 1
ST-A
ST-B
C0
C1
C1
C0
ST-B
ST-A
STS = 2
C0
C1
C2
C3
STS = 4
ST-A
ST-B
C0
C1
C4
C5
C2
C3
C6
C7
C4
C5
C0
C1
C6
C7
C2
C3
ST-B
ST-A
STS = 8

FIG. 8

020053

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☒ Declaration Submitted with Initial Filing, OR
☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)

Attorney Docket Number 00100.02.0053
First Named Inventor: Mark M. Leather
COMPLETE IF KNOWN
Application Number:
Filing Date:
Group Art Unit: _____
Examiner Name: _____

As a below named inventor, I hereby declare that:
My residence, post office address, and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

the specification of which:
☒ is attached hereto.
☐ was filed on _____ as _____ Application Number _____ or as PCT International Application Number _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Data (MM/DD/YYYY)
60/429,641	11/27/2002

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

020053

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transaction all business in the Patent and Trademark Office connected therewith:

Name	Registration Number	Name	Registration Number
Christopher J. Reckamp	34,414	Angelo J. Bufalino	29,622
Joseph P. Krause	32,578	Robert Beiser	28,687
Michael J. Turgeon	39,404	Brent A. Boyd	51,020
Timothy J. Bechen	48,126	Themi Anagnos	47,388

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.\

Direct all correspondence to:

Vedder, Price, Kaufman & Kammholz
222 N. LaSalle Street, Suite 2600
Chicago, Illinois 60601
Telephone: 312-609-7500
Facsimile: 312-609-5005

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

☐ A petition has been filed for this unsigned inventor

Name of Sole or First Inventor:

Given Name (first and middle [if any])			Family Name or Surname	
Mark M.			Leather	
Inventor's Signature	Mark M Leather		**Date** 5/23/03	
Residence	City: Saratoga	State: California	Country: USA	Citizenship: United Kingdom
Post Office Address	12187 Woodside Drive			
City: Saratoga	State: California		ZIP: 95070	Country: USA

☐ A petition has been filed for this unsigned inventor

Name of Additional Joint Inventor:

Given Name (first and middle [if any])			Family Name or Surname	
Eric			Demers	
Inventor's Signature	Eric Demers		**Date** 6/2/03	
Residence	City: Palo Alto	State: California	Country: USA	Citizenship: Canadian
Post Office Address	901 Sycamore Drive			
City: Palo Alto	State: California		ZIP: 94303	Country: USA

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/16/2003 DTESSEM1 00000014 500441 10459797

01 FC:1001 750.00 CH
02 FC:1202 72.00 CH

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/69033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY

SERIAL NO.

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1ST AMENDMENT		AFTER 2ND AMENDMENT	
	IND	DEP	IND	DEP	IND	DEP
1	1					
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20	1					
21						
22						
23						
24	1					
25						
26						
27						
28						
29						
30						
31						
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						
47						
48						
49						
50						
TOTAL IND.	3					
TOTAL DEP.	21					
TOTAL CLAIMS	24					

	IND	DEP	IND	DEP	IND	DEP
51						
52						
53						
54						
55						
56						
57						
58						
59						
60						
61						
62						
63						
64						
65						
66						
67						
68						
69						
70						
71						
72						
73						
74						
75						
76						
77						
78						
79						
80						
81						
82						
83						
84						
85						
86						
87						
88						
89						
90						
91						
92						
93						
94						
95						
96						
97						
98						
99						
100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

PTO-2202 (Replication only) (1/03)

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

6/12/03

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 24	=
Independent	* 3	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	257	345/506.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 13:46
S2	50	345/506.ccls. and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:58
S3	41	345/506.ccls. and tile and frame adj buffer	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S4	41	345/506.ccls. and tile and frame adj buffer and pixel	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S5	36	345/506.ccls. and tile and frame adj buffer and pixel and vertex	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S6	33	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S7	33	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3	US-PGPUB; USPAT	OR	OFF	2004/12/07 14:59
S8	7	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3 and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:03
S9	24	345/506.ccls. and multiple adj pipelines	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:21
S10	9	345/506.ccls. and multiple adj pipelines and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:01
S12	7	345/506.ccls. and tile and frame adj buffer and pixel and vertex and primitive and render$3 and scan adj converter and "16"	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:34
S13	13	345/506.ccls. and multiple adj pipelines and chip$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:08
S14	5	345/506.ccls. and multiple adj pipelines and memory adj controller	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:08
S15	15	345/506.ccls. and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:11
S16	14	345/506.ccls. and scan adj converter and coordinates	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:11
S17	3	345/506.ccls. and multiple adj pipelines and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:21
S18	127	345/506.ccls. and polygon	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:24
S20	40	345/506.ccls. and polygon and bounding adj box	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:24
S21	25	345/506.ccls. and polygon and bounding adj box and tile	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26

S22	21	345/506.ccls. and polygon and bounding adj box and tile and overlap	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S23	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S24	4	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and scan adj converter	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:26
S25	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S26	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S27	19	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:27
S28	16	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive and frame adj buffer	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:21
S29	3	345/506.ccls. and polygon and bounding adj box and tile and overlap and chip and pixel and vertex and primitive and frame adj buffer and multiple adj pipelines	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:28
S30	1	345/506.ccls. and repeating adj tile$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S31	35	repeating adj tile$1	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S32	10	repeating adj tile$1 and graphics	US-PGPUB; USPAT	OR	OFF	2004/12/07 15:31
S33	1	("6753878").PN.	USPAT	OR	OFF	2004/12/07 15:34
S34	11	345/506.ccls. and front adj end and back adj end	US-PGPUB; USPAT	OR	OFF	2004/12/08 13:46
S36	222	345/530.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:24
S37	245	345/505.ccls.	US-PGPUB; USPAT	OR	OFF	2004/12/08 15:28

85

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

7590 12/14/2004

Christopher J. Reckamp
Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☒ Claim(s) 9 and 24 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 objected to because of the following informalities: In line 6 on page 17, the claim states "two graphics pipeline" where it should state "two graphics pipelines". Appropriate correction is required.

2. Claim 24 objected to because of the following informalities: In lines 14-15 on page 20, the claim states "set of tiles *or* the repeating tile pattern" where it should state "set of tiles *of* the repeating tile pattern". In line 18 on page 20, the claim states "*receive* transmit and receive" where it should state "transmit and receive". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9, 12, and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "the first pipeline" and "the second pipeline". There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the pixel data". There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the front end circuitry" and "the back end circuitry". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-8, 10-18, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A).

8. With regard to Claim 1, Migdal describes a graphics processing circuit, comprising a graphics pipeline (Col. 1, line 66-Col. 2, line 17) operative to process data in a corresponding set of tiles, the graphics pipeline operative to process data in a dedicated tile (Col. 8, lines 20-23).

However, Migdal does not teach that there are at least two graphics pipelines and each graphics pipeline processes data in a dedicated tile. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33) and each graphics pipeline processes data in a dedicated part of the image (PI, Col. 6, lines 1-6).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Migdal so that there are at least two graphics pipelines and each graphics pipeline processes data in a dedicated tile as suggested by Heirich. Heirich suggests that it is advantageous to use multiple graphics pipelines because each pipeline can work on a different process or part of the image without waiting for the other processes to finish first (Col. 2, lines 24-39), so using multiple graphics pipelines speeds up the processing operation.

However, Migdal and Heirich do not teach a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 3, line 67-Col. 4, line 4; Col. 4, lines 31-32; Col. 5, lines 17-20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal and Heirich to include a repeating tile pattern, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions

as suggested by Duffy because Duffy suggests that rather than generating an entire simulated halftone screen for each process color of an image, which takes up substantial additional computing power, a set of rectangular repeating patterns can be stored and retrieved for use in filling incremental regions of the image (Col. 3, line 63-Col. 4, line 4).

9. With regard to Claim 2, Migdal describes that the square regions comprise a two dimensional partitioning of memory (Col. 7, lines 63-65).

10. With regard to Claim 3, Migdal describes that the memory is a frame buffer (Col. 5, lines 63-67).

11. With regard to Claim 4, Migdal describes that the graphics pipeline further includes front end circuitry (105, Figure 1) operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19), and back end circuitry (108), coupled to the front end circuitry, operative to receive and process a portion of the pixel data (Col. 4, lines 46-51).

However Migdal does not teach that there are two graphics pipelines operative to receive and process a portion of the pixel data. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33) operative to receive and process a portión of the pixel data (PI, Col. 6, lines 1-6), as discussed in the rejection for Claim 1.

12. With regard to Claim 5, Migdal describes that the graphics pipeline further includes a scan converter (602, Figure 6), coupled to the back end circuitry (603-615), operative to determine the portion of the pixel data to be processed by the back end circuitry (Col. 8, lines 7-19).

However Migdal does not teach that there are two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

13. With regard to Claim 6, Migdal describes that each tile of the set of tiles further comprises a 16x16 pixel array (Col. 7, lines 63-65).

14. With regard to Claim 7, Migdal does not teach that the at least two graphics pipelines separately receive the pixel data from the front end circuitry. However, Heirich describes that the at least two graphics pipelines (22, 24, Figure 1) separately receive the pixel data (PI) from the front end circuitry (22) (Col. 6, lines 1-6).

It would have been obvious at the time of invention by applicant to modify the device of Migdal so that the at least two graphics pipelines separately receive the pixel data from the front end circuitry as suggested by Heirich. Since Heirich describes using multiple graphics pipelines, each graphics pipeline must inherently separately receive the pixel data from the front end circuitry. The advantages of using multiple graphics pipelines were discussed in the rejection for Claim 1.

15. With regard to Claim 8, Migdal does not teach that the at least two graphics pipelines are on multiple chips. However, Heirich describes multiple graphics pipelines and that each graphics pipeline can be on a separate workstation (Figure 4; Col. 16, lines 53-59). Since the graphics pipelines are on separate workstations, the graphics pipelines must inherently be on multiple chips.

It would have been obvious at the time of invention by applicant to modify the device of Migdal so that the at least two graphics pipelines are on multiple chips as suggested by Heirich because Heirich suggests the advantage of being able to put the different chips on different workstations. In this configuration, off-the-shelf workstations and graphics accelerator cards can be used for image generation, which greatly reduces the cost of the system. The marginal costs of the image generation process might be reduced even further if the workstations and graphics accelerators are used for other purposes (Col. 16, lines 41-46).

16. With regard to Claim 10, Migdal does not teach that a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1), and each graphics pipeline processes only a part of an image (PI; Col. 6, lines 1-6). Therefore, Heirich describes that a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

17. With regard to Claim 11, Migdal describes that the graphics pipeline further includes a scan converter (602, Figure 6), coupled to the front end circuitry (105, Figure 1) and the back end circuitry (603-615, Figure 6), operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry (Col. 8, lines 17-19). The scan converter provides position coordinates to the texture request generator (603). From these position coordinates, the texture request generator knows which of the set of tiles is to be processed by the back end circuitry and generates the required tile addresses for theses tiles (Col. 8, lines 17-23). Therefore, the scan converter must inherently include a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

However Migdal does not teach that there are two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

18. With regard to Claim 12, Claim 12 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

19. With regard to Claim 13, Claim 13 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

20. With regard to Claim 14, Migdal describes a graphics pipeline (Col. 1, line 66-Col. 2, line 17) including front end circuitry (105, Figure 1) operative to receive vertex data and generate

pixel data corresponding to a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19), and back end circuitry (108), coupled to the front end circuitry, operative to receive and process the pixel data in a set of tiles in the repeating tile pattern (Col. 4, lines 46-51).

However, Migdal does not teach a third graphics pipeline and a fourth graphics pipeline. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1. Heirich also describes that each pipeline processes the pixel data only in one set of tiles in the repeating tile pattern, as discussed in the rejection for Claim 10.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

21. With regard to Claim 15, Claim 15 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

22. With regard to Claim 16, Claim 16 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

23. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

24. With regard to Claim 18, Migdal does not teach a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Heirich describes a bridge (20, Figure 1) operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines (22) (Col. 5, lines 45-50).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Migdal to include a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Heirich because Heirich suggests the advantage of being able to distribute all of the vertex data at once (Col. 5, lines 53-58). The advantages of having multiple graphics pipelines were discussed in the rejection for Claim 1.

25. With regard to Claim 20, Migdal describes a graphics processing method, comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data (Col. 4, lines 46-51); determining the pixels within a set of tiles to be processed by a the graphics pipeline in response to the pixel data; and performing pixel operations on the pixels within the determined set of tiles by the graphics pipeline (Col. 8, lines 6-23).

However, Migdal does not teach a repeating tile pattern including a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern including a horizontally and vertically repeating pattern of square regions (Col. 4, lines 26-53; Col. 5, lines 17-20) as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

26. With regard to Claim 21, Migdal does not teach that determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1), and each graphics pipeline processes only a part of an image (PI, Col. 6, lines 1-6), as discussed in the rejection for Claim 10. Therefore, Heirich inherently teaches determining the pixels within a set of tiles to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

However, Migdal and Heirich do not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

27. With regard to Claim 22, Migdal describes determining the pixels within a set of tiles to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the graphics pipeline (Col. 8, lines 17-23).

However, Migdal does not teach a repeating tile pattern. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach two graphics pipelines. However, Heirich describes multiple graphics pipelines (22, 24, Figure 1; Col. 5, lines 31-33), as discussed in the rejection for Claim 1.

28. With regard to Claim 23, Migdal describes transmitting the processed pixels to memory (109, Figure 1; Col. 8, line 48-Col. 9, line 3).

29. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A), further in view of Wang (US006184906B1).

Migdal, Heirich, and Duffy are relied upon for the teachings as discussed above relative to Claim 1.

However, Migdal, Heirich, and Duffy do not teach a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory. However, Wang describes a memory controller (28, Figure 2) coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory (60) (Col. 3, lines 55-58).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal, Heirich, and Duffy to include a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and the second pipeline and a memory as suggested by Wang because Wang

suggests the advantage of improving the speed of operation and allowing for a single memory clock cycle read/write operation (Col. 1, lines 51-55).

30. Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Heirich (US006753878B1), further in view of Duffy (US005179640A), further in view of Kent (US 20030164830A1).

Migdal, Heirich, and Duffy are relied upon for the teachings as discussed above relative to Claim 17.

However, Migdal, Heirich, and Duffy do not teach that the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip [0010, 0012] and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. However, Kent describes the data includes a polygon [0006] and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one [0129, 0144].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal, Heirich, and Duffy so that the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and

wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one as suggested by Kent because Kent suggests the advantage of being able to determine if a polygon is within the super tiles associated with a separate chip [0129, 0144]. This is needed in order for each separate chip to only process the pixel data in one set of tiles, as discussed in the rejections for Claims 8 and 10.

31. Claim 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Migdal (US006762763B1) in view of Duffy (US005179640A), further in view of Morgan (US006714203B1), further in view of Wang (US006184906B1).

Migdal describes a graphics processing circuit, comprising front end circuitry (105, Figure 1) operative to generate pixel data in response to primitive data for a primitive to be rendered (Col. 4, lines 46-51; Col. 5, lines 39-41; Col. 8, lines 17-19); first back end circuitry (108), coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates (Col. 8, lines 20-23); a first scan converter (602, Figure 6), coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles are to be processed by the first back end circuitry, and operative to provide the position coordinates of the first back end circuitry in response to the pixel data (Col. 8, lines 7-23).

However, Migdal does not teach a repeating tile pattern including a horizontally and vertically repeating pattern of square regions. However, Duffy describes a repeating tile pattern (Col. 4, lines 26-53; Col. 5, lines 17-20), as discussed in the rejection for Claim 1.

However, Migdal and Duffy do not teach a second back end circuitry. However, Morgan describes a front end circuitry (202, Figure 2) coupled to multiple back end circuitries (208, 210) (Col. 3, lines 41-42).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Migdal and Duffy to include a second back end circuitry as suggested by Morgan because Morgan suggests that it is simpler to have one front-end circuitry as a data communications interface for the image generation system (Col. 3, lines 32-34) and couple the one front-end circuitry to multiple back end circuitries. The multiple back-end circuitries are for multiple graphics pipelines. The advantages of having multiple graphics pipelines were discussed in the rejection for Claim 1.

However, Migdal, Duffy, and Morgan do not teach a memory controller, coupled to the first and second back end circuitry, operative to transmit and receive the processed pixel data. However, Wang describes a memory controller (28, Figure 2), coupled to multiple pipelines or the first and second back end circuitry, operative to transmit and receive the processed pixel data (Col. 3, lines 55-58), as discussed in the rejection for Claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2676	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,762,763 B1	07-2004	Migdal et al.	345/506
	B	US-6,753,878 B1	06-2004	Heirich et al.	345/629
	C	US-5,179,640 A	01-1993	Duffy, Christopher J.	345/596
	D	US-6,184,906 B1	02-2001	Wang et al.	345/532
	E	US-2003/0164830 A1	09-2003	Kent, Osman	345/505
	F	US-6,714,203 B1	03-2004	Morgan et al.	345/506
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application No.	Applicant(s)	
10/459,797	LEATHER ET AL.	
Examiner	**Art Unit**	
Joni Hsu	2676	

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	12/9/04
	1	√
	2	|
	3	|
	4	|
	5	|
	6	|
	7	|
	8	|
	9	|
	10	|
	11	|
	12	|
	13	|
	14	|
	15	|
	16	|
	17	|
	18	|
	19	|
	20	|
	21	|
	22	|
	23	|
	24	|
	25	
	26	
	27	
	28	
	29	
	30	
	31	
	32	
	33	
	34	
	35	
	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

Claim		Date
Final	Original	
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

Claim		Date
Final	Original	
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	
	114	
	115	
	116	
	117	
	118	
	119	
	120	
	121	
	122	
	123	
	124	
	125	
	126	
	127	
	128	
	129	
	130	
	131	
	132	
	133	
	134	
	135	
	136	
	137	
	138	
	139	
	140	
	141	
	142	
	143	
	144	
	145	
	146	
	147	
	148	
	149	
	150	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIBDATASHEET

Bib Data Sheet

CONFIRMATION NO. 4148

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,797	06/12/2003 RULE	345	2676	00100.02.0053

APPLICANTS

Mark M. Leather, Saratoga, CA;

Eric Demers, Palo Alto, CA;

** CONTINUING DATA **********

This appln claims benefit of 60/429,641 11/27/2002

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/07/2003

Foreign Priority claimed	35 USC 119 (a-d) conditions met	Verified and Acknowledged	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ yes ☑ no	☐ yes ☑ no ☐ Met after Allowance	Examiner's Signature / Initials	CA	5	24	3

ADDRESS
Christopher J. Reckamp
Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago , IL
60601

TITLE
Dividing work among multiple graphics pipelines using a super-tiling technique

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue)

822		☐ Other _____ ☐ Credit

Search Notes	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505	12/7/2004	

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached search history.	12/7/2004	

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 300.00

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Examiner Name	Joni Hsu
Art Unit	2676
Attorney Docket No.	00100.02.0053

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0441 Deposit Account Name: ATI International SRL

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
26 - 24 or HP =	2	x 50	= 100

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
4 - 3 or HP =	1	x 200	= 200

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
- 100 =	/ 50 =	(round up to a whole number)	x	=

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge):	

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 34,414	Telephone 312-609-7599
Name (Print/Type)	Christopher J. Reckamp		Date March 14, 2005

2676 TW

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2676
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [x] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  -return postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Vedder, Price, Kaufman & Kammholz, P.C.		
Signature			
Printed name	Christopher J. Reckamp		
Date	March 14, 2005	Reg. No.	34,414

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Christine A. Wright	Date	March 14, 2005

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Group: 2676
Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of First Class Mailing
I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

3-14-05
Date

Christine A. Wright

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed December 14, 2004, Applicants submit the following Amendment and Response.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 10 of this paper.

Amendments to the Specification:

Please replace paragraph [0046] with the following amended paragraph:

[0046] The bounding boxes' four corners are mapped to the tile pattern, simply by discarding the lower bits of X & Y. The four corners map to the same or different tiles. If they all map to the same tile, then only the pipeline that is associated with that tile receives the polygon. If it maps to only tiles that are associated with only one pipeline, then again only that pipeline receives the polygon. If it maps to tiles that are associated with multiple pipelines, then the entire polygon is sent to all pipelines. In [[our]]one implementation, ~~we broadcast~~ the polygon is broadcast to all pipelines, masking the pipelines that should not receive it. Consequently, polygons can be sent to only one pipe or up to all the pipes, depending on the coverage of the tiles by the polygon.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (original) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. (currently amended) The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics ~~pipeline~~pipelines, operative to transfer pixel data between each of [[the]]a first pipeline and [[the]]a second pipeline and a memory.

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first

set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (currently amended) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the [[pixel]] data only in a second set of tiles in the repeating tile pattern.

13. (currently amended) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to [[the]] front end circuitry and [[the]] back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip

and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (original) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (original) The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

24. (currently amended) A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles [[or]]of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry. operative to receive transmit and receive the processed pixel data.

25. (new) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process

data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions.

26. (new) The graphics processing circuit of claim 25 wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 9 and 24 are objected to due to typographical errors. These errors have been corrected.

Claims 9, 12 and 13 stand rejected under 35 U.S.C. §112, 2nd paragraph, as being indefinite due to antecedent discrepancies caused by typographical errors. Applicants have corrected typographical errors and as such, this rejection is respectfully requested to be withdrawn.

Claims 1-8, 10-18, 20-23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy. Applicants respectfully submit that the Migdal reference actually teaches away from a multi-graphics pipeline structure and as such, cannot render the claimed invention obvious. For example, the Migdal reference is directed to a computer system having a distributed texture memory architecture to overcome problems associated with parallel pipelined architectures. As specifically stated for example in column 2, lines 26-27, Migdal states that there are several disadvantages with using a parallel pipelined approach especially in the case when several pipelines perform parallel processing together in order to generate a single frames worth of data. (See specifically, column 2, lines 31-33). Since Applicants claim a multigraphics pipeline structure that processes data in sets of tiles in a frame, Migdal teaches away from the claimed circuit. Moreover, the office action also admits that Migdal does not teach that there are multiple graphics pipelines and wherein each graphics pipeline processes data in a dedicated tile. As noted, Migdal actually teaches away from Applicants' claimed invention. (See for example, columns 2 and 3 of Migdal). Since the Migdal reference teaches away from Applicants' claimed invention, the claims are in condition for

allowance and that the combination of the cited references with Migdal does not render the claims obvious.

In addition, the Duffy reference has been alleged to be properly combinable with Migdal and Heirich and is allegedly cited as describing a repeating tile pattern where the repeating tile patterns include a horizontally and vertically repeating pattern of square regions (office action citing column 3, lines 67 through column 4, line 4; column 4, lines 31-32; column 5, lines 17-20). However, Applicants respectfully submit that the cited portions of Duffy actually teach a completely different pattern than the repeating tile patterns that are processed by two graphics pipelines wherein the repeating tile pattern includes horizontally and vertically repeating patterns of regions as claimed. For example, the "repeating patterns" cited in the portions referenced in the office action of Duffy, are actually pixel "fill" patterns used for dithering. (See for example, column 3, lines 52-66). As such, the "repeating patterns" of tiles described in Duffy are actually patterned wallpaper or filled patterns that are when displayed allow a person's eye to blend neighboring pixels of differing visual patterns.

In contrast, the "tiles" and "repeating tile pattern" of the claimed invention deal with processing tiles that are used by graphics pipelines to process primitive data such as polygons to generate pixels that are ultimately displayed. Accordingly, although some of the wording is similar, the Duffy reference actually refers to a dithering halftone visual pattern of pixels whereas Applicants' claim is directed to tile processing using graphics pipelines. As such, upon further investigation of Duffy, it appears that the Duffy reference may have been misapprehended and actually teaches a different system from that described by Applicants and accordingly, the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter and are also allowable for at least depending upon allowable base claims.

As to claim 20, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and as such, this claim is also allowable.

Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy and in view of Wang. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Heirich further in view of Duffy and in view of Kent. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also in condition for allowance. In addition, this claim adds additional novel and non-obvious subject matter and is also therefore allowable.

Claim 24 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Migdal in view of Duffy further in view of Morgan and in view of Wang. Applicants respectfully reassert the relevant remarks made above with respect to the Migdal and Duffy reference and as such, this claim is also believed to be in condition for allowance.

New claims 25 and 26 are also allowable for similar reasons stated above as the references in combination do not teach or suggest the graphic pipelines and non-square tile processing in horizontally and vertically repeating patterns as claimed.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 3-14-05

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	822

6/7/05

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 24	= 2
Independent	* 4	Minus	*** 3	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18= 50	100
X42=		OR	X84= 200	200
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	300

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/459,797		2676	26M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 29153 on 07/20/2005

- Correspondence Address

The address of record for Customer Number 29153 is:
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO,IL 60601

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
10/459,797		2676	26M1

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 29153 on 07/22/2005

- Correspondence Address

The address of record for Customer Number 29153 is:
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO,IL 60601

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	307	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L2	256	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L3	272	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L4	37	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L5	81	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L6	448	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L7	68	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L8	712	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05

L9	335	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L10	557	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:05
L16	1179	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:08
L17	933	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:08
L18	100	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:09
L19	73	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:10
L24	212	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:12
L27	277	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:14

L28	72	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:14
L29	68	(multiple plurality) near2 pipelin$3 and scan adj conver$5 and pixel$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:15
L30	79	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:15
L32	34	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:16

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 08/01/2005

ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18, 20-26* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In light of Applicant's amendments to Claim 9, the objection to this claim has been withdrawn.

2. In light of Applicant's amendments to Claims 9, 12, and 13, the rejections of these claims under 35 U.S.C. 112, 2nd paragraph have been withdrawn.

3. Applicant's arguments, see page 12, filed March 14, 2005, with respect to Claim 19 have been fully considered and are persuasive. The rejection under 35 U.S.C. 103(a) of Claim 19 has been withdrawn.

4. With regard to Claim 19, Applicant argues that this claim adds additional novel and non-obvious subject matter and is also therefore allowable (page 12).

In reply, the Examiner agrees. The rejection under 35 U.S.C. 103(a) of Claim 19 has been withdrawn.

5. Applicant's arguments with respect to claims 1-18 and 20-24 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments, see pages 10-12, filed March 14, 2005, with respect to the rejection(s) of claim(s) 1-18 and 20-24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Alcorn (US005745118A).

7. With regard to Claim 1, Applicant argues that the Migdal reference (US006762763B1) actually teaches away from a multi-graphics pipeline structure and as such, cannot render the claimed invention obvious (pages 10-11). Applicant also argues that the "repeating patterns" of tiles described in Duffy (US005179640A) are actually patterned wallpaper or filled patterns that are when displayed allow a person's eye to blend neighboring pixels of differing visual patterns. In contrast, the "tiles" and "repeating tile pattern" of the claimed invention deal with processing tiles that are used by graphics pipelines to process primitive data such as polygons to generate pixels that are ultimately displayed (page 11).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Alcorn. Alcorn describes a graphics processing circuit (Col. 3, lines 58-60), comprising at least two graphics pipelines (*front end board 10, texture mapping board 12 and frame buffer board 14 each is pipelined and operates on multiple primitives simultaneously*, Col. 6, lines 33-35; *front end board 10 includes three 3-D geometry accelerator chips 32A, 32B and 32C, a 2-D geometry accelerator chip 34*, Col. 6, lines 40-43) operative to process data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the

texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). According to the disclosure of this application, a repeating tile pattern means that the pixel data is repeated [0022], and the pixel data includes appearance attributes such as texture [0003]. Therefore, Alcorn describes that the tiles have a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile (*tiler processes data within the texture map*, Col. 11, lines 8-31; *for example, texture is defined have S,T coordinates ranging from [0, 0] through (10, 10)*, Col. 11, lines 37-39). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6.

8. With regard to Claims 2-18 and 20-24, Applicant argues that these claims should be allowed for the same reasons given above (pages 11-12).

In reply, the Examiner disagrees for the same reasons given above.

9. With regard to Claims 25 and 26, Applicant argues that the references in combination do not teach or suggest the graphic pipelines and non-square tile processing in horizontally and vertically repeating patterns as claimed (page 12).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Alcorn, as discussed above. According to the disclosure of this application, the NxM format for the tile sizes are 8x8, 16x16, or 32x32 [0043], so the invention deals with square tile processing. Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating

pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6, and the horizontally and vertically repeating pattern of regions include NxM (4x4) number of texels (Col. 15, lines 44-57). In one example, Alcorn describes that one pixel maps to four texels (Col. 15, lines 55-57). Since the pixels map to the texels, the repeating pattern of regions of the pixels would still be in NxM format.

Claim Objections

10. Claim 24 is objected to because of the following informalities: Claim 24 recites "a memory controller, coupled to the first and second back end circuitry, operative to *receive* transmit and receive the processed pixel data" where it should recite "a memory controller, coupled to the first and second back end circuitry, operative to transmit and receive the processed pixel data." Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-4, 6-8, 9, 10, 12, 14, 17, 18, 20-23, 25, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Alcorn (US005745118A).

13. With regard to Claim 1, Alcorn describes a graphics processing circuit (Col. 3, lines 58-60), comprising at least two graphics pipelines (*front end board 10, texture mapping board 12 and frame buffer board 14 each is pipelined and operates on multiple primitives simultaneously*, Col. 6, lines 33-35; *front end board 10 includes three 3-D geometry accelerator chips 32A, 32B and 32C, a 2-D geometry accelerator chip 34*, Col. 6, lines 40-43) operative to process data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). According to the disclosure of this application, a repeating tile pattern means that the pixel data is repeated [0022], and the pixel data includes appearance attributes such as texture [0003]. Therefore, Alcorn describes that the tiles have a repeating tile pattern, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile (*tiler processes data within the texture map*, Col. 11, lines 8-31; *for example, texture is defined have S,T coordinates ranging from [0, 0] through (10, 10)*, Col. 11, lines 37-39). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6.

14. With regard to Claim 2, Alcorn describes that the square regions comprise a two dimensional partitioning of memory (*blocks of texture data are organized to take advantage of*

the four interleave implementation of the cache memory, Col. 15, lines 43-57, *S,T texture map coordinates*, Col. 10, lines 1-9).

15. With regard to Claim 3, Alcorn describes that the texture map partitions are provided to the frame buffer (Col. 14, lines 51-63), and therefore the memory is a frame buffer.

16. With regard to Claim 4, Alcorn describes that each of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) further includes front end circuitry (32A, 32B, 32C, Figure 2) are operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered (*distributes 3-D primitive data evenly among the 3-D geometry accelerator chips*, Col. 6, lines 43-47; *each 3-D geometry accelerator chip processes primitive data*, Col. 6, lines 56-62; *rendering hardware interpolates the primitive data to compute the display screen pixels that are turned on to represent each primitive*, Col. 1, lines 31-33; *vertex data*, Col. 7, lines 22-33), and back end circuitry (12), coupled to the front end circuitry (Col. 7, lines 5-10), operative to receive and process a portion of the pixel data (Col. 12, lines 13-20).

17. With regard to Claim 6, Alcorn describes that each texture map can comprise of texel arrays of either 4x4 (Col. 2, lines 38-41), 16x16 or 64x64 texels (Col. 2, lines 65-66). The pixel maps are in one-to-one correspondence with a single texel in the texture map (Col. 2, lines 62-64). The tiler partitions the memory into texture maps (Col. 11, lines 8-31), so each tile contains a texture map. Therefore, Alcorn discloses that each tile of the set of tiles further comprises a 16x16 pixel array.

18. With regard to Claim 7, Alcorn describes that the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) separately receive the pixel data from the front end circuitry (32A, 32B, 32C, Figure 2) (*distributes 3-D primitive data evenly among the 3-D geometry accelerator chips*, Col. 6, lines 43-47; *each 3-D geometry accelerator chip processes primitive data*, Col. 6, lines 56-62; *rendering hardware interpolates the primitive data to compute the display screen pixels that are turned on to represent each primitive*, Col. 1, lines 31-33; *texture mapping board receives data from the separate 3-D geometry accelerator chips*, Col. 7, lines 5-10).

19. With regard to Claim 8, Alcorn describes that the at least two graphics pipelines are on multiple chips (Col. 6, lines 33-35, *3-D geometry accelerator chips*, Col. 6, lines 40-43).

20. With regard to Claim 9, Alcorn describes a memory controller (50, Figure 2) coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory (51) (Col. 6, lines 33-35, 40-43; Col. 8, lines 27-40).

21. With regard to Claim 10, Alcorn describes processing pixel data in a corresponding set of tiles (tiler, Col. 11, lines 8-31). Alcorn describes mapping a texture to an object in a repeating fashion, such that the texture is mapped to multiple portions of the object (Col. 11, lines 35-37). Alcorn describes having a wrapping feature for coordinates falling outside the boundary of the texture map, and pixels having S,T coordinates [10, 10] through (20, 20) would respectively map

to the texels at S,T coordinates [0, 0] through (10, 10) (Col. 11, lines 46-50). Therefore, since the tiles are repeated, only a first set of tiles are processed, and then those tiles are repeated. Therefore, Alcorn discloses that a first of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) processes the pixel data only in a first set of tiles in the repeating tile pattern.

22. With regard to Claim 12, Claim 12 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

23. With regard to Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Alcorn gives an example of three graphics pipelines (Col. 6, lines 33-35, 40-43), however, Alcorn describes that the number of graphics pipeline can be modified (Col. 5, line 65-Col. 6, line 3). Therefore, Claim 14 is rejected under the same rationale as Claims 4 and 10.

24. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

25. With regard to Claim 18, Alcorn describes a bridge (30, Figure 2) operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines (Col. 6, lines 32-35, 40-47; Col. 7, lines 28-33; Col. 5, line 65-Col. 6, line 3).

26. With regard to Claim 20, Alcorn describes a graphics processing method (Col. 3, lines 58-60), comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data (Col. 7, lines 21-33); determining the pixels within a set of tiles (tiler, Col. 11, lines 8-31) of a repeating tile pattern to be processed by a corresponding one of at least two graphics pipelines (Col. 6, lines 33-35, 40-43) in response to the pixel data (Col. 11, lines 35-50). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6. Alcorn describes performing pixel operations on the pixels within the determined set of tiles (Col. 12, lines 13-20) by the corresponding one of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43).

27. With regard to Claim 21, Alcorn describes that determining the pixels within a set of tiles of the repeating tile pattern to be processed, as discussed in the rejection for Claim 20, and the set of tiles to be processed is inherently the set of tiles that the corresponding graphics pipeline is responsible for.

28. With regard to Claim 22, Alcorn describes that determining the pixels within a set of tiles of the repeating tile pattern (Col. 11, lines 35-50) to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines (Col. 10, lines 1-8; *texel data output from the parameter interpolator circuit 64 is provided to the tiler 72, which determines the address of the four texels...checks to determine whether each is within the boundary of the*

texture...texel data includes the interpolated S, T coordinates as well as the map number, Col. 11, lines 8-31; Col. 6, lines 33-35, 40-43).

29. With regard to Claim 23, Alcorn describes transmitting the processed pixels to memory (Col. 6, lines 14-20).

30. With regard to Claim 25, Claim 25 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

31. With regard to Claim 26, Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6, and the horizontally and vertically repeating pattern of regions include NxM (4x4) number of texels (Col. 15, lines 44-57). According to the disclosure of this application, the NxM format for the tile sizes are 8x8, 16x16, or 32x32 [0043], and therefore 4x4 fits this format. In one example, Alcorn describes that one pixel maps to four texels (Col. 15, lines 55-57). Since the pixels map to the texels, the repeating pattern of regions of the pixels would still be in NxM format.

32. Thus, it reasonably appears that Alcorn describes or discloses every element of Claims 1-4, 6-8, 9, 10, 12, 14, 17, 18, 20-23, 25, and 26 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

35. Claims 5, 11, 13, 15, 16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alcorn (US005745118A) in view of Furtner (US006778177B1).

36. With regard to Claim 5, Alcorn is relied upon for the teachings as discussed above relative to Claim 4.

However, Alcorn does teach that each of the at least two graphics pipelines further includes a scan converter. However, Furtner describes a parallel scan converter (16, Figure 23) that has a plurality of outputs for supplying data to a plurality of pixel pipelines (20, Col. 2, lines 3-16). Therefore, each of the at least two graphics pipelines further includes a scan converter.

The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). Therefore, the scan converter is coupled to the back end circuitry (20), operative to determine the portion of the pixel data to be processed by the back end circuitry.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Alcorn so that each of the at least two graphics pipelines further includes a scan converter as suggested by Furtner. Scan converting is the most popular method of drawing polygons because it uses only integer maths, takes up very little memory, and is simple to understand. The advantages of scan converters are well-known in the art and can be found in many publications, such as Elias' website. Furtner suggests that it is advantageous to have a parallel scan converter for two graphics pipelines because the scan conversion can be performed in parallel (Col. 17, lines 7-22), which increases the speed of processing.

37. With regard to Claim 11, Alcorn describes that the first of the at least two graphics pipelines (Col. 6, lines 33-35, 40-43) further includes circuitry (64, 72, Figure 3), coupled to the front end circuitry (60) and the back end circuitry (76), operative to provide position coordinates of the pixels within the first set of tiles (Col. 10, lines 1-8; *texel data output from the parameter interpolator circuit 64 is provided to the tiler 72, which determines the address of the four texels...checks to determine whether each is within the boundary of the texture...texel data includes the interpolated S, T coordinates as well as the map number*, Col. 11, lines 8-31) to be processed by the back end circuitry (*S, T coordinates for each display screen pixel are provided from the parameter interpolators, through the tiler, to texel interpolator 76*, Col. 12, lines 13-

20), the circuitry including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry (*texel data includes the interpolated S, T coordinates as well as the map number*, Col. 11, lines 15-17).

However, Alcorn does not teach a scan converter. However, Furtner describes a parallel scan converter (16, Figure 23) that has a plurality of outputs for supplying data to a plurality of pixel pipelines (20, Col. 2, lines 3-16). Therefore, the first of the at least two graphics pipelines further includes a scan converter. The scan converter receives, at its input, data which to write onto the graphic primitive to be processed (Col. 1, lines 58-62), and this data inherently comes from a front end circuitry. The output of the scan converter is connected to the pipelines (20, Col. 1, lines 62-66). Therefore, the scan converter is coupled to the front end circuitry and the back end circuitry (20). The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). The scan converter has knowledge with regard to mapping the screen areas onto the memory address area (tiling) (Col. 6, lines 60-65). Therefore, the scan converter is inherently operative to provide memory addresses or position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter inherently including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

38. With regard to Claim 13, Claim 13 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

39. With regard to Claim 15, Claim 15 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

40. With regard to Claim 16, Claim 16 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

41. With regard to Claim 24, Alcorn describes a graphics processing circuit (Col. 3, lines 58-63), comprising front end circuitry (32A, 32B, 32C, Figure 2) operative to generate pixel data in response to primitive data for a primitive to be rendered (*distributes 3-D primitive data evenly among the 3-D geometry accelerator chips*, Col. 6, lines 43-47; *each 3-D geometry accelerator chip processes primitive data*, Col. 6, lines 56-62; *rendering hardware interpolates the primitive data to compute the display screen pixels that are turned on to represent each primitive*, Col. 1, lines 31-33); first back end circuitry (12), coupled to the front end circuitry (Col. 7, lines 5-10), operative to receive and process a portion of the pixel data (Col. 12, lines 13-20) in response to position coordinates (Col. 12, lines 13-20); circuitry (64, 72), coupled between the front end circuitry and the first back end circuitry (76), operative to determine which set of tiles (tiler, Col. 11, lines 8-31) of a repeating tile pattern (Col. 11, lines 35-50) are to be processed by the first back end circuitry (Col. 11, lines 8-31). Alcorn discloses that the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Col. 15, lines 44-57), as shown in Figure 6. Alcorn describes providing the position coordinates to the first back end circuitry in response to the pixel data (Col. 12, lines 13-20). Alcorn describes a memory controller (50,

Figure 2), coupled to the at least two graphics pipelines, operative to transmit and receive the processed pixel data (Col. 6, lines 33-35, 40-43; Col. 8, lines 27-40).

However, Alcorn does not teach two back end circuitries and two scan converters. However, Furtner describes a first scan converter (16, Figure 23). The first scan converter receives, at its input, data which to write onto the graphic primitive to be processed (Col. 1, lines 58-62), and this data inherently comes from a front end circuitry. The output of the scan converter is connected to the pipelines (20, Col. 1, lines 62-66). Therefore, the first scan converter is coupled to the front end circuitry and the first back end circuitry (20). The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). Therefore, the first scan converter is operative to determine which set of tiles are to be processed by the first back end circuitry. The scan converter has knowledge with regard to mapping the screen areas onto the memory address area (tiling) (Col. 6, lines 60-65). Therefore, the first scan converter is inherently operative to provide the memory address area or position coordinates to the first back end circuitry in response to the pixel data. Furtner describes multiple pipelines, and each pipeline processes a cluster of pixel data (Col. 11, lines 41-59; Col. 13, lines 54-63). The scan converter is a parallel scan converter, and provides data to the multiple pipelines in parallel (Col. 2, lines 3-16), so the scan converter is considered to be similar to two scan converters, and the second scan converter performs in a similar manner as the first scan converter for the second back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

Allowable Subject Matter

42. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

43. The prior art singly or in combination do not teach or suggest that each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one, as recited in Claim 19.

44. The closest prior art (Kent) teaches calculating the bounding box of the primitive and testing this against the VisRect. If the bounding box of the primitive is contained in the other P10's super tile the primitive is discarded at this stage [0129]. The method used is to calculate the distance from each subpixel sample point in the point's bounding box to the point's center and compare this to the point's radius. Subpixel sample points with a distance greater than the radius do not contribute to a pixel's coverage. The cost of this is kept low by only allowing small radius points hence the distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within the bounding box [0144]. However, Kent does not teach that each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the

bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US 20030164830A1 teaches a graphics pipeline [0006] that calculates the bounding box of the primitive in a super tile [0129].

2. Elias, Hugo. "Polygon Scan Converting." http://freespace.virgin.net/hugo.elias/graphics/x_polysc.htm.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2671	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,745,118	04-1998	Alcorn et al.	345/587
	B	US-6,778,177	08-2004	Furtner, Wolfgang	345/544
	C	US-2003/0164830	09-2003	Kent, Osman	345/505
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Elias, Hugo. "Polygon Scan Converting." http://freespace.virgin.net/hugo.elias/graphics/x_polysc.htm.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/459,797	LEATHER ET AL.
Examiner	**Art Unit**
Joni Hsu	2671

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	7/22/05
	1	√
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	O
	20	√
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	
	32	
	33	
	34	
	35	
	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

Claim		Date
Final	Original	
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

Claim		Date
Final	Original	
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	
	114	
	115	
	116	
	117	
	118	
	119	
	120	
	121	
	122	
	123	
	124	
	125	
	126	
	127	
	128	
	129	
	130	
	131	
	132	
	133	
	134	
	135	
	136	
	137	
	138	
	139	
	140	
	141	
	142	
	143	
	144	
	145	
	146	
	147	
	148	
	149	
	150	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Bib Data Sheet

CONFIRMATION NO. 4148

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,797	06/12/2003 RULE	345	2676	00100.02.0053

APPLICANTS

Mark M. Leather, Saratoga, CA;

Eric Demers, Palo Alto, CA;

** CONTINUING DATA **********

This appln claims benefit of 60/429,641 11/27/2002

** FOREIGN APPLICATIONS **********

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/07/2003

Foreign Priority claimed	STATE OR	SHEETS	TOTAL	INDEPENDENT
☐ yes ☑ no				
35 USC 119 (a-d) conditions met ☐ yes ☑ no ☐ Met after Allowance				
Verified and Acknowledged Examiner's Signature Initials	COUNTRY CA	DRAWING 5	CLAIMS 24	CLAIMS 3

ADDRESS
29153
ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO , IL
60601

TITLE
Dividing work among multiple graphics pipelines using a super-tiling technique

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)

1122		☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/459,797	LEATHER ET AL.	
Examiner	**Art Unit**	
Joni Hsu	2671	

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505	12/7/2004	JH
Above	UPDATED	7/26/2005	JH
345	588, 544	7/26/2005	JH
345	545, 532	7/26/2005	JH
345	501, 502	7/26/2005	JH
345	531	7/26/2005	JH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached search history.	7/26/2005	JH

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Group: 2676
Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of First Class Mailing
I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

1-3-06
Date

Christine A. Wright

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed August 1, 2005, Applicants submit the following Amendment and Response.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. (previously presented) The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory.

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first

set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip

and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (currently amended) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (original) The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

24. (currently amended) A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry[[.]] operative to [[receive]] transmit and receive the processed pixel data.

25. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two

graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions.

26. (previously presented) The graphics processing circuit of claim 25 wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants with to thank the Examiner for the notice that claim 19 would be allowable if rewritten in independent form.

Claims 1-4, 6-8, 9, 10, 12, 14, 17, 18, 20-23, 25 and 26 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,745,118 (Alcorn). The independent claims have been amended to include inherent language indicating that the tiles described in the specification and claimed correspond to screen locations and may have corresponding frame buffer memory locations as well. Alcorn is directed to different structure and operations from that claimed and instead is directed to texture space source data. Alcorn describes a 3D bypass structure for the download of textures and describes a system that receives primitive information from a host processor and passes it through a distributor 30 which then distributes 3D primitive data evenly among the 3D geometry accelerator chips. In this way, for example, three groups of primitives are operated upon simultaneously. The multiple 3D geometry accelerator chips determine object red, green and blue values and texture values for the screen space coordinates and they also perform view clipping operations. The output from these multiple 3D geometry accelerator chips are then passed to a concentrator chip 36 which combines the 3D primitive output data received from the 3D geometry accelerator chips and reorders the primitives to the original order that they had prior to being distributed by the distributor chip 30. (See for example, column 6, line 42 through column 7, line 10). As such, distribution of primitive data is done merely in a round robin type approach wherein each graphics accelerator chip receives an even distribution of primitives. The texture mapping board 12 then receives the primitives in the same order that the distributor receives them in and then processes them in that order.

In contrast, Applicants' claims are directed to a different operation – render space destination data. There is no teaching or suggestion in Alcorn of at least two graphics pipelines that process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

It appears that the Alcorn reference actually teaches a type of round robin or sequential load balancing for texture source data in a front end. In contrast, Applicants describe, for example, a multi-pipeline system that performs pixel operations on pixels within a determined set of tiles by a corresponding one of a plurality of graphics pipelines based on a set of tiles of a repeating tile pattern corresponding to screen locations. In one embodiment, a scan converter determines, for example, whether pixels within portions of an object, such as a triangle, intersect with tiles that backend circuitry is responsible for processing. No tile based load distribution appears to be taught or suggested in the cited reference. Accordingly, the claims are believed to be in condition for allowance.

For example, the office action cites Alcorn, column 6, lines 40-43 as allegedly teaching a plurality of graphics pipelines. This portion refers to the multiple accelerator chips 32a-32c, for example. The office action then cites to column 11, lines 8-31 as teaching the processing of corresponding sets of tiles. However, this cited portion actually refers to the texture mapping board which is not part of the graphics accelerator chips. In fact, the graphics pipelines (i.e. the graphics accelerator chips) merely process data in a round robin fashion and do not process data based on tiles of a repeating tile pattern. Accordingly, the independent claims are in condition for allowance.

The office action also cites to Alcorn at column 15, lines 44-57. However again, this portion refers to the texture mapping board 12 which again processes data in the order in which

the distributor 30 received them. The portion referred to in the office action actually refers to the storage of texels in a MIP map so that the tiler 72 in the texture mapping board can access texels in the texel cache access 82. There is no teaching or suggestion that any texture tiles correspond to screen locations nor a plurality of pipelines that process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations wherein the pattern includes a horizontally and vertically repeating pattern of the square regions. Accordingly, claims 1, 20, 24 and 25 are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, claim 3 requires that the square regions are 2-dimensional partition of memory in a frame buffer. However, the cited portion of Alcorn actually indicates that the texture map which actually comes from the texture cache 48 and not the frame buffer VRAMs, is combined in the frame buffer board to generate the final RGB values for each display screen pixel.

Also for example, with respect to claim 14, again the office action cites the 3D geometry accelerator chips of Alcorn as the claimed graphics pipelines. However, these 3D geometry accelerators do not process pixel data in the set of tiles in a repeating tile pattern as alleged in the office action. As noted above, the texture mapping board obtains texels for texture mapping and this board is not part of the front end board 10. Accordingly, the claim is in condition for allowance.

Claims 5, 11, 13, 15, 16 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Alcorn in view of U.S. Patent No. 6,778,177 (Furtner). Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance.

In addition, the Furtner reference is directed to a method for rasterizing a graphics component. Claim 5 requires that each of the graphics pipeline each include a scan converter.

However, the cited portion of Furtner merely describes a parallel scan converter not a scan converter for each of the pixel pipelines. Accordingly, the claim is in condition for allowance. As to claim 11, this claim requires, among other things, a scan converter for one of the graphics pipelines that provides position coordinates of pixels within the first set of tiles to be processed by the back end circuitry and that the scan converter includes a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry. The office action cites column 10, lines 1-8 of Alcorn. However, the cited portion merely describes that there are texture map coordinates that are generated that correspond to the pixel. The cited portion actually refers to the back end circuit of Alcorn, namely the texture mapping card or board 12 (see FIG. 3). As such, the claim is in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 1/3/06

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005

PTO/SB/22 (12-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2005 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 00100.02.0053
Application Number 10/459,797	Filed June 12, 2003
For DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE	
Art Unit 2676	Examiner Joni Hsu

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$120	$60	$
☑ Two months (37 CFR 1.17(a)(2))	$450	$225	$ 450.00
☐ Three months (37 CFR 1.17(a)(3))	$1020	$510	$
☐ Four months (37 CFR 1.17(a)(4))	$1590	$795	$
☐ Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 22-0259. I have enclosed a duplicate copy of this sheet.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

01/06/2006 SHASSEN1 00000034 220259 10459797
01 FC:1252 450.00 DA

I am the ☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration Number 34,414

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature — January 3, 2006 (Date)

Christopher J. Reckamp (Typed or printed name) — 312-609-7599 (Telephone Number)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

TFW $2616

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2676
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☑ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☑ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  -return postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Vedder, Price, Kaufman & Kammholz, P.C.		
Signature			
Printed name	Christopher J. Reckamp		
Date	January 3, 2006	Reg. No.	34,414

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Christine A. Wright	Date	January 3, 2006

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

1-506

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 6	=
Independent	* 4	Minus	*** 7	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	355	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L2	273	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L3	294	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L4	40	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L5	92	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L6	478	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L7	72	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L8	740	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35

EAST Search History

L9	364	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L10	613	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L11	1322	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L12	1053	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L13	115	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L14	87	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L15	226	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L16	303	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35

EAST Search History

L17	81	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L18	76	(multiple plurality) near2 pipelin$3 and scan adj conver$5 and pixel$1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L19	84	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35
L20	34	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/03/01 15:35

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 03/13/2006

ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-26* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In light of Applicant's amendment to Claim 24, the objection to Claim 24 has been withdrawn.

2. Applicant's arguments with respect to claims 1-18 and 20-26 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see page 9, filed January 5, 2006, with respect to the rejection(s) of claim(s) 1-4, 6-10, 12, 14, 17, 18, 20-23, 25, and 26 under 35 U.S.C. 102(b) and claims 5, 11, 13, 15, 16, and 24 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Furtner (US006778177B1).

4. Applicant argues that Alcorn (US005745118A) is directed to texture space source data and not to tiles corresponding to screen locations (page 9).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Furtner.

5. Applicant's arguments filed January 5, 2006, with respect to Claim 5 have been fully considered but they are not persuasive.

6. With regard to Claim 5, Applicant argues that Furtner describes a parallel scan converter not a scan converter for each of the pixel pipelines (pages 11-12).

In reply, the Examiner disagrees. Furtner does teach a scan converter for each of the pixel pipelines (Col. 6, lines 47-51).

Specification

7. The disclosure is objected to because of the following informalities: Paragraph [0001] states that this application is a related application to a co-pending application, but does not provide the serial number for this co-pending application.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-17 and 20-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Furtner (US006778177B1).

10. With regard to Claim 1, Furtner describes a graphics processing circuit, comprising at least two graphics pipelines (20, Figure 23; Col. 2, lines 11-14) operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (Figure 21b, Col. 1, lines 40-49).

11. With regard to Claim 2, Furtner describes that the square regions comprise a two dimensional partitioning of memory (10, Figure 21b; Col. 1, lines 40-49).

12. With regard to Claim 3, Furtner describes that the memory is a frame buffer (10, Figure 21b; Col. 1, lines 40-49).

13. With regard to Claim 4, Furtner describes that each of the at least two graphics pipelines further includes front end circuitry (102, Figure 1) operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered (Col. 8, lines 38-44) , and back end circuitry (108), coupled to the front end circuitry, operative to receive and process a portion of the pixel data (Col. 8, lines 51-60).

14. With regard to Claim 5, Furtner describes that each of the at least two graphics pipelines further includes a scan converter (16, Figure 23) (Col. 2, lines 3-16; Col. 6, lines 47-51). The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). Therefore, the scan converter is coupled to the back end circuitry (20), operative to determine the portion of the pixel data to be processed by the back end circuitry.

15. With regard to Claim 6, Furtner describes that each tile of the set of tiles further comprises a 16x16 pixel array (Col. 11, lines 45-48, 64-65).

16. With regard to Claim 7, Furtner describes that the at least two graphics pipelines (108, Figure 1) separately receive the pixel data from the front end circuitry (102) (Col. 8, lines 51-57).

17. With regard to Claim 8, Furtner describes that the at least two graphics pipelines are on multiple chips (Col. 6, lines 47-51).

18. With regard to Claim 9, Furtner describes a memory controller (22, Figure 23) coupled to the at least two graphics pipelines (20), operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory (24) (Col. 2, lines 20-34).

19. With regard to Claim 10, Furtner describes that a first of the at least two graphics pipeline processes the pixel data only in a first set of tiles in the repeating tile pattern (Figure 21b, Col. 1, lines 41-49).

20. With regard to Claim 11, Furtner describes that the first of the at least two graphics pipelines further includes a scan converter (16; Col. 2, lines 3-16). The scan converter receives, at its input, data which to write onto the graphic primitive to be processed (Col. 1, lines 58-62), and this data inherently comes from a front end circuitry. The output of the scan converter is connected to the pipelines (20, Col. 1, lines 62-66). Therefore, the scan converter is coupled to the front end circuitry and the back end circuitry (20). The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). The scan converter has knowledge with regard to mapping the screen areas onto the memory address area (tiling) (Col. 6, lines 60-65). Therefore, the scan converter is inherently operative to provide memory addresses or position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter inherently including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

21. With regard to Claim 12, Furtner describes that a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern (Figure 21b, Col. 1, lines 41-49).

22. With regard to Claim 13, Claim 13 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

23. With regard to Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Furtner describes four graphics pipelines (Col. 1, lines 37-49). Therefore, Claim 14 is rejected under the same rationale as Claims 4 and 10.

24. With regard to Claim 15, Claim 15 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

25. With regard to Claim 16, Claim 16 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

26. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

27. With regard to Claim 20, Furtner describes a graphics processing method, comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data (Col. 8, lines 38-44); determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations (Figure 21b, Col. 1, lines 41-49) to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data (Col. 11, lines 41-59; Col. 13, lines 54-63), the repeating tile pattern including a horizontally and vertically

repeating pattern of square regions; and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines (Figure 21b, Col. 1, lines 41-49).

28. With regard to Claim 21, Furtner describes determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for (Col. 11, lines 41-49; Col. 13, lines 54-63).

29. With regard to Claim 22, Furtner describes that the scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). The scan converter has knowledge with regard to mapping the screen areas onto the memory address area (tiling) (Col. 6, lines 60-65). Furtner discloses that determining the pixels within a set of tiles of the repeating tile pattern to be processed (Col. 1, lines 41-49) inherently further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

30. With regard to Claim 23, Furtner describes transmitting the processed pixels to memory (24, Figure 23; Col. 2, lines 20-34).

31. With regard to Claim 24, Furtner describes a graphics processing circuit, comprising front end circuitry (102, Figure 1) operative to generate pixel data in response to primitive data for a primitive to be rendered (Col. 8, lines 38-44); first back end circuitry (108a), coupled to the

front end circuitry (Col. 8, lines 51-57), operative to process a first portion of the pixel data in response to position coordinates; a first scan converter (16, Figure 23). The first scan converter receives, at its input, data which to write onto the graphic primitive to be processed (Col. 1, lines 58-62), and this data inherently comes from a front end circuitry. The output of the scan converter is connected to the pipelines (20, Col. 1, lines 62-66). Therefore, the first scan converter is coupled to the front end circuitry and the first back end circuitry (20). The scan converter determines which clusters of pixel data are to be processed by which pipeline (Col. 11, lines 41-59; Col. 13, lines 54-63). Therefore, the first scan converter is operative to determine which set of tiles of a repeating tile pattern (Figure 21b, Col. 1, lines 41-49) are to be processed by the first back end circuitry. The scan converter has knowledge with regard to mapping the screen areas onto the memory address area (tiling) (Col. 6, lines 60-65). Therefore, the first scan converter is inherently operative to provide the memory address area or position coordinates to the first back end circuitry in response to the pixel data. Furtner describes multiple pipelines, and each pipeline processes a cluster of pixel data (Col. 11, lines 41-59; Col. 13, lines 54-63). The scan converter is a parallel scan converter, and provides data to the multiple pipelines in parallel (Col. 2, lines 3-16), so the scan converter is considered to be similar to two scan converters, and the second scan converter performs in a similar manner as the first scan converter for the second back end circuitry. Furtner also describes that each pipeline has a scan converter (Col. 6, lines 47-51). Furtner describes a memory controller (24, Figure 23), coupled to the first and second back end circuitry (20) operative to transmit and receive the processed pixel data (Col. 2, lines 30-34).

32. With regard to Claim 26, Furtner describes that the horizontally and vertically repeating pattern of regions (Figure 21b, Col. 1, lines 41-49) include NxM number of pixels (Col. 11, lines 45-55).

33. Thus, it reasonably appears that Furtner describes or discloses every element of Claims 1-17 and 20-26 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

36. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furtner (US006778177B1) in view of Alcorn (US005745118A).

Furtner is relied upon for the teachings as discussed above relative to Claim 14.

However, Furtner does not teach a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Alcorn describes a bridge (30, Figure 2) operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines (Col. 6, lines 32-35, 40-47; Col. 7, lines 28-33; Col. 5, line 65-Col. 6, line 3).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Furtner to include a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Alcorn because Alcorn suggests the advantage of being able to evenly distribute the vertex data among the graphics pipelines. In this manner, the system bandwidth is increased because the groups of vertex data are operated upon simultaneously (Col. 6, lines 43-49).

Allowable Subject Matter

37. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

38. The prior art singly or in combination do not teach or suggest that each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box

does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one, as recited in Claim 19.

39. The closest prior art (Kent) teaches calculating the bounding box of the primitive and testing this against the VisRect. If the bounding box of the primitive is contained in the other P10's super tile the primitive is discarded at this stage [0129]. The method used is to calculate the distance from each subpixel sample point in the point's bounding box to the point's center and compare this to the point's radius. Subpixel sample points with a distance greater than the radius do not contribute to a pixel's coverage. The cost of this is kept low by only allowing small radius points hence the distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within the bounding box [0144]. However, Kent does not teach that each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20030164830A1 teaches a graphics pipeline [0006] that calculates the bounding box of the primitive in a super tile [0129].

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

U Chauhan

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
10/459,797	LEATHER ET AL.
Examiner	**Art Unit**
Joni Hsu	2671

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	Jan 25
	1	√
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	O
	20	√
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	
	32	
	33	
	34	
	35	
	36	
	37	
	38	
	39	
	40	
	41	
	42	
	43	
	44	
	45	
	46	
	47	
	48	
	49	
	50	

Claim		Date
Final	Original	
	51	
	52	
	53	
	54	
	55	
	56	
	57	
	58	
	59	
	60	
	61	
	62	
	63	
	64	
	65	
	66	
	67	
	68	
	69	
	70	
	71	
	72	
	73	
	74	
	75	
	76	
	77	
	78	
	79	
	80	
	81	
	82	
	83	
	84	
	85	
	86	
	87	
	88	
	89	
	90	
	91	
	92	
	93	
	94	
	95	
	96	
	97	
	98	
	99	
	100	

Claim		Date
Final	Original	
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	
	114	
	115	
	116	
	117	
	118	
	119	
	120	
	121	
	122	
	123	
	124	
	125	
	126	
	127	
	128	
	129	
	130	
	131	
	132	
	133	
	134	
	135	
	136	
	137	
	138	
	139	
	140	
	141	
	142	
	143	
	144	
	145	
	146	
	147	
	148	
	149	
	150	

Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
10/459,797	LEATHER ET AL.	
Examiner	**Art Unit**	
Joni Hsu	2671	

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545	7/26/2005	JH
345	532, 501	7/26/2005	JH
345	502, 531	7/26/2005	JH
Above	UPDATED	3/1/2006	JH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
See attached search history.	3/1/2006	JH

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2671
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,424,345 B1	07-23-2002	Smith et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2671
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		European Search Report from European Patent Office; European Application No. 03257464.2; dated April 4, 2006	
		FOLEY, James et al.; Computer Graphics, Principles and Practice; Addison-Wesley Publishing Company; 1990; pages 873-899	
		CROCKETT, Thomas W.; An introduction to parallel rendering; Elsevier Science B.V.; 1997; pages 819-843	
		MONTRYM, John S. et al.; InfiniteReality: A Real-Time Graphics System; Silicon Graphics Computer Systems; 1997; pages 293-302	
		HUMPHREYS, Greg et al.; WireGL: A Scalable Grpahics System for Clusters; ACM Siggraph; 2001; pages 129-140	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	1017094
Application Number:	10459797
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	04-APR-2006
Filing Date:	12-JUN-2003
Time Stamp:	15:16:21
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Information Disclosure Statement (IDS) Filed	IDS_10459797.pdf	162453	no	2

Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	NPL Documents	EPSearchReport_10459797.pdf	118954	no	4
Warnings:					
Information:					
3	NPL Documents	Foley_10459797.pdf	1599163	no	28
Warnings:					
Information:					
4	NPL Documents	Crockett_10459797.pdf	1355723	no	25
Warnings:					
Information:					
5	NPL Documents	Montrym_10459797.pdf	693876	no	10
Warnings:					
Information:					
6	NPL Documents	Humphreys_10459797.pdf	1144513	no	12
Warnings:					
Information:					
		Total Files Size (in bytes):	5074682		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2671
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Electronic Submission

I hereby certify that this Response is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop AF on this date.

6-13-06
Dated

Christine A. Wright

RESPONSE

Dear Sir:

In response to the Final Office Action mailed March 13, 2006, Applicants submit the following response.

Listing of the Claims begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

LISTING OF THE CLAIMS

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile,

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines are on multiple chips.

9. (previously presented) The graphics processing circuit of claim 1, further including a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory.

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front

end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to

be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (previously presented) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; and

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (original) The graphics processing method of claim 20, further comprising transmitting the processed pixels to memory.

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions.

26. (previously presented) The graphics processing circuit of claim 25 wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

REMARKS

Claims 1-26 are now pending in the application. Applicants respectfully traverse and request reconsideration.

Claims 1-18, 20-26 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Furtner (U.S. Pat. No. 6,778,177).

With regard to claim 1, Furtner fails to show, teach, or suggest, inter alia, at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

Furtner is directed to a method for rasterizing a graphics basic component. The Examiner cites Figure 21b and Col. 1, lines 40-49, which is located in the "Background" section of Furtner, as disclosing at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, this portion merely discloses a method of accelerating image-rendering of three-dimensional images. The method uses multi-processors or hardware pipelines in parallel. Each processor or pipeline may be responsible for rendering only a single contiguous block of pixels as illustrated in Figure 21a. As such, no processor or pipeline processes a repeated tile pattern as required by the claim. Figure 21b depicts a per pixel, not a repeating tile pattern, based processing scheme. For example, the processing of each individual pixel is effected in an interleaved manner by the processors or pipelines. Neither of these configurations process a set of tiles (or blocks of pixels) in a repeating pattern that includes a horizontally and vertically repeating pattern of square regions. Therefore, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Claims 20, 24, and 25 are allowable for at least similar reasons as claim 1. Thus, reconsideration and withdrawal of the rejections is respectfully requested.

Claims 2-19, 21-23, and 26 each ultimately depend on claims 1, 20, 24, and 25, respectively, and are therefore allowable for at least similar reasons and are believed to be allowable for having novel and non-obvious subject matter.

The Examiner states that claim 19 would be allowable if rewritten in independent form. Applicants have presently refrained from rewriting claim 19 in view of the discussion above. Applicants reserve the right to amend claim 19 into their originally allowable form at a later date if needed.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this response is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (312) 609-7500.

Respectfully submitted,

Date: 6/13/06

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Acknowledgement Receipt

EFS ID:	1076773
Application Number:	10459797
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	13-JUN-2006
Filing Date:	12-JUN-2003
Time Stamp:	14:27:17
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		10459797_Response.pdf	325832	yes	9

	Multipart Description		
	Doc Desc	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	9
Warnings:			
Information:			
	Total Files Size (in bytes):	325832	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	24	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
	BASIC FEE	375.00	OR		BASIC FEE	750.00
	X$ 9=		OR		X$18=	72
	X42=		OR		X84=	
	+140=		OR		+280=	
	TOTAL		OR		TOTAL	

CLAIMS AS AMENDED - PART II

1-5-06

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 26	Minus	** 6	=
Independent	* 4	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
	X$ 9=		OR		X$18=	
	X42=		OR		X84=	
	+140=		OR		+280=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

6/13/06

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 20	= 4
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
	X$ 9=		OR		X$18=	
	X42=		OR		X84=	
	+140=		OR		+280=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
	X$ 9=		OR		X$18=	
	X42=		OR		X84=	
	+140=		OR		+280=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 06/22/2006

ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 06/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/459,797	Applicant(s) LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2628	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 June 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *see attached sheet*. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: *19*.
   Claim(s) rejected: *1-18 and 20-26*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached sheet.
12. ☒ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). 4/4/06
13. ☐ Other: _____.

Applicant argues that Furtner (US006778177B1) does not teach at least two graphics pipeline operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (page 8).

In reply, the Examiner disagrees. According to Applicant's disclosure, this repeating tile pattern for the two pipe configuration refers to a "checkerboard" pattern [0045] wherein each pipe is responsible for generating all of the pixels with its assigned tiles, and the tiles are distributed evenly across all pipes, in a checkerboard pattern [0047], and the patterns repeat across the whole screen, in both X & Y directions [0048], as shown in Figure 3. Furtner discloses subdividing a frame buffer into sub-sections which normally have the same size and associating each sub-section with a processor so that each of the processors is equally loaded (Col. 1, lines 23-32). Figure 21 shows two possibilities of partitioning the frame buffer with regard to the case of a graphics system operating with four graphics processing engines. Figure 21a shows that frame buffer 10 is subdivided into four equally sized blocks which are associated to the engines. Figure 21b shows that the processing of individual pixels 12 is effected in an interleaved manner by the four graphics processing engines of the graphics system (Col. 1, lines 37-49), and as can be seen in Figure 21, this results in a checkerboard pattern. Even though Figure 21b is described as partitioning the frame buffer into individual pixels, this is described as being only one possibility of partitioning the frame buffer (Col. 1, lines 37-39). Furtner describes subdividing a frame buffer into sub-sections which normally have the same size (Col. 1, lines 30-32) and does not specify the each sub-sections must contain only one pixel, and in fact describes that the sub-sections can be four equally sized blocks or tiles (Col. 1, lines 41-44).

Therefore, Furtner does disclose at least two graphics pipeline operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

PTO/SB/08A (06-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2671
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JH		US- 6,424,345 B1	07-23-2002	Smith et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	06/14/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2671
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
JH	1	European Search Report from European Patent Office; European Application No. 03257464.2; dated April 4, 2006	✓
JH	2	FOLEY, James et al.; Computer Graphics, Principles and Practice; Addison-Wesley Publishing Company; 1990; pages 873-899	✓
JH	3	CROCKETT, Thomas W.; An introduction to parallel rendering; Elsevier Science B.V.; 1997; pages 819-843	✓
JH	4	MONTRYM, John S. et al.; InfiniteReality: A Real-Time Graphics System; Silicon Graphics Computer Systems; 1997; pages 293-302	✓
JH	5	HUMPHREYS, Greg et al.; WireGL: A Scalable Grpahics System for Clusters; ACM Siggraph; 2001; pages 129-140	✓

Examiner Signature	/Joni Hsu/	Date Considered	06/14/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

PATENT
DOCKET NO. 00100.02.0053

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2671
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Electronic Submission

I hereby certify that this Response is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop AF on this date.

6-13-06
Dated

Christine A. Wright

RESPONSE

Dear Sir:

Do not enter 6/16/06

In response to the Final Office Action mailed March 13, 2006, Applicants submit the following response.

Listing of the Claims begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

PTO/SB/31 (04-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): 00100.02.0053

I hereby certify that this correspondence is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop AF

on July 13, 2006

Signature: Christine Wright

Typed or printed name: Christine A. Wright

In re Application of: Mark M. Leather et al.

Application Number	Filed
10/459,797	June 12, 2003

For: DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

Art Unit	Examiner
2628	Joni Hsu

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 500.00

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0441 . I have enclosed a duplicate copy of this sheet.

☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record. Registration number 34,414.

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

Signature: Christopher J. Reckamp

Typed or printed name: Christopher J. Reckamp

Telephone number: 312-609-7599

Date: July 13, 2006

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
Approved for use through xx/xx/200x. OMB 0651-00xx
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 00100.02.0053

I hereby certify that this correspondence is being forwarded via electronic submission to:
Electronic Business Center, Commissioner for Patents, Mail Stop AF

on July 13, 2006

Signature: Christine Wright

Typed or printed name: Christine A. Wright

Application Number	Filed
10/459,797	June 12, 2003

First Named Inventor: Mark M. Leather

Art Unit	Examiner
2628	Joni Hsu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 34,414.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Christopher J. Reckamp
Typed or printed name

312-609-7599
Telephone number

July 13, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Electronic Submission

I hereby certify that the this Remarks for Pre-Appeal Brief Request for Review is being forwarded via electronic submission to: Electronic Business Center, Commissioner of Patents, Mail Stop AF, on this date.

7-13-06
Date

Christine Wright

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants respectfully submit that the Examiner's rejections include clear errors because one or more limitations are not met by the cited reference and the reference does not teach what the Examiner alleges. Claims 1-18 and 20-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Furtner.

As to claim 1, Applicants claim a graphics processing circuit that includes at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. The Furtner reference fails to teach the claimed subject matter.

Furtner instead describes a non-repeating tile pattern approach and alternatively a per pixel processing approach, neither of which anticipate the claimed subject matter. The cited

FIG. 21A shows a non-repeating tile based approach, and is the only tile based approach described by the cited portion of Furtner. This non-repeating tile based approach is different from the claimed approach in at least that the Furtner tile approach breaks down a frame into a non-repeating four tile configuration wherein each of one of four graphics engine processes a single tile. There is no repeating tile pattern utilized that includes horizontally and vertically repeating tile patterns wherein a respective graphics pipeline is operative to process data in repeating patterns of square regions. For example, only a single tile is processed by each engine for a frame as taught by Furtner. Furtner does not use a horizontally and vertically repeating tile pattern within a frame but only describes using a single tile per engine.

In contrast, as shown in Applicants' Specification and as claimed, Applicants' approach breaks down screen locations of a frame into a repeating tile pattern that includes horizontally and vertically repeating patterns of square regions where a respective graphics pipeline operates to process data in a dedicated tile of the repeating tile pattern. As such, one engine in Applicants' apparatus is configured to process multiple tiles in a repeating tile pattern to effect, among other things, improved loading. As admitted in the Advisory Action, FIG. 21A merely shows a frame buffer 10 subdivided into four equally sized blocks where each block is associated to one engine. There is no repeating pattern of horizontal and vertical tiles shown in FIG. 21A nor is there any description of an apparatus that operates or is configured as Applicants' claim requires.

The Advisory Action also appears to read information into the Furtner reference based on Applicants' own claimed invention. For example, when applying FIG. 21B of Furtner, which merely shows a non-tile based approach wherein each pixel is handled individually by a different graphics processing engine, the office action alleges that this is "only one possibility of

portioning the frame buffer". Applicants respectfully note that the reference actually states that the two versions shown in FIG. 21A and FIG. 21B are actually "the above-described possibilities" (column 1, lines 37) meaning that these techniques are the ones described in the paragraphs above disclosed by Furtner. The reference cannot be cited for possibilities that are not disclosed in the reference.

In any event, the actual teaching in Furtner is as FIG. 21A and FIG. 21B show. FIG. 21B is a non-tile based approach whereas Applicants claim a repeating tile based approach and Furtner describes with respect to this figure that a separate engine handles a single pixel. As such, it is a per pixel approach and not a tile based approach.

In addition, the Advisory Action states Furtner describes "subdividing a frame buffer into subsections which normally have the same size (column 1, lines 30-32) and does not specify [that] each subsections must contain only one pixel, and in fact describes that the subsections can be four equally sized blocks or tiles (column 1, lines 41-44)." (Page 2 of Advisory Action). Applicants respectfully submit that the cited portion and, as admitted by the Advisory Action, requires a system that utilizes four equally sized blocks or tiles, each tile being handled by a different graphics processing engine and that only one tile per engine is (four blocks or tiles) described and shown. No repeating tile pattern per frame is employed. Although Furtner describes a tile based approach, he describes it as four tiles for a frame and each tile being processed by a different graphics processing engine. This is a non-repeating tile based approach.

In contrast, Applicants claim a repeating tile pattern approach wherein, among other things, respective graphics pipelines processed dedicated tiles of a repeating tile pattern. The only tile based approach taught in Furtner is a non-repeating tile approach. As such, the reference does not anticipate Applicants' claimed invention. In addition, Applicants respectfully

note that the Advisory Action also appears to exclude claim language in an effort to render the claim unpatentable. As shown on page 3 of the Advisory Action, the Examiner's use of Applicants' claim language fails to include that a respective one of at least two graphics pipelines are operative to process data in a dedicated tile wherein there is a repeating tile pattern. As noted, there is no repeating tile pattern shown in the figures or described in the cited portion of Furtner.

Applicants respectfully reassert the relevant remarks made above with respect to other independent claims.

The dependent claims add additional novel and non-obvious subject matter.

As to claim 25, Applicants again respectfully submit that there is no repeating tile pattern that includes a horizontally and vertically repeating patterns of regions wherein graphics pipelines are operative to process data in corresponding sets of tiles of a repeating tile pattern corresponding to screen locations. As such, this claim is also believed to be in condition for allowance.

Reconsideration and withdrawal of the rejection of the claims is respectfully requested. A Notice of Allowance is also respectfully requested.

Respectfully submitted,

Date: 7/13/06

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	1401	1	500	500
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	120	120
Miscellaneous:				
		Total in USD ($)		**620**

Electronic Acknowledgement Receipt

EFS ID:	1112614
Application Number:	10459797
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	13-JUL-2006
Filing Date:	12-JUN-2003
Time Stamp:	18:28:02
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$620
RAM confirmation Number	419
Deposit Account	500441
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Notice of Appeal Filed	10459797_NoticeofAppeal.pdf	87816	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	10459797_PreAppealBriefRequest.pdf	72556	no	1
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	10459797_Remarks.pdf	173743	no	4
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	8337	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	342452		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 01/16/2007

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/459,797	LEATHER ET AL.	
	Joni Hsu	Art Unit 2628	

Document Code - AP.PRE.DEC

Notice of Panel Decision from Pre-Appeal Brief Review

This is in response to the Pre-Appeal Brief Request for Review filed 7/13/06.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☐ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☐ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☒ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *Ulka Chauhan*.

(2) *Kee Tung*.

(3) *Joni Hsu*.

(4)_____.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	402	345/506.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L2	319	345/530.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L3	319	345/505.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L4	47	345/588.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L5	105	345/544.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L6	517	345/545.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03
L7	79	345/532.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:03

EAST Search History

L8	805	345/501.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:04
L9	405	345/502.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:04
L10	664	345/531.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:04
L11	1652	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:05
L12	1336	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:05
L13	147	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:06
L14	111	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:07

EAST Search History

L16	258	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:11
L17	356	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:12
L18	106	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:12
L19	101	18 and pixel$1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:12
L20	95	non adj square same til$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:13
L21	39	repeat$3 and til$3 and 20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:14
L22	22	parallel adj processor$1 with graphic$1 and pixel$1 and (til$3 block$1) and repeat$3 and pattern$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:16

EAST Search History

L23	78	parallel adj processor$1 with graphic$1 and pixel$1 and (til$3 block$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/24 10:16

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 02/09/2007

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-18 and 20-26 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 1-3, filed July 13, 2006, with respect to the rejection(s) of claim(s) 1-7 and 20-26 under 35 U.S.C. 102(e) and Claims 8-18 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kelleher (US005794016A).

3. Applicant argues that Furtner (US006778177B1) describes a non-repeating tile pattern approach and alternatively a per pixel processing approach, neither of which anticipate the claimed subject matter (page 1). The cited FIG. 21A shows a non-repeating tile based approach, and is the only tile based approach described by the cited portion of Furtner. Furtner describes that the per pixel processing approach is repeating. However, Furtner does not teach a repeating tile based approach. The Examiner attempted to cite the reference for possibilities that are not disclosed in the reference (pages 2-3).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Kelleher.

Claim Objections

4. Claim 25 is objected to because it is exactly the same as Claim 1, and therefore is a repeated claim. Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 20-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 20 recites a graphics processing method, however it appears to be directed to an abstract idea rather than a practical application of the abstract idea. The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result (*State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02). The tangible requirement requires that the claim must set forth a practical application of the 101 judicial exception to produce a real-world result (*Benson*, 409 U.S. at 71-72, 175 USPQ at 676-77). See MPEP 2106 II A. Since there is no tangible result recited in these claims, these claims are directed to non-statutory subject matter.

Claims 21-23 are non-statutory for the same reasons discussed above.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-5, 7, 9, 10, 12-16, 18, and 20-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelleher (US005794016A).

9. With regard to Claim 1, Kelleher discloses a graphics processing circuit (10C, Figure 3) comprising at least two graphics pipelines (20A, 20B; *graphics system 10C with N rendering processors 20A-20N*, Col. 3, lines 22-23; *rendering processor 20 provides a video pipeline*, Col. 4, lines 9-14) operative to process data in a corresponding set of tiles (group of pixel blocks 52, Figure 4) of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions, as shown in Figure 4 (*graphics memory 22 that has been partitioned into a plurality of pixel blocks 52 that are tiled in the x- and y-direction of the graphics memory 22, the graphics memory 22 renders a 1280x1024 screen display, pixel blocks 52 are organized into noncontiguous groups of blocks 52, groups of blocks 52 are then assigned to the rendering processors 20, each rendering processor 20 writes only those pixels that are located in the blocks 52 of the assigned groups*, Col. 4, line 60-Col. 5, line 19).

10. With regard to Claim 2, Kelleher discloses that the square regions (blocks 52) comprise a two dimensional partitioning of memory (22, Figure 4) ((*graphics memory 22 that has been partitioned into a plurality of pixel blocks 52 that are tiled in the x- and y-direction of the graphics memory 22,* Col. 4, lines 60-62).

11. With regard to Claim 3, Kelleher discloses that the memory (22, Figure 4) is a frame buffer (*graphics memory 22, also known as a frame buffer*, Col. 3, lines 38-41).

12. With regard to Claim 4, Kelleher discloses that each of the at least two graphics pipelines (20A, 20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) further includes front end circuitry (80, 82, Figure 7) operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry (84, Figure 7), coupled to the front end circuitry, operative to receive and process a portion of the pixel data (*each of the rendering processors 20 independently scan-converts the geometric objects, the rendering processor 20 first reads the command packets, the rendering processors 20 then processes the command packets in a pipeline process comprising a dispatch stage 80, a setup stage 82, and an updated stage 84, in a dispatch stage 80, the dispatch circuit 64 reads the command packets from the command queue 62 and dispatches the vertex data in the command to the next stage in the pipeline, the setup stage 82, the setup stage 82 includes the geometric setup circuit 66 and the attribute setup circuit 70 which accept the triangle vertex data and setup the triangles for scan-conversion by the*

update stage 84, the update stage 84 includes the interpolator circuit 72, which interpolates final attribute values for the pixels in each triangle, Col. 8, line 52-Col. 9, line 23).

13. With regard to Claim 5, Kelleher discloses that each of the at least two graphics pipelines (20A, 20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) further includes a scan converter (84, Figure 7), coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry (*scan-converts the geometric objects into the memory blocks 52 indicated by their block enable field 61*, Col. 8, lines 52-61; *scan-conversion by the update stage 84*, Col. 9, lines 1-23; *block enable field 61 determines which groups of blocks 52 within the graphics memory 22 are allocated to and controlled by the rendering processor 20*, Col. 6, lines 26-28).

14. With regard to Claim 7, Kelleher discloses that the at least two graphics pipelines 20A, (20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) separately receive the pixel data from the front end circuitry (Col. 8, lines 52-65).

15. With regard to Claim 9, Kelleher discloses a memory controller (68, Figures 7 and 11) coupled to the at least two graphics pipelines (20A, 20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14), operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory (22) (*address generation circuit 68 accepts the initial geometry values from the geometric setup circuit 66, and generates physical memory addresses*, Col. 9, lines 18-23; Col. 10, lines 40-47).

16. With regard to Claim 10, Kelleher discloses that a first of the at least two graphics pipelines (20A, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) processes the pixel data only in a first set of tiles (group 0 of pixel blocks 52) in the repeating tile pattern (*each rendering processor 20 writes to only those pixels that are located in the blocks 52 of the assigned groups, blocks in group "0" may be assigned to rendering processor 0*, Col. 4, line 65-Col. 5, line 19).

17. With regard to Claim 12, Kelleher discloses that a second of the at least two graphics pipelines (20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) processes the pixel data only in a second set of tiles (group 1 of pixel blocks 52) in the repeating tile pattern (*each rendering processor 20 writes to only those pixels that are located in the blocks 52 of the assigned groups, blocks in group "1" may be assigned to rendering processor 1,* Col. 4, line 65-Col. 5, line 19).

18. With regard to Claim 13, Claim 13 is similar in scope to Claim 11, and therefore is rejected under the same rationale.

19. With regard to Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Kelleher discloses four graphics pipelines (20A-20N, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14). Therefore, Claim 14 is rejected under the same rationale as Claims 4 and 10.

20. With regard to Claims 15 and 16, these claims are each similar in scope to Claim 11, and therefore are rejected under the same rationale.

21. With regard to Claim 18, Kelleher discloses a bridge (38, Figure 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (Col. 3, lines 22-23; Col. 4, lines 9-14; *rendering processor 20 first reads the command packets sent to it over the PCI bus 30*, Col. 8, lines 56-65; *rendering processors 20 are connected to a system PCI bus 30A through a PCI bridge 38*, Col. 3, lines 46-50).

22. With regard to Claim 20, Kelleher discloses a graphics processing method (Col. 2, lines 27-28), comprising receiving vertex data for a primitive to be rendered; generating pixel data in response to the vertex data; determining the pixels within a set of tiles (group of pixel blocks 52) of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines (20A, 20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, as shown in Figure 4; and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines (Col. 4, line 60-Col. 5, line 19; Col. 8, lines 56-65).

23. With regard to Claim 21, Kelleher discloses that determining the pixels within a set of tiles (group of pixel blocks 52) of the repeating tile pattern to be processed further comprises

determining the set of tiles that the corresponding graphics pipeline (20, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) is responsible for (Col. 4, line 60-Col. 5, line 19).

24. With regard to Claim 22, Kelleher discloses that the scan converter determines which groups of blocks 52 within the graphics memory 22 are allocated to and controlled by the graphics pipelines 20 (Col. 8, lines 52-61). The graphics memory is partitioned into a plurality of pixel blocks that are tiled in the x-and y-direction of the graphics memory (Col. 4, lines 60-62). Kelleher discloses that determining the pixels within a set of tiles (group of pixel blocks 52) of the repeating tile pattern to be processed (Col. 5, lines 6-19) inherently further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

25. With regard to Claim 23, Kelleher discloses transmitting the processed pixels to memory (22, Figure 4) (*rendering processor 20 scan-converts the object into the graphics memory 22, the graphics memory stores pixel data*, Col. 3, lines 36-41).

26. With regard to Claim 24, Kelleher discloses a graphics processing circuit, comprising front end circuitry (80, 82, Figure 7) operative to generate pixel data in response to primitive data for a primitive to be rendered; first back end circuitry (84), coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates; a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end

circuitry (Col. 3, lines 22-23; Col. 8, line 59-Col. 9, line 23), the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, as shown in Figure 4 (Col. 4, line 60-Col. 5, line 19), and operative to provide the position coordinates to the first back end circuitry in response to the pixel data (Col. 4, lines 60-62; Col. 8, lines 52-65; Col. 6, lines 36-38); second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates; a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data (Col. 3, lines 22-23; Col. 8, line 59-Col. 9, line 23; Col. 4, lines 60-62; Col. 8, lines 52-65; Col. 6, lines 36-38); and a memory controller (68, Figures 7 and 11), coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data (Col. 9, lines 18-23; Col. 10, lines 40-47).

27. With regard to Claim 25, Claim 25 is the same as Claim 1, and therefore is rejected under the same rationale.

28. With regard to Claim 26, Kelleher discloses a horizontally and vertically repeating pattern of regions (Col. 4, line 65-Col. 5, line 19) include NxM number of pixels (*each pixel block 52 is 128x128 pixels in size*, Col. 6, lines 2-4).

29. Thus, it reasonably appears that Kelleher describes or discloses every element of Claims 1-5, 7, 9, 10, 12-16, 18, and 20-26 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

32. Claims 6, 8, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelleher (US005794016A) in view of Furtner (US006778177B1).

33. With regard to Claim 6, Kelleher is relied upon for the teachings as discussed above relative to Claim 1.

However, Kelleher does not explicitly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner describes that each tile of the set of tiles further comprises a 16x16 pixel array (Col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Kelleher so that each tile of the set of tiles further comprises a 16x16 pixel array as suggested by Furtner because Furtner suggests that depending on the number of parallel image-rendering pipelines and depending on the memory organization, the optimum tile size and shape can be selected (Col. 11, lines 45-48, 64-65), and therefore it would be obvious to modify the tile size to be 16x16 pixels if that would be the optimum tile size for a particular number of parallel image-rendering pipelines and particular memory organization.

34. With regard to Claim 8, Kelleher does not teach that the at least two graphics pipelines are on multiple chips. However, Furtner describes that the at least two graphics pipelines are on multiple chips (Col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Kelleher so that the at least two graphics pipelines are on multiple chips as suggested by Furtner because Furtner suggests that this makes the system more configurable by being able to easily add more graphics pipelines to increase the performance (Col. 6, lines 29-30, 42-51).

35. With regard to Claim 17, Claim 17 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

36. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelleher (US005794016A) in view of Hamburg (US005905506A).

Kelleher is relied upon for the teachings as discussed above relative to Claim 10. Kelleher discloses that the first of the at least two graphics pipelines (20A, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14) further includes a scan converter (84, Figure 7), coupled to the front end circuitry (80, 82) and the back end circuitry (Col. 8, line 52-Col. 9, line 23). The scan converter determines which groups of blocks 52 within the graphics memory 22 are allocated to and controlled by the graphics pipelines (Col. 8, lines 52-65; Col. 6, lines 26-28). The graphics memory is partitioned into a plurality of pixel blocks that are tiled in the x-and y-direction of the graphics memory (Col. 4, lines 60-62). Therefore, the scan converter is inherently operative to provide memory addresses or position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry.

However, Kelleher does not explicitly teach using tile identification data to indicate which tiles are to be processed. However, Hamburg discloses a pixel identification line for receiving tile identification data indicating which tiles are to be processed (*during pixel modification, the system must write a pixel within at least one tile within image B, the system determines a tile ID at which to write the pixel value*, Col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Kelleher to include using tile identification data to indicate which tiles are to be processed as suggested by Hamburg because Hamburg suggests the

advantage of using tile identification data to easily track the storage locations of the tile pixel data and being able to easily retrieve data for a particular image tile (Col. 1, lines 46-54).

37. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelleher (US005794016A) and Furtner (US006778177B1) in view of Kent (US 20030164830A1).

Kelleher and Furtner are relied upon for the teachings as discussed above relative to Claim 17. Kelleher discloses that the data includes a polygon. Each pixel block 52 is 128x128 pixels in size. This block size has been determined to effectively divide the parallelism of the graphics pipelines 20. Since polygons tend to be particularly small, and 128x128 blocks 52 are relatively large, polygons will not commonly cross block boundaries (Col. 5, line 65-Col. 6, line 12). Furtner describes that the at least two graphics pipelines are on multiple chips (Col. 6, lines 47-51), as discussed in the rejection for Claim 8.

However, Kelleher and Further do not teach creating a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. However, Kent discloses that the graphics pipeline [0006] calculates the bounding box of the primitive and testing this against the VisRect. If the bounding box of the primitive is contained in the other P10's super tile the primitive is discarded at this stage [0129]. A primitive can be a polygon (*independent primitives (triangles or quads),* [0088]). The method used is to calculate the distance from each subpixel sample point in the point's bounding box to the point's center and compare this to the point's radius. Subpixel sample points with a distance greater

than the radius do not contribute to a pixel's coverage. The cost of this is kept low by only allowing small radius points hence the distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within the bounding box [0144]. Since the method calculates the distance from each subpixel sample point in the point's bounding box, this must include all the corners of the bounding box. Therefore, Kent discloses that the data includes a polygon and that the graphics pipeline creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to the graphics pipeline and wherein if the bounding box does not overlap any of the super tiles, then the processing circuit rejects the whole polygon and processes a next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Kelleher and Furtner to include creating a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one as suggested by Kent because Kent suggests the advantage of processing the super tiles one at a time in order to hide the page break costs [0129, 0051].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,794,016 A	08-1998	Kelleher, Brian Michael	345/505
*	B	US-5,905,506 A	05-1999	Hamburg, Mark	345/672
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531	3/1/2006	JH
Above	UPDATED	1/24/07	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	1/24/07	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/29/2007								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								
	24	✓								
	25	✓								
	26	✓								

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed February 9, 2007, Applicants petition for a one month extension of time and submit the following response.

Amendments to the Claims are reflected in the Listing of the Claims, which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile[[,]]; and

a memory controller in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (currently amended) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; [[and]]

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

REMARKS

Claims 1-26 are now pending in the application. Applicants respectfully traverse and request reconsideration.

Claim 25 stands objected to because it is allegedly exactly the same as claim 1 and is therefore a repeated claim. Applicants respectfully point out that claim 1 includes a "repeating pattern of square regions," (emphasis added), but claim 25 claims a "repeating pattern of regions" (without the limitation that those regions be square). Furthermore, Applicants have amended claim 25 to incorporate the limitation of claim 26 into claim 25, as noted below. Therefore, Applicants respectfully request that the objection be withdrawn.

Claims 20-23 stand rejected under 35 U.S.C. § 101 for allegedly being directed to non-statutory subject matter. As an initial matter, Applicants note that claim 23 has been canceled without prejudice, thereby rendering this rejection moot as to claim 23.

With regard to claim 20, the Examiner merely states that the graphics processing method does not yield a "useful, concrete and tangible result." The Examiner merely provides a conclusive statement that the claims allegedly constitute non-statutory subject matter without an explanation as to why the claims allegedly constitute non-statutory subject matter.

Applicants object to this rejection for at least the reason that no explanation has been given as to why the aforementioned claims are non-statutory. Accordingly, a *prima facie* case has not been established. Applicants kindly remind the Office that MPEP §2106(IV)(B) states that "[t]he burden is on the [Examiner] to set forth a prima facie case of unpatentablity." "After the examiner identifies and explains in the record the basis for why a claim is for an abstract idea with no practical application, then the burden shifts to the applicant to either amend the claim or make a showing of why the claim is eligible for patent protection." MPEP §2106(IV)(D).

In addition, the Examiner states that the claimed method fails to yield a useful, concrete, and tangible result. However, according the Federal Circuit, patentable subject matter includes a "process if the claimed invention as a whole is applied in a 'useful' manner." *AT&T Corp. v. Excel Communications, Inc.*, 172 F.3d 1352, 1357 (Fed. Cir. 1999). A proper inquiry requires "an examination of the contested claims to see if the claimed subject matter as a whole is . . . a 'law of nature' or an 'abstract idea,' or if the . . . concept has been reduced to some practical application rendering it 'useful'." *Id.* In addition, MPEP §2106(IV)(C) states that "[I]n evaluating whether a claim meets the requirements of section 101, the claim must be considered as a whole to determine whether it is for a particular application of an abstract idea, natural phenomenon, or law of nature, rather than for an abstract idea, natural phenomenon, or law of nature." Therefore, the claimed invention as a whole should yield a useful, concrete, and tangible result.

Applicants respectfully submit that at least independent claim 20 recites statutory subject matter. The claim includes, for example, processed pixels, which are concrete (e.g., receiving the same input data for the primitive to be rendered will always produce the same processed pixels), useful (e.g., has a practical utility), and has a real world, tangible result. For example, Applicants present a method for performing graphics processing that comprises, among other things, transmitting processed pixels to a memory controller.

For such subject matter to be statutory, the claimed process must be limited to a practical application of the abstract idea or mathematical algorithm in the technological arts. *In re Alappat*, 33 F.3d 1526, 1543 (Fed. Cir. 1994). A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible, and useful result. *AT&T Corp.*, 172 F.3d at 1357. In *AT&T* the claims in question were directed to generating a message record for an

interexchange call between an originating subscriber and a terminating subscriber and adding a primary interexchange carrier (PIC) indicator to the message record. *Id.* at 1354. The court held that "[t]he PIC indicator represents information about the call recipient's PIC, a useful, non-abstract result that facilitates differential billing of long-distance calls made by a . . . subscriber." *Id.* at 1358) Likewise, a machine claim is statutory when the machine, as claimed, produces a concrete, tangible and useful result (as in *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368, 1373 (Fed. Cir. 1998)). However, the analysis is the same regardless of whether the claim is directed to a machine or a process.

In *State Street*, the Federal Circuit reviewed a claim directed to a "data processing system for managing a financial services configuration of a portfolio established as a partnership, each partner being one of a plurality of funds, comprising" a variety of structural components including a "fifth means for processing data regarding aggregate year-end income, expenses, and capital gain or less for the portfolio and each of the funds." *Id.* at 1371-72. The Federal Circuit held that:

> [t]he transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces 'a useful, concrete and tangible result' – a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades. *Id.* at 1373.

Notably, the claim did not require that the tangible result, which was the share price, be claimed or produced. The mere fact that the *State Street* claim required "processing data" regarding expenses etc. was enough to be considered statutory subject matter. Thus, at least according to the Federal Circuit, a claim need not expressly recite a result that is useful, concrete, and tangible in a last step or anywhere else in order to be considered statutory subject matter. The fact that

the claimed process led to or allowed for a recorded, accepted, and/or relied upon result was sufficient to establish compliance with 35 U.S.C. § 101.

While method claims take a different form than a machine claim, the fact that Applicants claim methods and not machines, as presented in *State Street*, has no impact on the present analysis. *See AT&T Corp.*, 172 F.3d at 1357. Consequently, the fact that the *State Street* opinion notes that the claim is directed to a machine has no weight on the instant analysis.

With regard to claim 20, the method for graphics processing requires, among other things, generating pixel data in response to the vertex data and performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines. Similar to the claimed invention in *State Street*, Applicants' claimed subject matter is directed to a method that processes data not just once but twice: generating pixel data in response to the vertex data and performing pixel operations on the pixels. For at least this reason, claim 20 appears to be directed to a practical application of the section 101 judicial exception. Therefore, reconsideration and withdrawal of the rejection of claim 20 is respectfully requested.

Dependent claims 21-22 are believed to also be directed to statutory subject matter for the same or similar reasons as provided above. Therefore, reconsideration and withdrawal of the rejection of claims 21-22 is respectfully requested.

Claims 1-5, 7, 9, 10, 12-16, 18, and 20-26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,794,016 ("Kelleher"). Kelleher is generally directed to a parallel-processor graphics architecture appropriate for multimedia graphics workstations that is scalable to the needs of a user. (Abstract.) As shown in FIG. 3, for example, N separate rendering processors 20 each implement graphics and multimedia algorithms and interface with

the PCI bus 30 and all other components of the system 10. (Col. 3, line 65 – col. 4, line 1.) Each separate processor 20 has its own bus 32 coupled to its own SDRAM chip 42. In other words, graphics memory 22 is composed of a plurality of memory SDRAM chips 42, wherein each SDRAM chip 42 is coupled to at most one processor. As described in col. 4, lines 42-59, among other places, Kelleher teaches that it is beneficial to provide each processor with its own memory chip(s) and own bus to the memory chip(s) improves performance by, among other things, eliminating dependencies among the processors. In contrast, Applicants' claimed subject matter includes "a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory." (Emphasis added.)

Applicants have canceled claim 9 and incorporated the limitations of the originally filed claim 9 into claim 1. As such, Applicants will only address the rejection as to claim 9. Applicants have also canceled claim 8 without prejudice.

The Examiner suggests that Kelleher "discloses a memory controller (68, Figures 7 and 11) coupled to the at least two graphics pipelines (20A, 20B, Figure 3; Col. 3, lines 22-23; Col. 4, lines 9-14), operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory (22) (*address generation circuit 68 accepts the initial geometry values form the geometric setup circuit 66, and generates physical memory addresses*, Col. 9, lines 18-23; Col. 10, lines 40-47)." Applicants respectfully disagree that Kelleher discloses a memory controller coupled to at least two graphics pipelines. Instead, Applicants submit that Kelleher, in fact, shows each processor (e.g., the pipeline of each processor) coupled to only one bus, which couples one processor 20 to one SDRAM 42 or SDRAM set through one memory controller. For example, the Examiner suggests that 68 is a memory controller, but as shown in FIGs. 7 and

11, address generator 68 is inside one processor 20. Kelleher teaches that "the rendering processor 20 provides a video pipeline for multimedia applications" (emphasis added); Kelleher does not teach that each rendering processor 20 contains multiple pipelines. Therefore, since each address generator is within each processor 20, it is clear that each "memory controller" in Kelleher is not coupled to the at least two graphics pipelines. Applicants further point out that FIG. 4, for example, shows that each graphics memory 22 is partitioned into physical memory segments 42, with each memory segment 42 being coupled to a different processor 20 via its own bus 32. (*See also*, col. 4, lines 15-25.)

Thus, Kelleher does not teach "a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory." Therefore, claim 1 is in condition for allowance. The dependent claims add novel and nonobvious subject matter and are therefore also in condition for allowance.

As to claim 20, Applicants have amended the claim to include the step of transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller. Applicants therefore respectfully reassert the relevant remarks made above with respect to claim 1, and therefore respectfully submit that the claim is in condition for allowance. The dependent claims add novel and nonobvious subject matter and are therefore also in condition for allowance.

As to claim 24, Applicants respectfully submit that Kelleher does not disclose the claimed subject matter. For example, the Examiner states that Kelleher discloses a graphics processing circuit "comprising front end circuitry (80, 82, Figure 7) . . .; first back end circuitry (84) . . ." The claimed subject matter, also includes a first scan converter and a second scan converter, both coupled between the front end circuitry and a back end circuitry. Nothing the

Examiner cites, however, nor does Kelleher disclose anywhere else, as best understood, discloses a first and a second scan converter both coupled to the front end circuitry. At best, Kelleher discloses multiple processors 20, each of which may have its own front end circuitry and a scan converter.

The claimed subject matter also includes "a memory controller, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data." Thus, even if the processors did share front end circuitry (which is not disclosed), the processors, and therefore the first and second back end circuitry, do not share a memory controller for the reasons submitted above with respect to claim 1. Therefore, claim 24 is in condition for allowance.

As to claim 25, Applicants have amended the claim to incorporate the limitations of claim 26 into amended claim 25. The Examiner rejected claim 26 alleging that "Kelleher discloses a horizontally and vertically repeating pattern of regions (Col. 4, line 65-Col. 5, line 19) include NxM number of pixels (*each pixel block 52 is 128x128 pixels in size*, Col. 6, lines 2-4)." As the Office Action notes, however, Kelleher teaches that each block is square: 128 pixels by 128 pixels. This is contrary to Applicants' claimed subject matter, which claims a region that include NxM number of pixels. Since Kelleher, as best understood, does not teach any blocks that are not square, claim 25, as amended, is in condition for allowance, and Applicants respectfully request that the rejection be withdrawn.

Claims 6, 8, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelleher in view of U.S. Patent No. 6,778,177 ("Furtner:"). As noted above, Applicants have canceled claim 8 and have amended claim 1, the claim from which claim 6 and 17 ultimately depend, so that it now includes the limitations of claim 9. Thus, this rejection is moot, and

Applicants respectfully resubmit the relevant remarks made above as to claim 1. Therefore, claims 6 and 17 are in condition for allowance.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelleher in view of U.S. Patent No. 5,905,506 ("Hamburg"). As noted above, Applicants have amended claim 1, the claim from which claim 11 ultimately depends, so that it now includes the limitations of claim 9. Thus, this rejection is moot, and Applicants respectfully resubmit the relevant remarks made above as to claim 1. Therefore, claim 11 is in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kelleher and Furtner in view of U.S. Patent Application No. 2003/0164830 ("Kent"). As noted above, Applicants have amended claim 1, the claim from which claim 19 ultimately depends, so that it now includes the limitations of claim 9. Thus, this rejection is moot, and Applicants respectfully resubmit the relevant remarks made above as to claim 1. Therefore, claim 19 is in condition for allowance.

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this response is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (312) 609-7599.

Respectfully submitted,

Date: 6/13/07

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	120	120

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**120**

Electronic Acknowledgement Receipt

EFS ID:	1849378
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	07-JUN-2007
Filing Date:	12-JUN-2003
Time Stamp:	14:59:56
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$120
RAM confirmation Number	234
Deposit Account	220259
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	10459797_Extension.pdf	708795	no	1
Warnings:					
Information:					
2		10459797_Response.pdf	7382196	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment - After Non-Final Rejection	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	16

Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8190	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	8099181		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (12-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) FY 2005 *(Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).)*	Docket Number (Optional) 00100.02.0053
Application Number 10/459,797	Filed June 12, 2003
For DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE	
Art Unit 2628	Examiner Joni Hsu

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$120	$60	$ 120.00
☐ Two months (37 CFR 1.17(a)(2))	$450	$225	$
☐ Three months (37 CFR 1.17(a)(3))	$1020	$510	$
☐ Four months (37 CFR 1.17(a)(4))	$1590	$795	$
☐ Five months (37 CFR 1.17(a)(5))	$2160	$1080	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 22-0259. I have enclosed a duplicate copy of this sheet.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

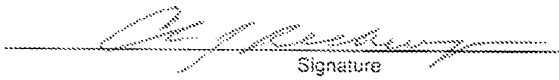
I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration Number 34,414

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____



Signature — June 7, 2007 (Date)

Christopher J. Reckamp (Typed or printed name) — 312-609-7599 (Telephone Number)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☑ Total of 1 forms are submitted.

BEST AVAILABLE COPY

PATENT APPLICATION FEE DETERMINATION RECORD
Effective January 1, 2003

Application or Docket Number: 10459797

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
TOTAL CLAIMS	29	
FOR		
TOTAL CHARGEABLE CLAIMS	24 minus 20=	* 4
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐			OTHER THAN SMALL ENTITY	
RATE	FEE	OR	RATE	FEE
BASIC FEE	375.00	OR	BASIC FEE	750.00
X$ 9=		OR	X$18=	72
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

1-5-06

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 25	Minus	** 6	=
Independent	* 4	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

6/13/06

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 24	Minus	** 20	= 4
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

6/7/07

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 29	Minus	** 24	= 5
Independent	* 4	Minus	*** 4	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY			OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Atty. Docket No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT IN ACCORDANCE WITH 37 CFR §§ 1.97(c) AND 1.98

Pursuant to 37 CFR §§ 1.97(c) and 1.98, Applicants respectfully submit the following statement consisting of:

1. A list of documents; and

2. General remarks.

Enclosed herewith is Forms PTO/SB/08A and PTO/SB/08B.

1. Document

   a. U.S. Patent No. 6,292,200 B1 issued September 18, 2001 to Bowen et al.;

   b. U.S. Patent No. 6,697,063 issued February 24, 2004 to Zhu;

   c. U.S. Patent No. 6,791,559 B2 issued September 14, 2004 to Baldwin;

   d. U.S. Patent No. 7,170,515 B1 issued January 30, 2007 to Zhu;

   e. U.S. Publication No. 2002/0145612 A1 published October 10, 2002 to Blythe et al. and

   f. AKELEY, K. et al.; High-Performance Polygon Rendering; ACM Computer Graphics; Vol. 22, No. 4; 1988; pages 239-246.

REMARKS

The submission of the listed documents are not an admission that the information is prior art, analogous or otherwise material. It is respectfully requested that the listed documents be considered and made of record in the present application.

The Patent Office is hereby authorized to charge the fee of $180.00 set forth in 37 CFR 1.17(p) to Deposit Account No. 50-0441 and is authorized to charge any additional fees required or credit any overpayments to this account.

Respectfully submitted,

Date: 7-26-07

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,292,200 B1	09-18-2001	Bowen et al.	
		US- 6,697,063	02-24-2004	Zhu	
		US- 6,791,559 B2	09-14-2004	Baldwin	
		US- 7,170,515 B1	01-30-2007	Zhu	
		US- 2002/0145612 A1	10-10-2002	Blythe et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		AKELEY, K. et al.; High-Performance Polygon Rendering; ACM Computer Graphics; Vol. 22, No. 4; 1988; pages 239-246.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	2017888
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	27-JUL-2007
Filing Date:	12-JUN-2003
Time Stamp:	10:13:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$180
RAM confirmation Number	4050
Deposit Account	500441
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	10459797_IDS.pdf	2140392 7e80789ab1a9680d291166d68bd54be6d0d65ee3	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	NPL Documents	10459797_NPL.pdf	965625 e03b4efa157930a95f28dc5198650e0342495a13	no	9
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8214 4cbf82665a89c4d8907894df2c684d197661e78f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3114231		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S55	431	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S56	341	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S57	336	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S58	51	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S59	109	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S60	533	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S61	86	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S62	849	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36

EAST Search History

S63	419	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S64	689	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S65	1796	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S66	1453	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:36
S67	171	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:37
S68	131	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:37
S69	268	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:37
S70	268	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:52

EAST Search History

S71	372	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:53
S72	111	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:53
S73	103	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:53
S74	45	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/08/09 12:54

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 08/28/2007

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 7, 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on July 27, 2007 was filed after the mailing date of the application on June 12, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see pages 8-11, filed June 7, 2007, with respect to the claim objection and the 35 U.S.C. 101 rejections have been fully considered and are persuasive. The objection to Claim 25 and the 35 U.S.C. 101 rejections of Claims 20-22 have been withdrawn.

3. Applicant's arguments with respect to claims 1-7, 10-22, 24, and 25 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's arguments, see pages 12-13, filed June 7, 2007, with respect to the rejection(s) of claim(s) 1-5, 7, 10, 12-16, 18, 20-22, 24, and 25 under 35 U.S.C. 102(b) and claims 6, 11, 17, and 19 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Perego (US006864896B2).

5. Applicant argues that Kelleher (US005794016A) does not teach "a memory controller coupled to the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory" (pages 12-13).

In reply, new grounds of rejection are made in view of Perego.

6. As per Claim 25, Applicant argues that Kelleher teaches that each block is square. Since Kelleher does not teach any blocks that are not square, and therefore does not teach a region that includes NxM number of pixels (page 14).

In reply, the Examiner points out that Claim 25 does not recite that N is not equal to M. Therefore, N can be equal to M. New grounds of rejection are made in view of Perego, which more clearly teaches Applicant's disclosed invention. Even if N does not equal to M, Perego teaches that each region is rectangular (c. 5, ll. 23-25).

7. Applicant's arguments filed June 7, 2007 with respect to Claim 24 have been fully considered but they are not persuasive.

8. As per Claim 24, Applicant argues that Kelleher discloses multiple processors 20, each of which may have its own front end circuitry and a scan converter. Kelleher does not disclose a first and a second scan converter both coupled to the front end circuitry (pages 13-14).

In reply, Examiner disagrees. Kelleher teaches first and second scan converter (update stage, Fig. 7 in 20A and 20B, Fig. 3) both coupled to front end circuitry 14 (c.8, ll. 32-c. 9, ll. 4).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-4, 7, 10, 12, 14, 20-22, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Perego (US006864896B2).

11. As per Claims 1 and 25, Perego teaches graphics processing circuit (300, Fig. 3; Col. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least two graphics pipelines (312), operative to transfer pixel data between each of first pipeline and second pipeline and shared memories (314) (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). The shared memories (314) are each part of the main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and therefore are considered to be one memory. The repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

12. As per Claim 2, Perego discloses that the square regions comprise a two dimensional partitioning of memory (c. 5, ll. 19-33).

13. As per Claim 3, Perego discloses that the memory is a frame buffer (c. 5, ll. 32-33).

14. As per Claim 4, Perego discloses that each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process a portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for the front end circuitry (308) to generate pixel data, it must inherently receive vertex data.

15. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive the pixel data from the front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

16. As per Claim 10, Perego discloses that a first of the at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes the pixel data only in a first set of tiles (tiles labeled "RE0" in Fig. 5) in the repeating tile pattern (c. 5, ll. 23-44).

17. As per Claim 12, Perego discloses that a second of the at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes the pixel data only in a second set of tiles (tiles labeled "RE1" in Fig. 5) in the repeating tile pattern (c. 5, ll. 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5,.ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 20, Perego teaches a graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines (312, Fig. 3) in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines (c. 5, ll. 19-44); and transmitting the processed pixels to a memory controller (310), wherein the at least two graphics pipelines share the memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44).

20. As per Claim 21, Perego discloses that determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

21. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least two graphics pipelines (c. 5, ll. 19-44).

Thus, it reasonably appears that Perego describes or discloses every element of Claims 1-4, 7, 10, 12, 14, 20-22, and 25 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

22. The text of those sections of Title 35, U.S. Code 103(a) not included in this action can be found in a prior Office action.

23. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Kelleher (US005794016A).

24. As per Claim 5, Perego is relied upon for the teachings as discussed relative to Claim 4.

However, Perego does not explicitly teach that at each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry. However, Kelleher discloses that each of the at least two graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes a scan converter (update stage, Fig. 7), coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that at each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry as suggested by Kelleher

because Kelleher suggests that the scan converters are needed in order to define the image data as an array of pixels by calculating the pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

25. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Kelleher discloses a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Kelleher because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

26. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); first back end circuitry (first rendering engine 312), coupled to front end circuitry 308, operative to process first portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by first back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; second back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process second portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by second back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44);

and memory controller (310), coupled to first and second back end circuitry (312) operative to transmit and receive processed pixel data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44).

However, Perego does not explicitly teach a first scan converter and a second scan converter. However, Kelleher discloses a first scan converter, coupled between the front end circuitry (14, Fig. 3) and the first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide the position coordinates to the first back end circuitry in response to the pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); a second scan converter, coupled between the front end circuitry and the second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for the same reasons given in the rejection for Claim 5.

27. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

28. As per Claim 6, Perego is relied upon for the teachings as discussed relative to Claim 1.

However, Perego does not explicitly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner describes that each tile of the set of tiles further comprises a 16x16 pixel array (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that each tile of the set of tiles further comprises a

16x16 pixel array as suggested by Furtner because Furtner suggests that depending on the number of parallel image-rendering pipelines and depending on the memory organization, the optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and therefore it would be obvious to modify the tile size to be 16x16 pixels if that would be the optimum tile size for a particular number of parallel image-rendering pipelines and particular memory organization.

29. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Perego so that pipelines are on separate chips as suggested by Furtner because Furtner suggests that this makes the system more configurable by being able to easily add more graphics pipelines to increase the performance (c. 6, ll. 29-30, 42-51).

30. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego is relied upon for the teachings as discussed relative to Claim 10.

However, Perego does not explicitly teach a scan converter. However, Kelleher discloses that the first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes a scan converter (84, Fig. 7), coupled to the front end circuitry (80, 82) and the back end circuitry (c. 8, ll. 52-c. 9, ll. 23). The scan converter determines which groups of blocks 52 within the graphics memory 22 are allocated to and controlled by the graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). The graphics memory is partitioned into a plurality of pixel blocks that are tiled in the x-and y-direction of the graphics memory (c. 4, ll. 60-62).

Therefore, the scan converter is inherently operative to provide memory addresses or position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not explicitly teach using tile identification data to indicate which tiles are to be processed. However, Hamburg discloses a pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Perego and Kelleher to include using tile identification data to indicate which tiles are to be processed as suggested by Hamburg because Hamburg suggests the advantage of using tile identification data to easily track the storage locations of the tile pixel data and being able to easily retrieve data for a particular image tile (c. 1, ll. 46-54).

31. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) and Furtner (US006778177B1) in view of Kent (US 20030164830A1).

Perego and Furtner are relied upon for the teachings discussed relative to Claim 17. Perego teaches data includes a polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed in the rejection for Claim 17.

However, Perego and Further do not teach creating a bounding box around the polygon and each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. However, Kent discloses that the graphics pipeline [0006] calculates the bounding box of the primitive and testing this against the VisRect. If the bounding box of the primitive is contained

in the other P10's super tile the primitive is discarded at this stage [0129]. A primitive can be a polygon [0088]. The method used is to calculate the distance from each subpixel sample point in the point's bounding box to the point's center and compare this to the point's radius. Subpixel sample points with a distance greater than the radius do not contribute to a pixel's coverage. The cost of this is kept low by only allowing small radius points hence the distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within the bounding box [0144]. Since the method calculates the distance from each subpixel sample point in the point's bounding box, this must include all the corners of the bounding box. Therefore, Kent discloses that the data includes a polygon and that the graphics pipeline creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to the graphics pipeline and wherein if the bounding box does not overlap any of the super tiles, then the processing circuit rejects the whole polygon and processes a next one. .

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Perego and Furtner to include a bounding box as suggested by Kent because Kent suggests the advantage of processing the super tiles one at a time in order to hide the page break costs [0129, 0051].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.H./		US- 6,292,200 B1	09-18-2001	Bowen et al.	
/J.H./		US- 6,697,063	02-24-2004	Zhu	
/J.H./		US- 6,791,559 B2	09-14-2004	Baldwin	
/J.H./		US- 7,170,515 B1	01-30-2007	Zhu	
/J.H./		US- 2002/0145612 A1	10-10-2002	Blythe et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	08/09/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.H./		AKELEY, K. et al.: High-Performance Polygon Rendering; ACM Computer Graphics; Vol. 22, No. 4; 1988; pages 239-246.	

Examiner Signature	/Joni Hsu/	Date Considered	08/09/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,864,896	03-2005	Perego, Richard E.	345/542
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/09/2007								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	-								
	9	-								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	-								
	24	✓								
	25	✓								
	26	-								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED

Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531	1/24/07	JH
Above	UPDATED	8/9/07	JH

SEARCH NOTES

Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	8/9/07	JH

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed August 28, 2007, Applicants respond as follows.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] This is a related application to a co-pending application entitled "Parallel Pipeline Graphics System" ~~having docket number 010025~~, having serial number 10/724,384, having Leather et al. as the inventors, filed on ~~even date~~ November 26, 2003, owned by the same assignee and hereby incorporated by reference in its entirety.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (original) The graphics processing circuit of claim 4, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (currently amended) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (currently amended) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 7, 10, 12, 14, 20-22 and 25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,864,896 (Perego). This is a new ground of rejection. Perego is directed to a scalable unified memory architecture and describes a "system…that provides multiple discrete memory modules coupled to a common memory controller. Each memory module includes a computing engine and a shared memory. A data processing task from the memory controller can be partitioned among the different computing engines to allow parallel processing of the various portions of the processing task." (Column 7, lines 35-42) (emphasis added). As such, Perego is directed to a system that employs separate and discrete memory modules wherein each memory module includes a computing engine and corresponding shared system memory and graphics memory.

In contrast, the amended independent claims require a multi-graphics pipeline circuit on a same chip that is operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to a screen location. In addition, a memory controller on the chip is in communication with the at least two graphics pipelines on the same chip to transfer pixel data between each of the first pipeline and the second pipeline in the memory. (See for example, claim 1).

Perego describes a different system. For example, Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory and shared main memory. Such multiple memory modules require multiple chips and packages taking up additional space and requiring additional signaling and synchronization operations and can be more acceptable to electromagnetic interference. In addition, a separate memory controller is described as being a part of a different and separate memory controller subsystem/CPU 302 that

is coupled "to four distinct memory modules 304". (See column 4, lines 26-36). Perego further describes that the memory controller/graphics controller is responsible for distributing particular processing tasks to the different rendering engines on different discrete memory modules.

Perego does not describe multi-graphics pipeline circuitry on a same chip nor a memory controller on the same chip but instead describes discrete memory modules having separate and single graphics engines thereon. In addition, the memory controller described in Perego is not on a same chip nor is it part of the memory module as described in Perego. As such, the Perego reference does not anticipate Applicants' claimed subject matter. Other differences will be recognized by those of ordinary skill in the art.

The dependent claims add additional novel and non-obvious subject matter. For example as to claim 4, the claim requires that each of the two graphics pipelines on a same chip include front end circuitry that receives vertex data and generates pixel data corresponding to a primitive to be rendered. The office action cites the CPU 308 as being the front end circuitry in Perego. However as claimed, the multiple graphics pipelines on the same chip include the front end circuitry, and not a separate CPU that passes information through a graphics controller as taught in Perego. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance. The other dependent claims add additional novel and non-obvious subject matter.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of Kelleher. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference

illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of Furtner. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of Kelleher, further in view of Hamburg. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego and Furtner in view of Kent. Applicants respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: November 28, 2007

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,980,209 B1	12-27-2005	Donham et al.	
		US- 5,550,962	08-27-1996	Nakamura et al.	
		US- 5,818,469	10-06-1998	Lawless et al.	
		US- 6,118,452	09-12-200	Gannett	
		US- 6,353,439 B1	03-05-2002	Lindholm et al.	
		US- 6,384,824 B1	05-07-2002	Morgan et al.	
		US- 6,417,858 B1	07-09-2002	Bosch et al.	
		US- 6,573,893 B1	06-03-2003	Naqvi et al.	
		US- 6,650,327 B1	11-18-2003	Airey et al.	
		US- 6,650,330 B2	11-18-2003	Lindholm et al.	
		US- 6,724,394 B1	04-20-2004	Zatz et al.	
		US- 6,731,289 B1	05-04-2004	Peercy et al.	
		US- 6,809,732 B2	10-26-2004	Zatz et al.	
		US- 6,864,893 B2	03-08-2005	Zatz	
		US- 6,897,871 B1	05-24-2005	Morein et al.	
		US- 7,015,913 B1	03-21-2006	Lindholm et al.	
		US- 2003/0076320 A1	04-24-2003	Collodi	
		US- 2005/0200629 A1	09-15-2005	Morein et al.	
		US- 2004/0041814 A1	03-04-2004	Wyatt et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,222,550 B1	04-2001	Rosman et al.	
		US- 6,557,083 B1	04-2003	Sperber et al.	
		US- 6,219,062 B1	04-2001	Matsuo et al.	
		US- 5,977,997	11-1999	Vainsencher	
		US- 6,323,860	11-27-2001	Zhu et al.	
		US- 6,344,852	02-05-2002	Zhu et al.	
		US- 6,380,935	04-30-2002	Heeschen et al.	
		US- 6,636,232	10-21-2003	Larson	
		US- 6,801,203	10-05-2004	Hussain	
		US- 7,061,495	06-13-2006	Leather	
		US- 2004/0164987 A1	08-26-2004	Aronson et al.	
		US- 2005/0068325 A1	03-31-2005	Lefebvre et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		BRETERNITZ, JR., MAURICIO et al.; Compilation, Architectural Support, and Evaluation of SIMD Graphics Pipeline Programs on a General-Purpose CPU; IEEE; 2003; pages 1-11.	
		International Search Report for PCT Patent Application PCT/IB2004/003821 dated March 22, 2005.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	2517147
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	28-NOV-2007
Filing Date:	12-JUN-2003
Time Stamp:	11:03:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	5972
Deposit Account	500441
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		10459797_Response.pdf	116059 bc3b199cec689cdd459beda5278d11e059b9451a	yes	11

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment - After Non-Final Rejection	1	1
Specification	2	2
Claims	3	8
Applicant Arguments/Remarks Made in an Amendment	9	11

Warnings:

Information:

2	Information Disclosure Statement Letter	10459797_IDSCover.pdf	78801 e56cc2fdd0aca332a5caaac70a654a2a75138112	no	1

Warnings:

Information:

3	Information Disclosure Statement (IDS) Filed	10459797_IDS.pdf	207593 c2500b953bf655ac19241119bdccaa9a47257b92	no	3

Warnings:

Information:

This is not an USPTO supplied IDS fillable form

4	NPL Documents	10459797_Ref1.pdf	1640558 5087811be5b9f94284b8a3e57ab47316e047ce47	no	11

Warnings:

Information:

5	NPL Documents	10459797_Ref2.pdf	796566 b156b1e21ab3c7695393bab79ee6cb67e24b25ec	no	15

Warnings:

Information:

6	Fee Worksheet (PTO-06)	fee-info.pdf	8214 68dae946b762f40f6c3961372da051fbdbe2b916	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2847791	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148
Examiner: Joni Hsu
Art Unit: 2628
Atty. Docket No.: 00100.02.0053
Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT IN ACCORDANCE WITH 37 CFR §§ 1.97(c) AND 1.98

Pursuant to 37 CFR §§ 1.97(c) and 1.98, Applicants respectfully submit forms PTO/SB/08A and PTO/SB/08B.

REMARKS

The submission of the listed documents are not an admission that the information is prior art, analogous or otherwise material. It is respectfully requested that the listed documents be considered and made of record in the present application.

The Patent Office is hereby authorized to charge the fee of $180.00 set forth in 37 CFR 1.17(p) to Deposit Account No. 50-0441 and is authorized to charge any additional fees required or credit any overpayments to this account.

Respectfully submitted,

Date: November 28, 2007

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
Phone: (312) 609-7599
Fax: (312) 609-5005

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	542	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L2	360	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L3	116	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L4	89	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L5	873	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L6	434	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L7	55	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L8	700	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44

EAST Search History

L9	443	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L10	1883	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L11	1529	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L12	340	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L13	278	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L14	173	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L15	132	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L16	278	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44

EAST Search History

L17	389	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L18	118	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L19	105	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:44
L20	45	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:46
L21	305	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:46
L25	45	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:48
L27	107	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/07 14:49

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 02/04/2008
ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
02/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/28/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Information disclosure statement (IDS) submitted on November 28, 2007 was filed after mailing date of application on June 12, 2003. Submission is in compliance with provisions of 37 CFR 1.97. Accordingly, information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments, see pages 9-11, filed November 28, 2007, with respect to the rejection(s) of claim(s) 1-4, 7, 10, 12, 14, 20-22, and 25 under 35 U.S.C. 102(e) and claims 5, 6, 11, 13, 15-19, and 24 under 35 U.S.C. 103(a) have been fully considered and are persuasive. So, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Furtner (US006778177B1) and MacInnis (US006570579B1).

3. Applicant argues Perego (US006864896B2) does not teach multi-graphics pipeline circuitry on same chip nor memory controller on the same chip but instead teaches discrete memory modules having separate and single graphics engines thereon. The memory controller taught in Perego is not on a same chip nor is it part of the memory module (page 10).

In reply, new grounds of rejection are made in view of Furtner and MacInnis.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1).

6. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines (312), operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories (314) (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). Shared memories (314) are each part of main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches that the graphics pipelines are on a same chip (c. 6, ll. 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (c. 4, ll. 65-67; c. 5, ll. 36-41; c. 6, ll. 10-13). This would be obvious for same reasons given above.

7. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (c. 5, ll. 19-33).

8. As per Claim 3, Perego discloses that the memory is a frame buffer (c. 5, ll. 32-33).

9. As per Claim 4, Perego teaches each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for front end circuitry (308) to generate pixel data, it must inherently receive vertex data.

10. As per Claim 6, Perego does not explicitly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches each tile of set of tiles has 16x16 pixel array (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and

so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

11. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive the pixel data from the front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

12. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

13. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

14. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5, ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

15. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (c. 6, ll. 29-30, 42-51).

16. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A).

17. As per Claim 5, Perego, Furtner, and MacInnis are relied upon for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of at least two graphics pipelines further includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least two graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, and MacInnis so at each of at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

18. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines. However, Kelleher discloses a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines as suggested by Kelleher because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

19. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); first back end circuitry (first rendering engine 312), coupled to front end circuitry 308, operative to process first portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by first back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; second back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process second portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by second back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44); and memory controller (310), coupled to first and second back end circuitry (312) operative to transmit and receive processed pixel data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end

circuitry in response to pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same chip (c. 6, ll. 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed in the rejection for Claim 1.

20. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (c. 8, ll. 52-c. 9, ll. 23). Scan converter determines which groups of blocks

52 within graphics memory 22 are allocated to and controlled by graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (c. 4, ll. 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for reasons for Claim 5.

But, Perego, Furtner, MacInnis, Kelleher do not explicitly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (c. 1, ll. 46-54).

21. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then

processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

22. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

23. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of at least two graphics pipelines (312, Fig. 3) in response to

pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (c. 5, ll. 19-44); and transmitting processed pixels to memory controller (310), wherein at least two graphics pipelines share memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches graphics pipelines are on a same chip (c. 6, ll. 30-32), as discussed for Claim 1.

24. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

25. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least two graphics pipelines (c. 5, ll. 19-44).

26. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44).

However, Perego does not teach that the graphics pipelines are on a same chip. However, Furtner teaches graphics pipelines are on a same chip (c. 6, ll. 30-32), as discussed for Claim 1.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP §.706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

KEE M. TUNG
SUPERVISORY PATENT EXAMINER

Notice of References Cited	Application/Control No. 10/459,797	Applicant(s)/Patent Under Reexamination LEATHER ET AL.	
	Examiner Joni Hsu	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,570,579	05-2003	MacInnis et al.	345/629
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.H./		US- 6,980,209 B1	12-27-2005	Donham et al.	
/J.H./		US- 5,550,962	08-27-1996	Nakamura et al.	
/J.H./		US- 5,818,469	10-06-1998	Lawless et al.	
/J.H./		US- 6,118,452	09-12-200	Gannett	
/J.H./		US- 6,353,439 B1	03-05-2002	Lindholm et al.	
/J.H./		US- 6,384,824 B1	05-07-2002	Morgan et al.	
/J.H./		US- 6,417,858 B1	07-09-2002	Bosch et al.	
/J.H./		US- 6,573,893 B1	06-03-2003	Naqvi et al.	
/J.H./		US- 6,650,327 B1	11-18-2003	Airey et al.	
/J.H./		US- 6,650,330 B2	11-18-2003	Lindholm et al.	
/J.H./		US- 6,724,394 B1	04-20-2004	Zatz et al.	
/J.H./		US- 6,731,289 B1	05-04-2004	Peercy et al.	
/J.H./		US- 6,809,732 B2	10-26-2004	Zatz et al.	
/J.H./		US- 6,864,893 B2	03-08-2005	Zatz	
/J.H./		US- 6,897,871 B1	05-24-2005	Morein et al.	
/J.H./		US- 7,015,913 B1	03-21-2006	Lindholm et al.	
/J.H./		US- 2003/0076320 A1	04-24-2003	Collodi	
/J.H./		US- 2005/0200629 A1	09-15-2005	Morein et al.	
/J.H./		US- 2004/0041814 A1	03-04-2004	Wyatt et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.H./		US- 6,222,550 B1	04-2001	Rosman et al.	
/J.H./		US- 6,557,083 B1	04-2003	Sperber et al.	
/J.H./		US- 6,219,062 B1	04-2001	Matsuo et al.	
/J.H./		US- 5,977,997	11-1999	Vainsencher	
/J.H./		US- 6,323,860	11-27-2001	Zhu et al.	
/J.H./		US- 6,344,852	02-05-2002	Zhu et al.	
/J.H./		US- 6,380,935	04-30-2002	Heeschen et al.	
/J.H./		US- 6,636,232	10-21-2003	Larson	
/J.H./		US- 6,801,203	10-05-2004	Hussain	
/J.H./		US- 7,061,495	06-13-2006	Leather	
/J.H./		US- 2004/0164987 A1	08-26-2004	Aronson et al.	
/J.H./		US- 2005/0068325 A1	03-31-2005	Lefebvre et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 3

	Complete if Known
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.H./		BRETERNITZ, JR., MAURICIO et al.; Compilation, Architectural Support, and Evaluation of SIMD Graphics Pipeline Programs on a General-Purpose CPU; IEEE; 2003; pages 1-11.	
/J.H./		International Search Report for PCT Patent Application PCT/IB2004/003821 dated March 22, 2005.	

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/07/2007								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	-								
	9	-								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	-								
	24	✓								
	25	✓								
	26	-								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED

Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531	8/9/07	JH
Above	UPDATED	12/7/07	JH
345	519	12/7/07	JH

SEARCH NOTES

Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	12/7/07	JH

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

PTO/SB/30 (04-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 22-0259. I have enclosed a duplicate copy of this sheet.

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☑ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☐ Check in the amount of $ _____ enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	July 3, 2008
Name (Print/Type)	Christopher J. Reckamp	Registration No.	34,414

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being forwarded via electronic submission to: Electronic Business Center, Commissioner for Patents, Mail Stop RCE, on the date shown below.

Signature			
Name (Print/Type)	Christine A. Wright	Date	July 3, 2008

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

In response to the Final Office Action mailed February 4, 2008, Applicants submit a Request for Continued Examination, petition for a two month extension of time and submit the following preliminary amendment.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (currently amended) The graphics processing circuit of claim [[4]]7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (previously presented) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 6, 7, 10, 12, 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of U.S. Patent No. 6,570,579 (MacInnis). Applicants wish to thank the Examiner for reconsideration in view of the prior remarks. As a result, this is a new ground of rejection. Applicants respectfully traverse however based on the actual teachings of the references since the alleged combination would actually result in the inoperability of the primary Perego reference. Combining teachings that render the operation of a reference inoperable is not a prima facia case of obviousness. As such, Applicants respectfully submit that the claims are in condition for allowance.

For example, Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory and shared main memory. Perego teaches an opposite approach from that claimed by Applicants. Perego requires interconnecting modules that can allow variable scalability in addition to requiring shared memory controllers. In addition, a separate memory controller is described as being a part of a different and separate memory controller subsystem/CPU 302 that is coupled "to four distinct memory modules 304". (See column 4, lines 26-36). Perego further describes that the memory controller/graphics controller is responsible for distributing particular processing tasks to the different rendering engines on different discrete memory modules.

It is alleged however that placing a plurality of modules on a single chip is taught in Furtner, and modifying Perego accordingly would be proper. However, Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory. Placing rendering engines 312 onto a single chip would require redesign of the memory graphics controller and CPU memory subsystem as well as each individual module of Perego. Applicants

respectfully submit that the alleged motivation, namely that placing a plurality of modules on a single chip takes up less space is not applicable in this instance as to Perego since it would render the Perego system inoperable for its intended purpose since Perego teaches a scalable module system and unified memory architecture with a memory controller coupled to multiple modules (see Abstract). Perego teaches an opposite approach from that claimed by Applicants where interconnecting modules can allow variable scalability in addition to requiring shared memory controllers. As such, the motivation does not appear to be applicable to the teachings of Perego. In fact, modifying Perego as suggested would render Perego inoperable for its intended purpose. For these reasons alone, the claims are in condition for allowance.

Moreover, not only does Furtner fail to teach the claimed subject matter, but the office action also attempts to combine the teachings of MacInnis as a further level of consolidation. However, Applicants respectfully submit that again the teachings of the references cannot be ignored. As noted above, the combination of Perego, MacInnis and Furtner would change the operation of Perego to the point where it would be inoperable for its intended purpose. As such, further combination would further render the Perego operation unusable for its intended purposes. Accordingly, Applicants respectfully request reconsideration and respectfully submit that the claims are in condition for allowance.

Applicants respectfully reassert the relevant remarks made above with respect to the independent claims and as such, the independent claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, as to claim 4, the claim requires that each of the two graphics pipelines on a same chip include front end circuitry that receives vertex data and generates pixel data corresponding to a primitive to be rendered. The office action cites the CPU 308 as being the front end circuitry in

Perego. However as claimed, the multiple graphics pipelines on the same chip include the front end circuitry, and not a separate CPU that passes information through a graphics controller as taught in Perego. Accordingly, Applicants respectfully submit that this claim is also in condition for allowance. The other dependent claims add additional novel and non-obvious subject matter.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Perego in view of Kelleher. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, Furtner, and MacInnis in view of Kelleher, further in view of Hamburg. A fourth reference has been added in an attempt to render these claims obvious. Applicants respectfully reassert the remarks made above with respect to the Perego, Further and MacInnis references and as such, these claims are also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, Furtner, and MacInnis in view of Kent. Applicants respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 20-22 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner. Applicants respectfully reassert the remarks made above with respect to Perego and Furtner and as such, these claims are also in condition for allowance.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: July 3, 2008

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 2 months with $0 paid	1252	1	460	460

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**1270**

Electronic Acknowledgement Receipt

EFS ID:	3563474
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	03-JUL-2008
Filing Date:	12-JUN-2003
Time Stamp:	11:52:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1270
RAM confirmation Number	8524
Deposit Account	220259
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	10459797_RCE.pdf	80172 5fa39899ec6684b5c885ed7d753b7cc18a6fa8f3	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2		10459797_PrelAmdt.pdf	112437 c9c1d74a30b9a2bb32af8c2b140a319a720e7bd6	yes	11

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	11

Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8352 ae06602d6b443b30f386312664b07ec9386b718b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	200961		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/03/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/THERESA LINDSAY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 08/25/2008

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
08/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 3, 2008 has been entered.

Response to Arguments

2. Applicant's arguments filed July 3, 2008 have been fully considered but they are not persuasive.

3. Applicant argues that the alleged motivation for modifying Perego (US006864896B2) with Furtner's (US006778177B1) teaching of placing a plurality of modules on a single chip, namely that placing a plurality of modules on a single chip takes up less space is not applicable in this instance as to Perego since it would render the Perego system inoperable for its intended purpose since Perego teaches a scalable module system and unified memory architecture with a memory controller coupled to multiple modules (p. 8-9).

In reply, the Examiner disagrees. Perego actually describes that it is advantageous to integrate a plurality of subsystems into a single integrated circuit. Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39). Since Perego describes that it is advantageous to integrate a plurality of

subsystems into a single integrated circuit, implementing the teaching of placing the plurality of graphics pipelines on a single chip as taught by Furtner (col. 6, lines 30-32) into the Perego system would not render the Perego system inoperable for its intended purpose.

4. Applicant argues combination of Perego, MacInnis (US006570579B1) and Furtner would change operation of Perego to point where it would be inoperable for its intended purpose (p. 9).

In reply, Examiner disagrees. MacInnis is used for its teaching of having memory controller on same chip as graphics pipeline (col. 4, lines 65-67; col. 5, lines 36-41; col. 6, lines 10-13). Perego teaches it is advantageous to integrate a plurality of subsystems into a single integrated circuit (col. 1, lines 34-39), as discussed above. Perego also goes on to describe "As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 39-43). So, implementing the teaching of having memory controller on same chip as a graphics pipeline as taught by MacInnis into the Perego system would not render the Perego system inoperable for its intended purpose.

5. As per Claim 4, Applicant argues that as claimed, the multiple graphics pipelines on the same chip include the front end circuitry, and not a separate CPU that passes information through a graphics controller as taught in Perego (p. 9-10).

In reply, Examiner points out that Claim 4 does not recite that multiple graphics pipelines are on same chip, and that is why this limitation is not addressed in rejection for Claim 4. This limitation is addressed in the rejection for Claim 1, and Furtner is used to teach this limitation.

6. As per Claim 24, Applicant argues Perego does not teach multiple backend circuitry on common chip nor common front end circuitry and memory controller on common chip (p. 10).

In reply, Examiner points out Furtner and MacInnis are used to teach these limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1).

10. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in dedicated tile (col. 5, lines 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines (312), operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories (314) (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories (314) are each part of main

memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43).

However, Perego does not expressly teach graphics pipelines (312) are on a same chip. However, Furtner teaches that the graphics pipelines are on a same chip (col. 6, lines 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (col. 4, lines 65-67; col. 5, lines 36-41; col. 6, lines 10-13). This would be obvious for same reasons given above.

11. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (col. 5, lines 19-33).

12. As per Claim 3, Perego discloses that the memory is a frame buffer (col. 5, lines 32-33).

13. As per Claim 4, Perego teaches each of at least two graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data.

14. As per Claim 6, Perego does not expressly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches this limitation (col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (col. 11, lines 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

15. As per Claim 7, Perego teaches the at least two graphics pipelines (312, Fig. 3) separately receive pixel data from front end circuitry (308) (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44).

16. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44).

17. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (col. 5, lines 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches 3rd and 4th pipelines are on separate chips (col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (col. 6, lines 29-30, 42-51).

20. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kelleher (US005794016A).

21. As per Claim 5, Perego, Furtner, and MacInnis are relied upon for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (col. 8, lines 52-61; col. 9, lines 1-23; col. 6, lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, and MacInnis so at each of at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to

determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (col. 9, lines 1-23), as is well-known in the art.

22. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the first (20A), second (20B), third (20C) and fourth (20N) graphics pipelines (col. 3, lines 22-23; col. 4, lines 9-14; col. 8, lines 56-65; col. 3, lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests the advantage of being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (col. 2, lines 31-35; col. 8, lines 56-65; col. 9, lines 1-23).

23. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (col. 5, lines 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 2nd back end circuitry (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44); and

memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel data (col. 3, lines 65-67; col. 4, lines 1-53; col. 5, lines 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (col. 3, lines 22-23; col. 8, lines 33-col. 9, lines 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23; col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38). This would be obvious for same reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not expressly teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same chip (col. 6, lines 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed for Claim 1.

24. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (col. 8, lines 52-col. 9, lines 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled

by graphics pipelines (col. 8, lines 52-65; col. 6, lines 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (col. 4, lines 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the same reasons given in the rejection for Claim 5.

But, Perego, Furtner, MacInnis, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (col. 1, lines 46-54).

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1), further in view of MacInnis (US006570579B1), further in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (col. 5, lines 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (col. 6, lines 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip

and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

26. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) in view of Furtner (US006778177B1).

27. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (col. 5, lines 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to

be processed by corresponding one of at least two graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (col. 5, lines 19-44); and transmitting processed pixels to memory controller (310), wherein at least two graphics pipelines share memory controller (col. 3, line 65-col. 4, line 25; col. 5, lines 31-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

But, Perego does not expressly teach graphics pipelines (312) are on a same chip. But, Furtner teaches graphics pipelines are on a same chip (col. 6, lines 30-32), as discussed for Claim 1.

28. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (col. 5, lines 19-50).

29. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (col. 5, lines 19-44).

30. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two

graphics pipelines operative to process data in a dedicated tile (col. 5, lines 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

But, Perego does not expressly teach graphics pipelines are on a same chip. But, Furtner teaches graphics pipelines are on a same chip (col. 6, lines 30-32), as discussed for Claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Joni Hsu/
Patent Examiner, Art Unit 2628

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	-								
	9	-								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	-								
	24	✓								
	25	✓								
	26	-								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	12/7/07	JH
Above	UPDATED	7/29/08	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	7/29/08	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	568	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L2	400	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L3	127	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L4	92	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L5	931	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L6	483	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L7	56	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L8	739	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L9	481	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L10	2085	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L11	1693	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L12	384	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L13	316	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L14	192	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L15	145	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L16	316	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L17	456	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L18	166	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L19	115	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

L20	50	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L21	316	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L22	91	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19
L23	141	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 16:19

7/29/08 4:22:02 PM
C:\Documents and Settings\jhsu\My Documents\10459797a.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

In response to the Office Action mailed August 25, 2008, Applicants respond as follows.

Listing of the Claims begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

Listing of Claims:

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (previously presented) The graphics processing circuit of claim 7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front

end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to

be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (previously presented) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 6, 7, 10, 12, 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis. Applicants respectfully request reconsideration in view of the "Response to Arguments" section of the office action and the rejection. Applicants respectfully submit that the cited portion of Perego is being taken out of context and that the actual teachings of Perego are being ignored. Ignoring the teachings of the reference as a whole for purposes of rejecting a claim under 35 U.S.C. §103(a) is improper. Although the Perego reference in the Background section makes a general statement as noted by the Examiner, the Perego reference actually describes an invention that only allows certain elements that are integrated and specifically comes up with an invention whose architecture prevents the integration alleged to be taught by the office action. As specifically stated by Perego in column 4, lines 48-65 reproduced below:

> The architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to the various rendering engines 312, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory modules 304. Thus, the partitioning of memory among multiple memory modules 304 improves graphical data throughput relative to systems in which a single graphics controller performs all processing tasks and reduces bandwidth contention with the CPU. This bandwidth reduction occurs because the primitive commands typically contain significantly less data than the amount of data referenced when rendering the primitive. Additionally, the system partitioning described allows aggregate bandwidth between the rendering engines and the memory devices to be much higher than the bandwidth between the controller and memory modules. Thus, effective system bandwidth is increased for processing graphics tasks. (Emphasis added).

The reference also refers to the specific structure of Perego stating "This ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture." (Column4 , lines 45-48). Perego requires multiple discrete memory modules each

with its own rendering engine and each with its own memory and shared main memory. Perego requires interconnecting such modules to allow variable scalability in addition to requiring shared memory controllers. Moreover, a separate memory controller 310 is required by Perego which is part of a different and separate memory controller subsystem 302 that is coupled "to four distinct memory modules 304". (Column 4, lines 26-36). As stated in the reproduced portion of Perego above, Perego specifically requires a non-integration technique to facilitate the bandwidth reduction described by Perego (above) as well as allowing the scalability described in Perego. The teachings of the reference must not be ignored in a determination as to whether a combination would be obvious and where the combination would result in the inoperability or complete redesign of the cited reference, the combination and alleged suggestion is improper. Perego does not teach or suggest that any and all integration is proper. If so, the Perego patent would be invalid.

The Furtner reference has been cited as being properly combinable with Perego for allegedly teaching a motivation to place multiple graphic pipelines on the same chip as taught by Furtner. However, doing so as specifically stated by Perego would prevent the scalable architecture of Perego from existing. Perego teaches an opposite approach from that claimed and that described by Furtner and instead requires that the interconnecting modules allow variable scalability in addition to requiring shared memory controllers. One of ordinary skill in the art could not obtain a combination given the actual teachings of the references alleged in the office action.

In addition, the MacInnis reference is allegedly cited as teaching that "memory controller 54 is on same chip 10 as graphics pipeline, as shown in FIG. 2" (office action, page 5). Again, it is improper to combine teachings of multiple references wherein those teachings teach away

from one another and would render one of the references to be inoperable. Combining MacInnis with Furtner and Perego could not teach one of ordinary skill in the art that which is claimed since the MacInnis reference specifically teaches an opposite approach from that required by the Perego reference as to the memory controller. As stated in Perego, Perego cannot have a memory controller on the same chip as alleged. Perego would be improperly combinable with MacInnis and Furtner since Perego specifically teaches that the memory controller 310 cannot be integrated with the graphics controller. As set forth in the cited portion above, Perego specifically states that the architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to various rendering engines 312 that are on separate modules, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory module 304. The partitioning of the memory among multiple memory modules improves graphical data throughput etc. Since the office action alleges that it would be obvious for the same reasons given above with respect to Perego, Applicants respectfully submit that this reasoning is not supported by the teachings of the references when the references are considered for what they actually teach. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, as to claim 4, in the "Response to Arguments" section, the Examiner states that "Claim 4 does not recite that multiple graphics pipelines are on the same chip". Applicants respectfully submit that claim 4 does recite this because it includes all of the limitations of claim 1. The office action appears to disregard the actual teachings of Perego since the office action cites the CPU 308 as being the front end circuitry. However, the claim requires that the graphics pipelines include the front end circuitry as claimed. There is no front end circuitry described

related to the CPU 308 in Perego. Applicants respectfully request a showing by column and line number if the rejection is maintained as it does not appear to be present in the cited portions.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis, further in view of Kelleher. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kelleher, further in view of Hamburg. Applicants respectfully reassert the remarks made above with respect to the Perego, Further and MacInnis references and as such, these claims are also believed to be in condition for allowance.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kent. Applicants respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 20-22 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner. Applicants respectfully reassert the remarks made above with respect to Perego and Furtner and as such, these claims are also in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: November 25, 2008

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Acknowledgement Receipt

EFS ID:	4354403
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	25-NOV-2008
Filing Date:	12-JUN-2003
Time Stamp:	16:21:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10459797_Response.pdf	108637 87a32e9a8b434141fe8e8d0021fe3cb5db22806f	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	12
Warnings:			
Information:			
	Total Files Size (in bytes):	108637	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/25/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DORIS m. BURNS/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 02/13/2009

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
02/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed November 25, 2008 have been fully considered but they are not persuasive.

2. As per Claim 1, Applicant argues that Perego (US006864896B2) describes an invention that only allows certain elements that are integrated and specifically comes up with an invention whose architecture prevents the integration alleged to be taught by the office action. The reference also refers to the specific structure of Perego stating "This ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture. Perego requires multiple discrete memory modules each with its own rendering engine and each with its own memory and shared main memory. Moreover, a separate memory controller 310 is required by Perego which is part of a different and separate memory controller subsystem 302 that is coupled to four distinct memory modules 304". Perego specifically requires a non-integration technique to facilitate the bandwidth reduction described by Perego as well as allowing the scalability described in Perego. The teachings of the reference must not be ignored in a determination as to whether a combination would be obvious and where the combination would result in the inoperability or complete redesign of the cited reference, the combination and alleged suggestion is improper. Perego does not suggest that any and all integration is proper. If so, the Perego patent would be invalid. Perego teaches an opposite approach from that claimed and that described by Furtner and instead requires that the interconnection modules allow variable scalability in addition to requiring shared

memory controllers. One of ordinary skill in the art could not obtain a combination given the actual teachings of the references alleged in the office action (p. 8-9).

In reply, the Examiner points out Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; c. 6, ll. 61-62). From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. The Examiner makes note that Claim 1 recites "**at least two** graphics pipelines on a same chip", and this is what Perego teaches.

3. Applicant argues MacInnis (US006570579B1) specifically teaches an opposite approach from that required by Perego as to memory controller. As stated in Perego, Perego cannot have memory controller on the same chip as alleged. Perego specifically teaches that memory controller 310 cannot be integrated with the graphics controller. Perego specifically states that the architecture of Fig. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to various rendering engines 312 that are on separate modules, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory module 304. The partitioning of the memory among multiple memory modules improves graphical data throughput (p. 9-10).

In reply, the Examiner points out that the section in Perego cited by Applicant describes that the reduction in bandwidth is due to the fact that there are a plurality of graphics pipelines, and each graphics pipeline has a corresponding portion of shared memory (c. 4, ll. 48-65). However, Perego does not actually describe that the reduction

in bandwidth is due to the fact that the memory controller is on a separate chip from the graphics pipelines. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to reduce the bandwidth by having the memory controller issue high level primitive commands to various rendering engines that are on the same chip. Therefore, the various rendering engines that are on the same chip would still be able to perform the processing tasks rather than having a single graphic controller perform all the processing tasks, therefore reducing the bandwidth, and reducing bandwidth contention with the CPU. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to operate in the same manner that reduces the bandwidth. Therefore, Perego does not teach away from the teaching from MacInnis, and therefore the teaching from MacInnis is able to be combined with the teachings from Perego.

4. Applicant argues that as to Claim 4 in the "Response to Arguments" section, the Examiner states that "Claim 4 does not recite that multiple graphics pipelines are on the same chip". Claim 4 does recite this because it includes all of the limitations of Claim 1 (p. 10).

In reply, the Examiner respectfully again clarifies that the limitation that multiple graphics pipelines are on the same chip was not expressly addressed in the rejection for Claim 4 because it was **already addressed in the rejection for Claim 1**, and this limitation is not recited in Claim 4. The Examiner understands that Claim 4 includes all of the limitations of Claim 1, but since all of the limitations of Claim 1 were already

addressed in the rejection for Claim 1, the Examiner did not feel the need to continually repeat the rejection for Claim 1 for each of the claims that depend from Claim 1.

5. Applicant argues that the office action cites the CPU 308 as being the front end circuitry. However, the claim requires that the graphics pipelines include the front end circuitry. There is no front end circuitry described related to the CPU 308 in Perego (p. 10-11).

In reply, the Examiner points out that Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (c. 5, ll. 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (c. 1, ll. 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (c. 5, ll. 19-27; c. 1, ll. 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

6. As per Claim 24, Applicant argues that Perego does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip (p. 11).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Furtner (US006778177B1) and Kelleher (US005794016A) are used to expressly teach these limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-4, 6, 7, 10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1).

10. As per Claim 1, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least 2 graphics pipelines operative to process data in dedicated tile (c. 5, ll. 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines 312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (c. 3, ll. 65-67; c. 4, ll. 1-10, 48-65). Shared memories 314 are each part of main memory (c. 1, ll. 44-54; c. 3, ll. 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (c. 1, ll. 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; c. 6, ll. 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800.

However, Perego does not expressly teach graphics pipelines (312) are on a same chip. However, Furtner teaches this limitation (c. 6, ll. 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Perego so graphics pipelines are on same chip as suggested by Furtner. Placing plurality of modules on single chip takes up less space as compared to using multiple chips, and this is well-known in the art.

However, Perego and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches memory controller (54) is on same chip (10) as graphics pipeline (58), as shown in Fig. 2 (c. 4, ll. 65-67; c. 5, ll. 36-41; c. 6, ll. 10-13). This would be obvious for reasons given above. Perego describes that the reduction in bandwidth is due to the fact that there are a plurality of graphics pipelines, and each graphics pipeline has a corresponding portion of shared memory (c. 4, ll. 48-65). However, Perego does not actually describe that the reduction in bandwidth is due to the fact that the memory controller is on a separate chip from the graphics pipelines. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to reduce the bandwidth by having the memory controller issue high level primitive commands to various rendering engines that are on the same chip. Therefore, the various rendering engines that are on the same chip would still be able to perform the processing tasks rather than having a single graphic controller perform all the processing tasks, therefore reducing the bandwidth, and reducing bandwidth contention with the CPU. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to operate in the same manner that reduces the bandwidth. Therefore, Perego does not teach

away from the teaching from MacInnis, and therefore the teaching from MacInnis is able to be combined with the teachings from Perego.

11. As per Claim 2, Perego teaches square regions have two dimensional partitioning of memory (c. 5, ll. 19-33).

12. As per Claim 3, Perego teaches that the memory is a frame buffer (c. 5, ll. 32-33).

13. As per Claim 4, Perego teaches each of at least 2 graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data. Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (c. 5, ll. 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (c. 1, ll. 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (c. 5, ll. 19-27; c. 1, ll. 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end

circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

14. As per Claim 6, Perego does not expressly teach each tile of set of tiles has 16x16 pixel array. But, Furtner teaches this limitation (c. 11, ll. 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (c. 11, ll. 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

15. As per Claim 7, Perego teaches at least two graphics pipelines (312) separately receive pixel data from front end circuitry (308) (c. 3, ll. 64-c. 4, ll. 2; c. 5, ll. 19-44).

16. As per Claim 10, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

17. As per Claim 12, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (c. 5, ll. 23-44).

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (c. 5, ll. 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 17, Perego does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches this limitation (c. 6, ll. 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (c. 6, ll. 29-30, 42-51).

20. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A).

21. As per Claim 5, Perego, Furtner, and MacInnis are relied on for teachings for Claim 4.

But, Perego, Furtner, and MacInnis do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (c. 8, ll. 52-61; c. 9, ll. 1-23; c. 6, ll. 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis so at each of at least two graphics pipelines includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry

because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (c. 9, ll. 1-23), as is well-known in the art.

22. As per Claim 18, Perego does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the 1st (20A), 2nd (20B), 3rd (20C) and 4th (20N) graphics pipelines (c. 3, ll. 22-23; c. 4, ll. 9-14; c. 8, ll. 56-65; c. 3, ll. 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (c. 2, ll. 31-35; c. 8, ll. 56-65; c. 9, ll. 1-23).

23. As per Claim 24, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (c. 5, ll. 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 2nd back end circuitry (c. 3, ll. 63-c. 4, ll. 2; c. 5, ll. 19-44); and memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel

data (c. 3, ll. 65-67; c. 4, ll. 1-53; c. 5, ll. 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (c. 1, ll. 34-43).

However, Perego does not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (c. 3, ll. 22-23; c. 8, ll. 33-c. 9, ll. 23; c. 4, ll. 60-62; c. 8, ll. 52-65; c. 6, ll. 36-38). This would be obvious for reasons given in the rejection for Claim 5.

However, Perego and Kelleher do not expressly teach front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. However, Furtner teaches graphics pipelines are on same

chip (c. 6, ll. 30-32). Front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline, as discussed above. Since Furtner teaches graphics pipelines are on same chip, this teaching from Furtner can be applied to Perego-Kelleher combination so front end circuitry, first back end circuitry, first scan converter, second back end circuitry, and second scan converter are all on same chip. This would be obvious for reasons for Claim 1.

However, Perego, Kelleher, and Furtner do not expressly teach memory controller is also on the same chip. However, MacInnis teaches this limitation, as discussed for Claim 1.

24. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

Perego, Furtner, and MacInnis are relied upon for teachings relative to Claim 10.

However, Perego, Furtner, and MacInnis do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; c. 3, ll. 22-23; c. 4, ll. 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (c. 8, ll. 52-c. 9, ll. 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled by graphics pipelines (c. 8, ll. 52-65; c. 6, ll. 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics

memory (c. 4, ll. 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the reasons given in the rejection for Claim 5.

But, Perego, Furtner, MacInnis, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (c. 5, ll. 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, MacInnis, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (c. 1, ll. 46-54).

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2), Furtner (US006778177B1), and MacInnis (US006570579B1) in view of Kent (US 20030164830A1).

Perego, Furtner, and MacInnis are relied on for teachings for Claim 17. Perego teaches data includes polygon (c. 5, ll. 19-23). Furtner teaches third and fourth graphics pipelines are on separate chips (c. 6, ll. 47-51), as discussed for Claim 17.

But, Perego, Furtner, and MacInnis do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and

testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Perego, Furtner, and MacInnis to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

26. Claims 20-22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2) and Furtner (US006778177B1).

27. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (c. 5, ll. 19-25), which is inherently generated in response to received vertex data; determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of at least two

graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (c. 5, ll. 19-44); and transmitting processed pixels to memory controller 310, at least 2 graphics pipelines share memory controller (c. 3, ll. 65-c. 4, ll. 25; c. 5, ll. 31-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (c. 1, ll. 34-39).

But, Perego does not expressly teach graphics pipelines (312) are on a same chip. But, Furtner teaches this limitation (c. 6, ll. 30-32), as discussed for Claim 1.

28. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (c. 5, ll. 19-50).

29. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (c. 5, ll. 19-44).

30. As per Claim 25, Perego teaches graphics processing circuit (300, Fig. 3; c. 3, ll. 61-63) having at least two graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least two graphics pipelines operative to process data in a dedicated tile (c. 5, ll. 19-27, 38-44), wherein the repeating tile pattern includes a horizontally and

vertically repeating pattern of regions of square regions, as shown in Fig. 5 (c. 5, ll. 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (c. 1, ll. 34-39).

But, Perego does not expressly teach graphics pipelines are on a same chip. But, Furtner teaches this limitation (c. 6, ll. 30-32), as discussed for Claim 1.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED

Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	7/29/08	JH
Above	UPDATED	2/6/09	JH

SEARCH NOTES

Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	2/6/09	JH

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008	02/06/2009							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	-	-							
	9	-	-							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							
	21	✓	✓							
	22	✓	✓							
	23	-	-							
	24	✓	✓							
	25	✓	✓							
	26	-	-							

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S129	597	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S130	423	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S131	134	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S132	99	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S133	975	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S134	506	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S135	57	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S136	765	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

S137	507	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S138	2244	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S139	1835	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S140	405	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S141	332	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S142	203	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S143	153	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

S144	332	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S145	491	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S146	182	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S147	120	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S148	55	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S149	333	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S150	105	(multiple plural $3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42
S151	147	graphic$1 adj pipelin$3 same memory adj controller $1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/02/06 16:42

2/6/09 4:58:45 PM
C:\Documents and Settings\jhsu\My Documents\10459797a.wsp

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (12-08)
Approved for use through 01/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	10/459,797	Filing Date	2003-06-12	Docket Number (if applicable)	00100.02.0053	Art Unit	2628
First Named Inventor	Mark M. Leather			Examiner Name	Joni Hsu		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 500441

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (12-08)
Approved for use through 01/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/Christopher J. Reckamp/	Date (YYYY-MM-DD)	2009-05-13
Name	Christopher J. Reckamp	Registration Number	34414

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

In response to the Final Office Action mailed February 13, 2009, Applicants submit a Request for Continued Examination and the following preliminary amendment:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (previously presented) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (previously presented) The graphics processing circuit of claim 7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (currently amended) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

passing the same pixel data to both of the at least two graphics pipelines on a same chip;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of the at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels; and a memory controller on the chip, coupled to the at least two graphics pipelines on the chip.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 6, 7, 10, 12, 14 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis. Applicants wish to thank the Examiner for the comments in the "Response to Arguments" section of final action. However, it appears that a conflicting rejection is present. A new reasoning has been provided compared to the previous rejection as noted on page 7 of the final action. For the first time, the office action raises that "Perego shows in FIG. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810…and therefore at least two graphic pipelines…are on a same memory module 800". In the "Response to Arguments" section on page 3, the Examiner states "Claim 1 recites "at least two graphics pipeline on a same chip" and this is what Perego teaches." However, in the rejection, it is Furtner that is cited as teaching graphics pipelines are on a same chip. (Page 7 of office action). If Furtner is not being applied, Applicants respectfully request that the rejection be withdrawn. As it currently stands, Applicants are unable to determine which reference the Examiner is using in an attempt to render the claims unpatentable.

As to claim 1, it is also alleged that "Perego does not actually describe that the reduction in bandwidth is due to the fact that the memory controller is on the separate chip from the graphics pipelines. Therefore, if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same chip, the device of Perego would still be able to reduce the bandwidth by having memory controller issue high level primitive commands to various rendering engines that are on the same chip. …therefore if the device of Perego is modified so that the memory controller and at least two graphics pipelines are on the same, chip, the device of Perego would still be able to operate in the same manner that reduces the

bandwidth. Therefore, Perego does not teach away from the teaching from MacInnis, and therefore the teaching from MacInnis is able to be combined with the teaching from Perego."

Applicants respectfully submit that the teachings of Perego and statements in Perego are being ignored. Perego is specifically directed to a system architecture that "provid[es] scalability option to higher levels of aggregate memory bandwidth" (col. 2, lns. 53-57). Applicants have previously noted the scalability architecture of Perego is key to Perego's invention as stated in Perego's specification and title. The modules described in Perego having rendering engines and shared main and graphics memory thereon are always described as being separate from the CPU/memory controller subsystem and memory controller 310. This is because the separate modules from the memory controller provides the specific scalability provided by the architecture of Perego. Removing this scalability renders the Perego invention inoperable for its intended purpose. In addition, Applicants again note that Perego refers to the bandwidth reduction that occurs due to the scalability "allows aggregate bandwidth between the rendering engines and the memory device to be much higher than the bandwidth between the controller [memory controller] and memory modules. Thus effective system bandwidth is increased for processing graphics tasks." (col. 4, lns. 50-65). Moreover, Perego specifically states that as to the scalability which is a requirement of Perego, "this ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture" (col. 4, lns. 45-48). These teachings cannot be ignored in an effort to render Applicants' claims unpatentable. Perego specifically requires the separate memory controller 310 to be separate from the separate memory controller that is coupled to the memory modules 304. Perego specifically requires a non-integration technique to facilitate his scalability and operation.

In addition, the MacInnis reference is allegedly cited as teaching that "memory controller 54 is on same chip 10 as graphics pipeline, as shown in FIG. 2" (office action, page 5). Again, it is improper to combine teachings of multiple references wherein those teachings teach away from one another and would render one of the references to be inoperable. Combining MacInnis with Furtner and Perego could not teach one of ordinary skill in the art that which is claimed since the MacInnis reference specifically teaches an opposite approach from that required by the Perego reference as to the memory controller. As stated in Perego, Perego cannot have a memory controller on the same chip as alleged. Perego would be improperly combinable with MacInnis and Furtner since Perego specifically teaches that the memory controller 310 cannot be integrated with the graphics controller otherwise his scalability is negated. As set forth in the cited portion above, Perego specifically states that the architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to various rendering engines 312 that are on separate modules, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory module 304. The partitioning of the memory among multiple memory modules improves graphical data throughput etc. Since the office action alleges that it would be obvious for the same reasons given above with respect to Perego, Applicants respectfully submit that this reasoning is not supported by the teachings of the references when the references are considered for what they actually teach. Accordingly, Applicants respectfully submit that the claims are in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter. For example, as to claim 4, there is no front end circuitry described related to the CPU 308 in Perego since admitted in the "Response to Arguments" section, the CPU of Perego does not generate

pixel data. Applicants respectfully request a showing by column and line number if the rejection is maintained as it does not appear to be present in the cited portions.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner, further in view of MacInnis, further in view of Kelleher. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance. Claim 24 requires front end circuitry on a chip and first and second backend circuitry on the chip. The first and second backend circuitry processes different portions of the pixel data in response to position coordinates. A memory controller on the same chip is also coupled to the first and second backend circuitry. In this example, common front end circuitry is used on a chip for multiple backend operations. Again, the Perego reference illustrates a completely different structure and does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip as claimed. As such, the claim is also in condition for allowance. Also, these claims add additional novel and non-obvious subject matter.

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kelleher, further in view of Hamburg. Applicants respectfully reassert the remarks made above with respect to the Perego, Further and MacInnis references and as such, these claims are also believed to be in condition for allowance. In addition, the reference does not teach the tile in data in combination as claimed.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego, in view of Furtner, further in view of MacInnis, further in view of Kent. Applicants

respectfully reassert the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 20-22 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego in view of Furtner. Applicants have amended claim 20 to indicate that the process is directed to passing the same pixel data to both of the two graphics pipelines on a same chip. (See for example, Specification describing shared front end). The method also includes determining the pixels within a set of tiles of the repeating pattern which are to be processed by corresponding graphics pipeline on the same chip in response to the pixel data. As such, entire triangles may be rejected at the input to a scan converter when it has been determined that they lie entirely outside the set of tiles owned by its pipelines. Other advantages will be recognized by those of ordinary skill in the art.

The dependent claims add additional novel and non-obvious subject matter.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: May 13, 2009

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

Electronic Patent Application Fee Transmittal	
Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	5331837
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	13-MAY-2009
Filing Date:	12-JUN-2003
Time Stamp:	21:02:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	7005
Deposit Account	500441
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	10459797_IDS.pdf	608458 797f35070139ae47c305ff9d2381ed8a1f324acb	no	4
Warnings:					
Information:					
2	Transmittal Letter	10459797_IDSCover.pdf	70507 b11c424c53a05bfd41ee061ed95dba8bcc813c30	no	1
Warnings:					
Information:					
3	NPL Documents	10459797_Ref.pdf	2004500 37680eec53592334f809905f10cc03e77ff8dcde	no	10
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	10459797_RCETransmittal.pdf	697435 1cfebae046d39e46b54c8623bb17436f39438d70	no	3
Warnings:					
Information:					
5		10459797_response.pdf	116628 f82cb3dfb40763bb7c9d67d39adcd0d3b1dd21ae	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	12

Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	30075 110784f12639bd35872b3823d227fe6fb8cb776e	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	3527603

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (10-08)
Approved for use through 11/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	10459797
Filing Date	2003-06-12
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4885703		1989-12-05	Deering	
	2	5999196		1999-12-07	Storm et al.	
	3	6407736		2002-06-18	Regan	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

EFS Web 2.1.7

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	10459797
	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	FUCHS, HENRY et al.; Pixel-Planes 5: A Heterogeneous Multiprocessor Graphics System Using Processor-Enhanced Memories; Computer Graphics; Vol. 23, No. 3; July 1989; pages 79-88.	☐

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10459797
	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher J. Reckamp/	Date (YYYY-MM-DD)	2009-05-13
Name/Print	Christopher J. Reckamp	Registration Number	34,414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148
Examiner: Joni Hsu
Art Unit: 2628
Atty. Docket No.: 00100.02.0053
Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT IN ACCORDANCE WITH 37 CFR §§ 1.97(c) AND 1.98

Pursuant to 37 CFR §§ 1.97(c) and 1.98, Applicants respectfully submit form PTO/SB/08A.

The submission of the listed documents are not an admission that the information is prior art, analogous or otherwise material. It is respectfully requested that the listed documents be considered and made of record in the present application.

The Patent Office is hereby authorized to charge the fee of $180.00 set forth in 37 CFR 1.17(p) to Deposit Account No. 50-0441 and is authorized to charge any additional fees required or credit any overpayments to this account.

Respectfully submitted,

Date: May 13, 2009

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
Phone: (312) 609-7599
Fax: (312) 609-5005

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/13/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LASHAWN MARKS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 07/23/2009

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
07/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/13/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 13, 2009 has been entered.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on May 13, 2009 was filed after the mailing date of the application on June 12, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

3. Applicant's arguments, see p. 8-12, filed May 13, 2009, with respect to the rejection(s) of claim(s) 1-7, 10-22, 24, and 25 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of MacInnis (US006570579B1) in view of Perego (US006864896B2).

4. As per Claim 1, Applicant argues that in the "Response to Arguments" section, the Examiner states "Claim 1 recites 'at least two graphics pipelines on a same chip' and this is what Perego teaches'". However, in the rejection, it is Furtner (US006778177B1) that is cited as

teaching graphics pipelines are on a same chip. As it currently stands, Applicants are unable to determine which reference the Examiner is using (p. 8).

In reply, the Examiner points out that Furtner was used because it more explicitly teaches the limitation. However, the Examiner agrees that this may be confusing, and is no longer applying Furtner to teach this limitation.

5. Applicant argues that Perego states that as to the scalability which is a requirement of Perego, "this ability to add and remove memory modules 304 provides an upgradeable and scalable memory and computing architecture." Perego requires the separate memory controller 310 to be separate from the separate memory controller that is coupled to the memory modules 304. Therefore, the teaching from MacInnis that the memory controller is also on the same chip cannot be combined with Perego because removing the scalability renders the Perego invention inoperable for its intended purpose (p. 8-9).

In reply, the Examiner agrees. However, new grounds of rejection are made so that MacInnis is used as the main reference and the teaching of the repeating tile pattern from Perego is combined into the main reference MacInnis. Therefore, Perego is now only being used for the teaching of the repeating tile pattern, not for the teaching of the scalability. Since Perego is now only being used as a secondary reference, the Examiner is no longer relying on the entire device of Perego for the rejection.

6. As per Claim 4, Applicant argues that there is no front end circuitry described related to the CPU 308 in Perego since admitted in the "Response to Arguments" section, the CPU of Perego does not generate pixel data (p. 10-11).

In reply, the Examiner points out that Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (col. 5, lines 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (col. 1, lines 18-21). Therefore, the **CPU** is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and **generate pixel data** corresponding to a primitive to be rendered (col. 5, lines 19-27; col. 1, lines 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

7. As per Claim 24, Applicant argues that Perego does not describe multiple backend circuitry on a common chip nor common front end circuitry and memory controller on a common chip (p. 11).

In reply, the Examiner points out that Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module

800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip, and so first backend circuitry (first rendering engine 312) and second backend circuitry (second rendering engine 312) (col. 3, lines 65-67; col. 4, liens 1-53; col. 5, lines 32-44) are on a common chip. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). MacInnis is used to expressly teach common front end circuitry and memory controller are on a common chip.

8. As per Claim 20, Applicant argues that Perego does not teach passing the same pixel data to both of the two graphics pipelines on a same chip. (See for example, Specification describing shared front end). Perego does not teach determining the pixels within a set of tiles of the repeating pattern which are to be processed by corresponding graphics pipeline on the same chip in response to pixel data (p. 12).

In reply, the Examiner points out that Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines. Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From

Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. Perego teaches determining the pixels within a set of tiles of the repeating pattern which are to be processed by corresponding graphics pipeline on the same chip in response to pixel data (col. 5, lines 19-44).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-4, 7, 10, 12, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2).

12. As per Claim 1, MacInnis teaches a graphics processing circuit, comprising: a graphics pipeline (58, Fig. 2) on a chip (10); a memory controller (54) on the chip (10), as shown in Fig. 2 (col. 4, lines 65-67; col. 5, lines 36-41), in communication with the graphics pipeline (58),

operative to transfer pixel data between the pipeline (58) and a memory (col. 6, lines 10-13, 59-66).

However, MacInnis does not teach at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least 2 graphics pipelines operative to process data in dedicated tile (col. 5, lines 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines 312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego

shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions because Perego suggests that this parallel processing significantly reduces the processing burden on the memory controller/graphics controller (col. 5, lines 38-46).

13. As per Claim 2, MacInnis does not teaches that the square regions comprise a two dimensional partitioning of memory. However, Perego teaches square regions have two dimensional partitioning of memory (col. 5, lines 19-33). This would be obvious for the reasons given in the rejection for Claim 1.

14. As per Claim 3, MacInnis teaches wherein the memory is a frame buffer (col. 6, line 66-col. 7, line 2).

15. As per Claim 4, MacInnis does not teach that each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end

circuitry, operative to receive and process a portion of the pixel data. However, Perego teaches each of at least 2 graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data. Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (col. 5, lines 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (col. 1, lines 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (col. 5, lines 19-27; col. 1, lines 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline. This would be obvious for the reasons given in the rejection for Claim 1.

16. As per Claim 7, MacInnis does not teach that the at least two graphics pipelines separately receive the pixel data from the front end circuitry. However, Perego teaches at least two graphics pipelines (312) separately receive pixel data from front end circuitry (308) (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). This would be obvious for the reasons given in the rejection for Claim 1.

17. As per Claim 10, MacInnis does not teach that a first of the at least two graphics pipelines processes the pixel data only in the first set of tiles in the repeating tile pattern. However, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

18. As per Claim 12, MacInnis does not teach that a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern. However, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

19. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (col. 5, lines 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

20. As per Claim 25, Claim 25 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

21. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A).

22. As per Claim 5, MacInnis and Perego are relied on for teachings for Claim 4.

But, MacInnis and Perego do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (col. 8, lines 52-61; col. 9, lines 1-23; col. 6, lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so at each of at least two graphics pipelines includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (col. 9, lines 1-23), as is well-known in the art.

23. As per Claim 18, MacInnis does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the 1st (20A), 2nd (20B), 3rd (20C) and 4th (20N) graphics pipelines (col. 3, lines 22-23; col. 4, lines 9-14; col. 8, lines 56-65; col. 3, lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include a bridge operable to transmit vertex data to each of the

first, second, third and fourth graphics pipelines because Kelleher suggests being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (col. 2, lines 31-35; col. 8, lines 56-65; col. 9, lines 1-23).

24. As per Claim 24, MacInnis teaches a graphics processing circuit, comprising: front end circuitry (90, Fig. 4) operative to generate pixel data in response to primitive data for a primitive to be rendered (col. 8, lines 49-59); back end circuitry (98), coupled to the front end circuitry (90) (col. 9, lines 15-34), operative to process the pixel data in response to position coordinates (col. 9, lines 35-54). The front end circuitry (90) and the back end circuitry (98) are in the graphics display pipeline (80) (col. 7, lines 55-63), and the graphics display pipeline (80) is equivalent to display engine (58, Fig. 2), which is on graphics chip (10) (col. 4, lines 65-67; col. 5, lines 36-39). A memory controller (54) is also on graphics chip (10) (col. 4, lines 65-67; col. 5, lines 36-39). Therefore, the front end circuitry (90), the back end circuitry (98), and the memory controller (54) are on the chip (10). The memory controller (54) is coupled to the display engine (58) and is operative to transmit and receive the processed pixel data (col. 6, lines 10-13, 59-67; col. 7, lines 1-2). Since the display engine (58) is equivalent to the graphics display pipeline (80) which contains the back end circuitry (98) (col. 6, lines 59-67; col. 7, lines 55-63), the memory controller (54) is coupled to the back end circuitry (98) and is operative to transmit and receive the processed pixel data.

However, MacInnis does not teach first back end circuitry operative to process a first portion of the pixel data; set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; second back end circuitry operative to process a second portion of the

pixel data; set of tiles of the repeating tile pattern are to be processed by the second back end circuitry. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (col. 5, lines. 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 2nd back end circuitry (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44); and memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel data (col. 3, lines 65-67; col. 4, lines 1-53; col. 5, lines 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module

800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip, and so the front end circuitry, first back end circuitry, and second back end circuitry are on the same chip. This would be obvious for the reasons given in the rejection for Claim 1.

However, MacInnis and Perego do not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23; col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38). Therefore, by implement this teaching into the device of Perego, front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline. Since Perego teaches graphics pipelines are on the same chip, the teaching from Kelleher can be applied to Perego so that the

first scan converter and the second scan converter are also on the same chip. This would be obvious for reasons given in the rejection for Claim 5.

25. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1).

26. As per Claim 6, MacInnis and Perego are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis and Perego do not expressly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner teaches that each tile of the set of tiles further comprises a 16x16 pixel array (col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (col. 11, lines 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

27. As per Claim 17, MacInnis does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches this limitation (col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis so pipelines are on separate chips because Furtner teaches this

makes system more configurable by being able to easily add more graphics pipelines to increase performance (col. 6, lines 29-30, 42-51).

28. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

MacInnis and Perego are relied upon for teachings relative to Claim 10.

However, MacInnis and Perego do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (col. 8, line 52-col. 9, line 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled by graphics pipelines (col. 8, lines 52-65; col. 6, lines 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (col. 4, lines 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the reasons given in the rejection for Claim 5.

But, MacInnis, Perego, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile

identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (col. 1, lines 46-54).

29. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1), further in view of Kent (US 20030164830A1).

MacInnis, Perego, and Furtner are relied upon for the teachings as discussed above relative to Claim 17. MacInnis teaches data includes polygon (col. 58, lines 50-54). Furtner teaches third and fourth graphics pipelines are on separate chips (col. 6, lines 47-51), as discussed for Claim 17.

But, MacInnis, Perego, and Furtner do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and

graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Furtner to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

30. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2).

31. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (col. 5, lines 19-25), which is inherently generated in response to received vertex data. Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines. Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. Perego teaches determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of the at least two graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of

square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (col. 5, lines 19-44); and transmitting processed pixels to memory controller 310, at least 2 graphics pipelines share memory controller (col. 3, line 65-col. 4, line 25; col. 5, lines 31-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

32. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (col. 5, lines 19-50).

33. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (col. 5, lines 19-44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Joni Hsu/
Examiner, Art Unit 2628

Receipt date: 05/13/2009
Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (10-08)
Approved for use through 11/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	10459797
Filing Date	2003-06-12
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4885703		1989-12-05	Deering	
	2	5999196		1999-12-07	Storm et al.	
	3	6407736		2002-06-18	Regan	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

EFS Web 2.1.7

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.H./

Receipt date: 05/13/2009	Application Number	10459797
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

If you wish to add additional Foreign Patent Document citation information please click the Add button			Add
NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	FUCHS, HENRY et al.; Pixel-Planes 5: A Heterogeneous Multiprocessor Graphics System Using Processor-Enhanced Memories; Computer Graphics; Vol. 23, No. 3; July 1989; pages 79-88.	☐
If you wish to add additional non-patent literature document citation information please click the Add button			Add

EXAMINER SIGNATURE			
Examiner Signature	/Joni Hsu/	Date Considered	07/21/2009

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.H./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	2/6/09	JH
Above	UPDATED	7/21/09	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	7/21/09	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008	02/06/2009	07/21/2009						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	-	-	-						
	9	-	-	-						
	10	✓	✓	✓						
	11	✓	✓	✓						
	12	✓	✓	✓						
	13	✓	✓	✓						
	14	✓	✓	✓						
	15	✓	✓	✓						
	16	✓	✓	✓						
	17	✓	✓	✓						
	18	✓	✓	✓						
	19	✓	✓	✓						
	20	✓	✓	✓						
	21	✓	✓	✓						
	22	✓	✓	✓						
	23	-	-	-						
	24	✓	✓	✓						
	25	✓	✓	✓						
	26	-	-	-						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	621	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L2	451	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L3	141	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L4	100	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L5	1017	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L6	533	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27

L7	59	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L8	793	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L9	535	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L10	2361	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L11	1931	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L12	428	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L13	337	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27

L14	207	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L15	155	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L16	337	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L17	510	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L18	189	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L19	124	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27

L20	58	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L21	345	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L22	122	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27
L23	156	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/07/21 13:27

EAST Search History (Interference)

< This search history is empty>

7/21/09 1:29:11 PM
C:\Documents and Settings\jhsu\My Documents\10459797a.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148

Examiner: Joni Hsu
Art Unit: 2628
Our File No.: 00100.02.0053

Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed July 23, 2009, Applicants petition for a three month extension of time and respond as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. (original) The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. (original) The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. (original) The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. (original) The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

6. (original) The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. (original) The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

8. (canceled)

9. (canceled)

10. (previously presented) The graphics processing circuit of claim 7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. (original) The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. (previously presented) The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. (previously presented) The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

14. (original) The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. (original) The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for

receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. (original) The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

17. (original) The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. (original) The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. (original) The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. (currently amended) A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

passing the same pixel data to both of the at least two graphics pipelines on a same chip;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of the at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller wherein the memory controller transfers pixel data from each of the at least two pipelines, to a shared memory.

21. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. (original) The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

23. (canceled)

24. (previously presented) A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. (currently amended) A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels; and a memory controller on the chip, coupled to the at least two graphics pipelines on the chip and operative to transfer pixel data between each of the two graphics pipelines and a memory shared among the at least two graphics pipelines.

26. (canceled)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1-4, 7, 10, 12, 14 and 25 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacInnis in view of Perego. This is a new ground of rejection. Applicants wish to thank the Examiner for the remarks in the office action. Applicants have amended claims to indicate what is believed to be inherent subject matter, that the memory controller that is on chip with the at least two graphics pipelines transfers pixel data between each of the first and second pipelines and a memory that is shared among the at least two on chip pipelines.

MacInnis is a conventional graphics processing circuit that includes a single pipeline and corresponding memory controller on chip. It is admitted that MacInnis does not teach at least two graphics pipelines on a same chip that process data in a corresponding set of tiles for a repeating tile pattern corresponding to screen locations. Nor does it teach a plurality of graphics pipelines and associated memory controller on the same chip in communication with the at least two graphics pipelines wherein the memory controller transfers pixel data between each of the two pipelines and a memory that is shared among the at least two graphic on chip pipelines. The office action alleges that Perego teaches this subject matter.

The office alleges that the memory controller 310 in FIG. 3 is in communication with at least two graphic pipelines but the office action appears to disregard the actual teachings of Perego. Applicants respectfully submit that is improper to use hindsight reconstruction and ignore the teachings of the reference as a whole in an effort to render a claim obvious. The memory controller 310 is intentionally left off of the modules 304 that include rendering engines and their own dedicated memory. The purpose of the Perego structure is to "provide scalability option to higher levels of aggregate memory bandwidth" (col. 2, lns. 53-57). Perego actually

teaches "a system…that provides multiple discrete memory modules coupled to a common memory controller [which is off chip from the dedicated memory modules]. Each memory module includes a computing engine and a shared memory. A data processing task from the memory controller can be partitioned among the different computing engines to allow parallel processing of the various portions of the processing task." (col. 7, lns. 35-42). As such, the modules described in Perego that have rendering engines also have dedicated memory thereon that are always described as being separate from the CPU/memory controller subsystem and memory controller 310. This is because the separate modules from the memory controller 310 provides the specific scalability provided by the architecture of Perego. Perego specifically requires the separate memory controller 310 to be off chip and separate from the memory modules 304. As such, combining the graphic pipeline teachings of Perego with those of MacInnis would render the Perego system inoperable.

In addition, or alternatively, the office action alleges that the shared memories 314 are each part of main memory and "so are considered to be one memory". However, Applicants respectfully submit that this is a misconstruction of the actual teachings of the reference. The shared memories 314 are actually dedicated memories that are each dedicated to a dedicated graphics pipeline and in no embodiment are these dedicated memories that are on separate modules ever described as storing data from more than one rendering engine. This is because this would again eliminate the advantages of Perego's scalable unified memory architecture. As claimed, not only is the memory controller on chip and in communication with two graphics pipelines that are also on the same chip, but the memory controller is in communication with a memory that is shared among the at least two graphics on chip pipelines.

FIG. 8 has been alleged as being properly combinable to teach multiple rendering engines on the same chip and an on chip memory controller that communicates with the memory that is shared among the at least two graphics on chip pipelines. However, as shown in FIG. 8, it is clear that memory devices 804 are only in communication with rendering engine 802 whereas memory devices 812 are only in communication with rendering engine 810. These memories are dedicated and are separate and are not shared among graphics pipelines or rendering engines 802 and 810. Accordingly, Applicants respectfully request reconsideration and believe that the claims are in condition for allowance. The dependent claims are believed to add additional novel and non-obvious subject matter.

As to claim 25, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and as such, this claim is also believed to be in condition for allowance.

Claims 5, 18, and 24 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacInnis in view of Perego further in view of Kelleher. Claims 5 and 18 are believed to be in condition for allowance as adding novel and non-obvious subject matter and/or being based on allowable base claims.

As to independent claim 24, it is alleged that Perego teaches "that two graphics pipelines are the same chip, and so the front end circuitry, first back end circuitry, and second back end circuitry on the same chip." (office action, page 14) referring to FIG. 8. However, Perego does not teach nor does nit contemplate both front and back end circuitry on the chip both coupled to the same front end circuitry as claimed. In fact, FIG. 8 actually shows separate front end circuitry being employed since separate rendering engines 802 and 810 are employed and each of these are identical in structure. There is no teaching or suggestion in Perego as alleged and as such, this claim is in condition for allowance.

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacInnis, in view of Perego further in view of Furtner. These claims are believed to add additional novel and non-obvious subject matter and are also allowable at least as depending on allowable base claims.

Claims 11, 13, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacInnis, in view of Perego further in view of Kelleher, further in view of Hamburg. These claims are believed to add additional novel and non-obvious subject matter and are also allowable at least as depending on allowable base claims.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over MacInnis, in view of Perego, further in view of Furtner, further in view of Kent. This claim is believed to add additional novel and non-obvious subject matter and is also allowable at least as depending on an allowable base claim.

Claims 20-22 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Perego. These claims are believed to add additional novel and non-obvious subject matter and are also allowable at least as depending on allowable base claims.

The dependent claims add additional novel and non-obvious subject matter.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

/Christopher J. Reckamp/

Date: January 25, 2010

By: _____
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
phone: (312) 609-7599
fax: (312) 609-5005

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Mark M. Leather et al.
Serial No.: 10/459,797
Filing Date: June 12, 2003
Confirmation No.: 4148
Examiner: Joni Hsu
Art Unit: 2628
Atty. Docket No.: 00100.02.0053
Title: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**

Mail Stop amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT IN ACCORDANCE WITH 37 CFR §§ 1.97(c) AND 1.98

Pursuant to 37 CFR §§ 1.97(c) and 1.98, Applicants respectfully submit form PTO/SB/08A. The submission of the listed documents are not an admission that the information is prior art, analogous or otherwise material. It is respectfully requested that the listed documents be considered and made of record in the present application.

The Patent Office is hereby authorized to charge the fee of $180.00 set forth in 37 CFR 1.17(p) to Deposit Account No. 50-0441 and is authorized to charge any additional fees required or credit any overpayments to this account.

Respectfully submitted,

Date: January 25, 2010

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 North LaSalle Street, Suite 2600
Chicago, Illinois 60601
Phone: (312) 609-7599
Fax: (312) 609-5005

Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (10-08)
Approved for use through 11/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	10459797
Filing Date	2003-06-12
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6750867		2004-06-15	Gibson	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060170690	A1	2006-08-03	Leather	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10459797
	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	10459797
	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher J. Reckamp/	Date (YYYY-MM-DD)	2010-01-25
Name/Print	Christopher J. Reckamp	Registration Number	34,414

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Evelyn Stenseth
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	1253	1	1110	1110

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**1290**

Electronic Acknowledgement Receipt	
EFS ID:	6874069
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Evelyn Stenseth
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	25-JAN-2010
Filing Date:	12-JUN-2003
Time Stamp:	15:43:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1290
RAM confirmation Number	2146
Deposit Account	220259
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	EOT.pdf	331665 35a1612920aee656170ad8c930e2b1dd3da8d463	no	2
Warnings:					
Information:					
2		Amendment.pdf	159858 7cd568450e51a07e5c93209ca1dcb1b813a04b08	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	8
Applicant Arguments/Remarks Made in an Amendment	9	13

Warnings:					
Information:					
3	Transmittal Letter	IDSCover.pdf	133734 085275ea6c70e541477c7385d0e1483ffd476fd8	no	1
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	IDS.pdf	607891 cb71ddeee4395f103cc387e92be839e51dd2080d	no	4
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	32070 d884b24e6c641a5a9bd30c69ff7439e93917dbb4	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1265218		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) **FY 2009** (*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*)	Docket Number (Optional) 00100.02.0053
Application Number 10/459797	Filed 06/12/2003
For Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique	
Art Unit 2628	Examiner Joni Hsu

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$130	$65	$
☐	Two months (37 CFR 1.17(a)(2))	$490	$245	$
☑	Three months (37 CFR 1.17(a)(3))	$1110	$555	$ 1110.00
☐	Four months (37 CFR 1.17(a)(4))	$1730	$865	$
☐	Five months (37 CFR 1.17(a)(5))	$2350	$1175	$

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 220259.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration Number 34414

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Christopher J. Reckamp/ — Signature

2010-01-25 — Date

Christopher J. Reckamp — Typed or printed name

312.609.7599 — Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/459,797	06/12/2003	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 01/25/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 22	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
//REGINA D. BALTIMORE//

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 04/22/2010

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
04/22/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/459,797	LEATHER ET AL.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/25/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on January 25, 2010 was filed after the mailing date of the application on June 12, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

2. Applicant's arguments filed January 25, 2010 have been fully considered but they are not persuasive.

3. Applicant argues that it is improper to use hindsight reconstruction and ignore the teachings of the reference as a whole in an effort to render a claim obvious (p. 9).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. As per Claim 1, Applicant argues that the separate modules from the memory controller 310 provide the specific scalability provided by the architecture of Perego (US006864896B2). Perego requires the separate memory controller 310 to be off chip and separate from the memory

modules. As such, combining the graphic pipeline teachings of Perego with those of MacInnis (US006570579B1) would render the Perego system inoperable (p. 10).

In reply, the Examiner respectfully points out that the main reference MacInnis is used to teach that the graphics pipeline (58, Fig. 2) and the memory controller (54) are on the same chip (10) (Fig. 2; col. 4, lines 65-67; col. 5, lines 36-41). Perego is used for its teaching of two graphics pipelines on the same chip to process data in a set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. Perego is used as a secondary reference to modify the device of the main reference MacInnis. Thus, these teachings from the secondary reference Perego are being implemented into the device of the main reference MacInnis. Perego is not being used as the main reference, and so the teaching that the graphics pipeline and the memory controller are on the same chip from MacInnis is not being implemented into the device of Perego to render the device of Perego inoperable. Since these teachings from the secondary reference Perego are being implemented into the device of the main reference MacInnis, and the device of the main reference MacInnis is still operable after this implementation, the combination is proper.

5. Applicant argues that the shared memories 314 of Perego are dedicated memories that are each dedicated to a dedicated graphics pipeline and in no embodiment are these dedicated memories that are on separate modules ever described as storing data from more than one rendering engine. This is because this would eliminate the advantages of Perego's scalable unified memory architecture (p. 10). As shown in Fig. 8, memory devices 804 are only in

communication with rendering engine 8012 whereas memory devices 812 are only in communication with rendering engine 810. These memories are dedicated and are separate and are not shared among graphics pipelines or rendering engines 802 and 810 (p. 11).

In reply, the Examiner points out that Perego describes "The shared memory 314 typically includes multiple memory devices coupled together to form a block of storage space" (col. 4, lines 8-10). Thus, the block of storage space is considered to be a memory shared among the two graphics pipelines. Claim 1 recites "at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile…wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions", and Claim 2 recites "wherein the square regions comprise a two dimensional partitioning of memory". Since each graphics pipeline processes a dedicated tile that is a square region, and each square region is a partition of memory, this means that each graphics pipelines stores data to a partition of memory. Since Perego teaches that each graphics pipeline stores data to a partition of the block of storage space, and the block of storage space is shared among the two graphics pipelines (col. 1, lines 44-54; col. 3, lines 3-6, 65-67; col. 4, lines 1-10, 48-65; col. 5, lines 42-44), Perego reads on the limitations as recited in the claim.

6. As per Claim 24, Applicant argues that Fig. 8 of Perego shows separate front end circuitry being employed since separate rendering engines 802 and 810 are employed and each of these are identical in structure. Thus, Perego does not teach that there is one front end circuitry that sends pixel data to both the first back end circuitry and the second back end circuitry (p. 11).

In reply, the Examiner points out that MacInnis is used to teach that the front end circuitry (90), the back end circuitry (98) and the memory controller (54) are on the same chip (10) (col. 7, lines 55-63; col. 4, lines 65-67; col. 5, lines 36-39). Perego teaches one front end circuitry (308, Fig. 3) that sends pixel data to both the first back end circuitry (first rendering engine 312) and the second back end circuitry (second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44). The first back end circuitry (802, Fig. 8) and the second back end circuitry (810) are on the same chip (800) (Fig. 8; col. 6, lines 61-62). Since MacInnis teaches that the front end circuitry, the back end circuitry and the memory controller are on the same chip, this teaching from Perego can be implemented into the device of MacInnis so that the front end circuitry sends pixel data to both the first back end circuitry and the second back end circuitry, and the front end circuitry, the first back end circuitry, the second back end circuitry, and the memory controller are on the same chip.

Claim Objections

7. Claim 20 is objected to because of the following informalities: Claim 20 recites "…the memory controller wherein the memory controller…" where it should recite "…the memory controller**,** wherein the memory controller…". Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-4, 7, 10, 12, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2).

11. As per Claim 1, MacInnis teaches a graphics processing circuit, comprising: a graphics pipeline (58, Fig. 2) on a chip (10); a memory controller (54) on the chip (10), as shown in Fig. 2 (col. 4, lines 65-67; col. 5, lines 36-41), in communication with the graphics pipeline (58), operative to transfer pixel data between the pipeline (58) and a memory (col. 6, lines 10-13, 59-66).

However, MacInnis does not teach at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least 2 graphics pipelines operative to process data in dedicated tile (col. 5, lines 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines

312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory that is shared among the at least two graphics pipelines. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically

repeating pattern of square regions because Perego suggests that this parallel processing significantly reduces the processing burden on the memory controller/graphics controller (col. 5, lines 38-46).

12. As per Claim 2, MacInnis does not teaches that the square regions comprise a two dimensional partitioning of memory. However, Perego teaches square regions have two dimensional partitioning of memory (col. 5, lines 19-33). This would be obvious for the reasons given in the rejection for Claim 1.

13. As per Claim 3, MacInnis teaches wherein the memory is a frame buffer (col. 6, line 66-col. 7, line 2).

14. As per Claim 4, MacInnis does not teach that each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data. However, Perego teaches each of at least 2 graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data. Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (col. 5, lines 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to

store data which are referenced during the execution of the programs (col. 1, lines 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (col. 5, lines 19-27; col. 1, lines 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline. This would be obvious for the reasons given in the rejection for Claim 1.

15. As per Claim 7, MacInnis does not teach that the at least two graphics pipelines separately receive the pixel data from the front end circuitry. However, Perego teaches at least two graphics pipelines (312) separately receive pixel data from front end circuitry (308) (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). This would be obvious for the reasons given in the rejection for Claim 1.

16. As per Claim 10, MacInnis does not teach that a first of the at least two graphics pipelines processes the pixel data only in the first set of tiles in the repeating tile pattern. However, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

17. As per Claim 12, MacInnis does not teach that a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern. However, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

18. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (col. 5, lines 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

19. As per Claim 25, Claim 25 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

20. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A).

21. As per Claim 5, MacInnis and Perego are relied on for teachings for Claim 4.

But, MacInnis and Perego do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (col. 8, lines 52-61; col. 9, lines 1-23; col. 6, lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so at each of at least two graphics pipelines includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (col. 9, lines 1-23), as is well-known in the art.

22. As per Claim 18, MacInnis does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the 1st (20A), 2nd (20B), 3rd (20C) and 4th (20N) graphics pipelines (col. 3, lines 22-23; col. 4, lines 9-14; col. 8, lines 56-65; col. 3, lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (col. 2, lines 31-35; col. 8, lines 56-65; col. 9, lines 1-23).

23. As per Claim 24, MacInnis teaches a graphics processing circuit, comprising: front end circuitry (90, Fig. 4) operative to generate pixel data in response to primitive data for a primitive to be rendered (col. 8, lines 49-59); back end circuitry (98), coupled to the front end circuitry (90) (col. 9, lines 15-34), operative to process the pixel data in response to position coordinates (col. 9, lines 35-54). The front end circuitry (90) and the back end circuitry (98) are in the graphics display pipeline (80) (col. 7, lines 55-63), and the graphics display pipeline (80) is equivalent to display engine (58, Fig. 2), which is on graphics chip (10) (col. 4, lines 65-67; col.

5, lines 36-39). A memory controller (54) is also on graphics chip (10) (col. 4, lines 65-67; col. 5, lines 36-39). Therefore, the front end circuitry (90), the back end circuitry (98), and the memory controller (54) are on the chip (10). The memory controller (54) is coupled to the display engine (58) and is operative to transmit and receive the processed pixel data (col. 6, lines 10-13, 59-67; col. 7, lines 1-2). Since the display engine (58) is equivalent to the graphics display pipeline (80) which contains the back end circuitry (98) (col. 6, lines 59-67; col. 7, lines 55-63), the memory controller (54) is coupled to the back end circuitry (98) and is operative to transmit and receive the processed pixel data.

However, MacInnis does not teach first back end circuitry operative to process a first portion of the pixel data; set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; second back end circuitry operative to process a second portion of the pixel data; set of tiles of the repeating tile pattern are to be processed by the second back end circuitry. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (col. 5, lines. 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be

processed by 2nd back end circuitry (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44); and memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel data (col. 3, lines 65-67; col. 4, lines 1-53; col. 5, lines 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip, and so the first back end circuitry and second back end circuitry are on the same chip. Since MacInnis teaches that the front end circuitry, the back end circuitry and the memory controller are on the same chip, this teaching from Perego can be implemented into the device of MacInnis so that the front end circuitry sends pixel data to both the first back end circuitry and the second back end circuitry, and the front end circuitry, the first back end circuitry, the second back end circuitry, and the memory controller are on the same chip. This would be obvious for the reasons given in the rejection for Claim 1.

However, MacInnis and Perego do not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23; col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38). Therefore, by implement this teaching into the device of Perego, front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline. Since Perego teaches graphics pipelines are on the same chip, the teaching from Kelleher can be applied to Perego so that the first scan converter and the second scan converter are also on the same chip. This would be obvious for reasons given in the rejection for Claim 5.

24. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1).

25. As per Claim 6, MacInnis and Perego are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis and Perego do not expressly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner teaches that each tile of the set of tiles further comprises a 16x16 pixel array (col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (col. 11, lines 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

26. As per Claim 17, MacInnis does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches this limitation (col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (col. 6, lines 29-30, 42-51).

27. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

MacInnis and Perego are relied upon for teachings relative to Claim 10.

However, MacInnis and Perego do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (col. 8, line 52-col. 9, line 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled by graphics pipelines (col. 8, lines 52-65; col. 6, lines 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (col. 4, lines 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the reasons given in the rejection for Claim 5.

But, MacInnis, Perego, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (col. 1, lines 46-54).

28. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1), further in view of Kent (US 20030164830A1).

MacInnis, Perego, and Furtner are relied upon for the teachings as discussed above relative to Claim 17. MacInnis teaches data includes polygon (col. 58, lines 50-54). Furtner teaches third and fourth graphics pipelines are on separate chips (col. 6, lines 47-51), as discussed for Claim 17.

But, MacInnis, Perego, and Furtner do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Furtner to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

29. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2).

30. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (col. 5, lines 19-25), which is inherently generated in response to received vertex data. Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines. Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. Perego teaches determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of the at least two graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (col. 5, lines 19-44); and transmitting processed pixels to memory controller 310, at least 2 graphics pipelines share

memory controller (col. 3, line 65-col. 4, line 25; col. 5, lines 31-44) wherein the memory controller transfers pixel data from each of the at least two pipelines, to shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one shared memory. Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39).

31. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (col. 5, lines 19-50).

32. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (col. 5, lines 19-44).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Joni Hsu/
Primary Examiner, Art Unit 2628

Receipt date: 01/25/2010
Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (10-08)
Approved for use through 11/30/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	10459797
Filing Date	2003-06-12
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6750867		2004-06-15	Gibson	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060170690	A1	2006-08-03	Leather	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.7

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.H./

Receipt date: 01/25/2010	Application Number	10459797
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2003-06-12
	First Named Inventor	Mark M. Leather
	Art Unit	2628
	Examiner Name	Joni Hsu
	Attorney Docket Number	00100.02.0053

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Joni Hsu/	Date Considered	04/12/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.H./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	683	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L2	492	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L3	148	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L4	105	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L5	1092	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L6	591	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28

L7	62	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L8	830	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L9	587	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L10	2557	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L11	2097	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L12	463	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L13	349	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28

L14	222	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal $2 and vertical $2 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L15	167	til$3 and repeat$3 with (til$3 pattern $3) same pixel $1 and pattern $3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L16	349	scan adj conver$5 and pixel$1 and til $3 and pipelin $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L17	540	(multiple plurality) same pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L18	206	(multiple plurality) near2 pipelin $3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L19	129	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28

L20	62	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L21	363	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L22	129	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28
L23	167	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/04/12 15:28

EAST Search History (Interference)

< This search history is empty>

4/12/10 3:30:23 PM
C:\Documents and Settings\jhsu\My Documents\10459797a.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	Hsu, Joni	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/29/2008	02/06/2009	07/21/2009	04/12/2010					
	1	✓	✓	✓	✓					
	2	✓	✓	✓	✓					
	3	✓	✓	✓	✓					
	4	✓	✓	✓	✓					
	5	✓	✓	✓	✓					
	6	✓	✓	✓	✓					
	7	✓	✓	✓	✓					
	8	-	-	-	-					
	9	-	-	-	-					
	10	✓	✓	✓	✓					
	11	✓	✓	✓	✓					
	12	✓	✓	✓	✓					
	13	✓	✓	✓	✓					
	14	✓	✓	✓	✓					
	15	✓	✓	✓	✓					
	16	✓	✓	✓	✓					
	17	✓	✓	✓	✓					
	18	✓	✓	✓	✓					
	19	✓	✓	✓	✓					
	20	✓	✓	✓	✓					
	21	✓	✓	✓	✓					
	22	✓	✓	✓	✓					
	23	-	-	-	-					
	24	✓	✓	✓	✓					
	25	✓	✓	✓	✓					
	26	-	-	-	-					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Hsu, Joni	2628

SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	7/21/09	JH
Above	UPDATED	4/12/10	JH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	4/12/10	JH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Doc Code: AP.PRE.REQ

PTO/SB/33 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 00100.02.0053

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on July 22, 2010

Signature /Christine A. Wright/

Typed or printed name Christine A. Wright

Application Number	Filed
10/459,797	June 12, 2003

First Named Inventor: Mark M. Leather et al.

Art Unit	Examiner
2628	Joni Hsu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 34,414.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Christopher J. Reckamp/
Signature

Christopher J. Reckamp
Typed or printed name

312-609-7599
Telephone number

July 22, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mark M. Leather et al.	Examiner:	Joni Hsu
Serial No.:	10/459,797	Art Unit:	2628
Filing Date:	June 12, 2003	Atty. Docket No.:	00100.02.0053
Confirmation No.:	4148		
Title:	**DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**		

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicants respectfully submit that there is clear error since the references do not teach what is alleged.

Claims 1-4, 7, 10, 12, 14, and 25 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. US 6,570,579 (MacInnis et al.) in view of U.S. Patent No. US 6,864,896 (Perego). Claims 1 states, inter alia,

> a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines

Applicants respectfully submit that the Perego reference has been misapprehended, as it does not teach what is alleged and is directed to a different operation and structure from that claimed by Applicants. The final office action alleges on pages 6-7 that:

> Perego teaches…memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines 312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10,48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory that is shared among the at least two graphics pipelines (emphasis added).

The final office action further alleges on page 4 that:

> Perego describes "The shared memory 314 typically includes multiple memory devices coupled together to form a block of storage space" (col. 4, lines 8-10). Thus, the block of storage space is considered to be a memory shared among the two graphics pipelines (emphasis added).

Applicants respectfully submit that the final office action misinterprets the term "shared memory" as used by Perego. As best understood by Applicants, the final office action interprets the term "shared memory" as memory shared between graphics pipelines. However, Perego defines "shared memory" as memory devices partitioned for use as both "main memory" and "graphics memory", not as memory shared between two or more graphics pipelines. Furthermore, "main memory" is described as memory used only by the CPU, not memory used for graphics. Perego states:

> Each memory module 304 includes a rendering engine 312 and a shared memory 314 (i.e., main memory and graphics memory). The main memory typically contains instructions and/or data used by the CPU. The graphics memory typically contains instructions and/or data used to process, render, or otherwise handle graphical images or graphical information. (column 4, lines 1-6; emphasis added)

Perego uses the term "shared memory" because a portion of the memory on each memory module is used by the CPU while the remainder is used as graphics memory. In other words, the physical memory devices are "shared" between the CPU and a rendering engine. However, the memory used for graphics processing is separate from the memory used by the CPU. Perego explicitly states that, "the graphics memory is statically or dynamically partitioned off from the main memory pool" (column 1, lines 46-47; emphasis added).

Additionally, Applicants respectfully submit that at no point does Perego teach that multiple rendering engines (alleged by the final office action to teach Applicants' multiple graphics pipelines) access the same memory. In fact, Perego teaches each rendering engine as having separate, dedicated memory. Perego's FIG. 8 (reproduced below) shows two separate rendering engines (802 and 810), each associated with their own dedicated group of memory devices (memory devices 804 and 812, respectively) using distinct memory interconnects (806 and 814, respectively). These separate groups of memory are each comprised of multiple memory devices that are coupled together into separate discrete blocks of storage.

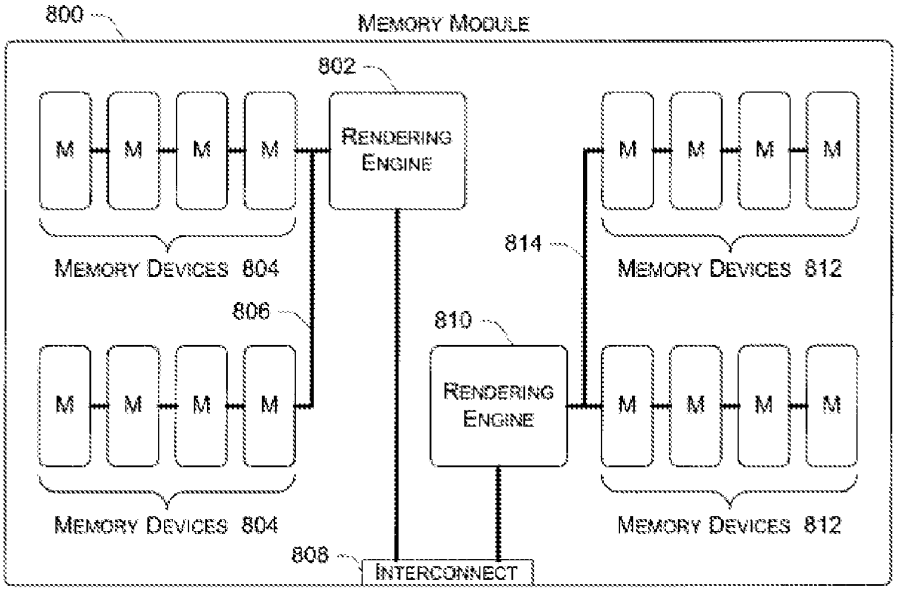


Fig. 8

Additionally or alternatively, Applicants respectfully submit that Perego teaches away from Applicants' claimed design where a single memory controller shares a single memory between multiple graphics pipelines. Perego explicitly states the advantages of having distinct memory devices tied to individual rendering engines:

> The architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to the various rendering engines 312, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory modules 304. Thus, the partitioning of memory among multiple memory modules 304 improves graphical data throughput relative to systems in which a single graphics controller performs all processing tasks and reduces bandwidth contention with the CPU. This bandwidth reduction occurs because the primitive commands typically contain significantly less data than the amount of data referenced when rendering the primitive. Additionally, the system partitioning described allows aggregate bandwidth between the rendering engines and the memory devices to be much higher than the bandwidth between the controller and memory modules. Thus, effective system bandwidth is increased for processing graphics tasks (column 4, lines 47-65; emphasis added).

In other words, bandwidth is increased by having each distinct rendering engine utilize its own dedicated memory present on the same memory module as the rendering engine. Assuming for the sake of argument that Perego did share graphics memory between rendering engines, no bandwidth gain would be attained as graphics data would necessarily be transferred through the memory/graphics controller to another memory module – exactly the scenario Perego seeks to avoid. Perego places rendering engines on memory modules specifically to prevent the bottleneck created by passing data through the memory controller during parallel processing.

Claims 20-22 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. US 6,864,896 (Perego). Applicants respectfully submit that the Perego reference has been misapprehended and it is directed to a different operation and structure from that claimed by Applicants. The final office action states on page 18 that:

> Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines (emphasis added).

In claim 20, inter alia, Applicants specifically require:

> passing the same pixel data to both of the at least two graphics pipelines on a same chip; (emphasis added)

Applicants respectfully submit Perego does not teach transferring the same pixel data to two or more graphics pipelines. Applicants' FIG. 2 discloses that front end circuitry 35 passes identical pixel data 36 to two separate graphics pipelines (pipeline A comprised of scan converter 37 and back end circuitry 38; pipeline B comprised of scan converter 40 and back end circuitry 42) located on the same chip. In sharp contrast thereto, Perego specifically teaches each separate rendering engine receiving distinct and different pixel data. Perego states:

> The memory controller/graphics controller partitions the processing task into multiple portions (block 404) and distributes each portion of the processing task to a rendering engine on a memory module (block 406). (column 5, lines 3-6; emphasis added)

Applicants respectfully submit that Perego teaches that each rendering engine receives only the specific portion the processing task that it is responsible for processing. The memory controller/graphics controller is responsible for dividing the processing task into discrete portions, so that each rendering engine can process its portion of the data independently and in

parallel. Perego's FIG. 8 (reproduced above) shows that each rendering engine (802 and 810) on a memory module has a separate connection to the memory module interconnect, and thus to the memory controller – thereby allowing for each rendering engine to receive only the data it will process. As such, Perego does not teach multiple rendering engines receiving identical pixel data as required Applicants' above claim language.

For the above reasons and due to the presence of additional clear error, reconsideration and withdrawal of the rejection of the claims is respectfully requested and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Date: July 22, 2010

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	1401	1	540	540
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**540**

Electronic Acknowledgement Receipt	
EFS ID:	8068102
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	22-JUL-2010
Filing Date:	12-JUN-2003
Time Stamp:	12:48:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$540
RAM confirmation Number	10456
Deposit Account	220259
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Notice of Appeal Filed	10459797_NoticeofAppeal.pdf	42367 cd42081ea2e8da846de182c13837c638b354fc33	no	1
Warnings:					
Information:					
2	Pre-Brief Conference request	10459797_PreAppealRequest.pdf	38502 9a02afc05045c98e603107cceefcd01e3c5843ca	no	1
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	10459797_Remarks.pdf	56276 58d197634bf417339d8cce6ceca8ae9b06a702f2	no	5
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	29870 9fcf06999259f6cca3a4aa7fd7b14369bc291953	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	167015		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/31 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): 00100.02.0053

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on July 22, 2010

Signature: /Christine A. Wright/

Typed or printed name: Christine A. Wright

In re Application of: Mark M. Leather et al.

Application Number	Filed
10/459,797	June 12, 2003

For: DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE

Art Unit	Examiner
2628	Joni Hsu

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 540.00

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 22-0259 .

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record. Registration number 34,414.

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

/Christopher J. Reckamp/
Signature

Christopher J. Reckamp
Typed or printed name

312-609-7599
Telephone number

July 22, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 07/30/2010

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
07/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application/Control No.	Applicant(s)/Patent under Reexamination
	10/459,797	LEATHER ET AL.
	JONI HSU	Art Unit: 2628

This is in response to the Pre-Appeal Brief Request for Review filed 22 July 2010.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: *1-7, 10-22, 24, 25*.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *Joni Hsu*. (3)*Xiao Wu*.

(2) *Kee Tung*. (4)_____.

/Joni Hsu/	/Kee M Tung/	/XIAO M. WU/
Primary Examiner, Art Unit 2628	Supervisory Patent Examiner, Art Unit 2628	Supervisory Patent Examiner, Art Unit 2628

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Mark M. Leather et al.	Examiner: Joni Hsu
Application No.: 10/459,797	Group Art Unit: 2628
Filed: June 12, 2003	Docket No.: 00100.02.0053
For: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**	

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Sir:

Appellants submit this brief further to the Pre-Appeal Brief Request for Review filed July 22, 2010, and the Notice of Panel Decision from Pre-Appeal Brief Review dated July 30, 2010 in the above-identified application. Appellants petition for a four month extension of time.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

ATI Technologies ULC is the real party in interest in this appeal by virtue of an executed assignment from the named inventors of their entire interest to ATI International, SRL and an executed name change. The assignment evincing such ownership interest was recorded on June 12, 2003, in the United States Patent and Trademark Office at Reel 014176, Frame 0613. The Name Change was recorded on December 30, 2010, in the United States Patent and Trademark Office at Reel 025573, Frame 0443.

II. RELATED APPEALS AND INTERFERENCES

To Appellants' knowledge, there are no related Appeals or Interferences filed, pending, or decided.

III. STATUS OF CLAIMS

Claims 1-7, 10-22, 24 and 25 are pending. Claims 1-7, 10-22, 24 and 25 stand rejected. The originally filed Application contained claims 1-24. Claims 25 and 26 were added during prosecution of the present application. Claims 8, 9, 23 and 26 were canceled during prosecution of the present application. Claims 1, 10, 12, 13, 20, 24 and 25 were amended during prosecution of the present application. Claims 1-7, 10-22, 24 and 25 are being appealed. Of the pending appealed claims, 1, 20, 24 and 25 are independent.

IV. STATUS OF AMENDMENTS

A Pre-Appeal Brief Request for Review was filed on July 22, 2010, in response to the Final Office Action mailed on April 22, 2010. No amendments were made to the claims, however, subsequent to the Final Office Action. The claims listed in Appendix A reflect the claims as they stood at the time the Final Office Action was mailed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Computer graphics systems, set top box systems or other graphics processing systems typically include a host processor, graphics (including video) processing circuitry, memory (e.g. frame buffer), and one or more display devices. The host processor may have a graphics application running thereon, which provides vertex data for a primitive (e.g. triangle) to be rendered on the one or more display devices to the graphics processing circuitry. The display device, for example, a CRT display includes a plurality of scan lines comprised of a series of pixels. When appearance attributes (e.g. color, brightness, texture) are applied to the pixels, an object or scene is presented on the display device. The graphics processing circuitry receives the vertex data and generates pixel data including the appearance attributes which may be presented on the display device according to a particular protocol. The pixel data is typically stored in the frame buffer in a manner that corresponds to the pixels location on the display device (at least ¶ 0003).

In a conventional display device, a screen may be partitioned into a series of vertical strips. The strips are typically 1-4 pixels in width. In like manner, the frame buffer of conventional graphics processing systems is partitioned into a series of vertical strips having the same screen space width. Alternatively, the frame buffer and the display device may be partitioned into a series of horizontal strips. Graphics calculations, for example, lighting, color, texture and user viewing information are performed by the graphics processing circuitry on each of the primitives provided by the host. Once all calculations have been performed on the primitives, the pixel data representing the object to be displayed is written into the frame buffer. Once the graphics calculations have been repeated for all primitives associated with a specific frame, the data stored in the frame buffer is rendered to create a video signal that is provided to the display device (at least ¶ 0004).

The amount of time taken for an entire frame of information to be calculated and provided to the frame buffer becomes a bottleneck in graphics systems as the calculations associated with the graphics become more complicated. Contributing to the increased complexity of the graphics calculation is the increased need for higher resolution video, as well as the need for more complicated video, such as 3-D video. The video image observed by the human eye becomes distorted or choppy when the amount of time taken to render an entire frame of video exceeds the amount of time in which the display device must be refreshed with a new graphic or frame in order to avoid perception by the human eye. To decrease processing time, graphics processing systems typically divide primitive processing among several graphics processing circuits where, for example, one graphics processing circuit is responsible for one vertical strip of the frame while another graphics processing circuit is responsible for another vertical strip of the frame. In this manner, the pixel data is provided to the frame buffer within the required refresh time (at least ¶ 0005).

Load balancing is a significant drawback associated with the partitioning systems as described above. Load balancing problems occur, for example, when all of the primitives of a particular object or scene are located in one strip. When this occurs, only the graphics processing circuit responsible strip 13 is actively processing primitives; the remaining graphics processing circuits are idle. This results in a significant waste of computing resources as at most only half of the graphics processing circuits are operating. Consequently, graphics processing system performance is decreased as the system is only operating at a maximum of fifty percent capacity (at least ¶ 0006).

In contrast, according to an aspect of Appellants' present disclosure, the same frame buffer is shared among multiple pipelines that are on a single chip. The shared frame buffer is

configured such that the primitive data is written in the tiles being processed by the first graphics pipeline and the tiles being processed by the second graphics pipeline will be substantially equal in size, notwithstanding the primitive orientation. Thus, the amount of processing performed by the first graphics pipeline and the second graphics pipeline, respectively, are substantially equal; thereby, effectively eliminating the load balance problems exhibited by conventional techniques (at least ¶ 0030).

As to independent claim 1 and also referring to FIGs. 2 and 3, reproduced below for convenience,

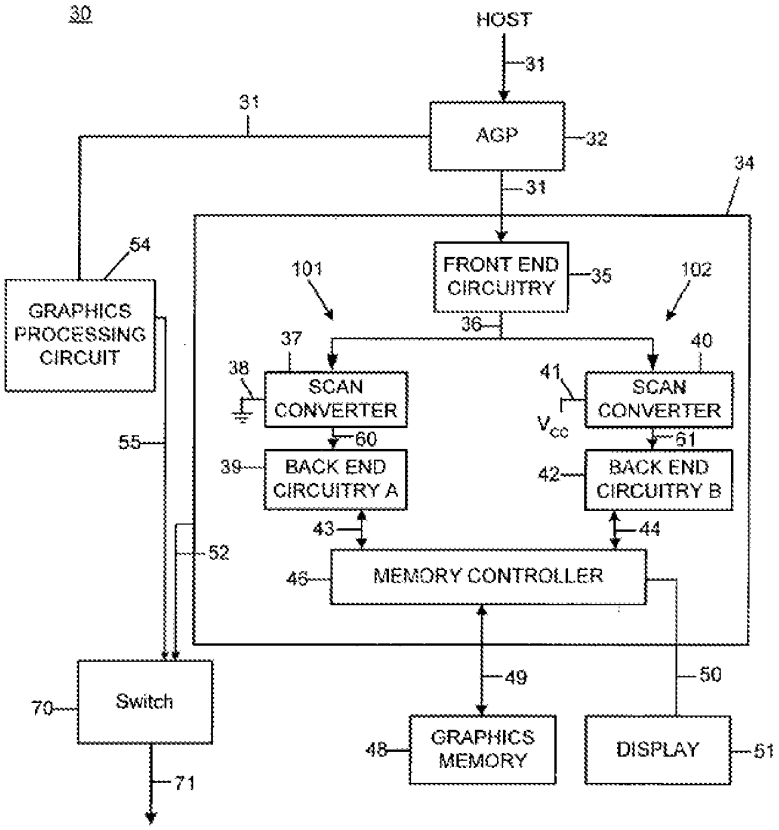


FIG. 2

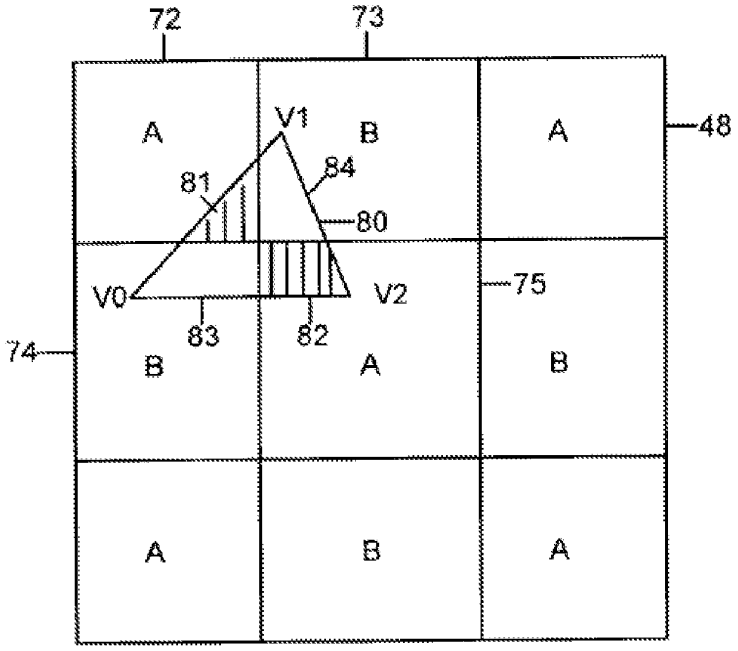


FIG. 3

a graphics processing circuit (34), including at least two graphics pipelines (102, 102) on a same chip are operative to process data in a corresponding set of tiles (72, 73 respectively) of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines are operative to process data in a dedicated tile. The graphics processing circuit 34 also includes a memory controller 46 on the chip in communication with the at least two graphics pipelines (101, 102), and is operative to transfer pixel data (43, 44) between each of a first pipeline and a second pipeline and a memory (48) shared among the at least two graphics pipelines (101, 102), wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions (FIG. 2, FIG. 3, at least ¶¶ 0018-0030).

Dependent claim 4 is directed to the graphics processing circuit (34), wherein each of the at least two graphics pipelines (101, 102) further includes front end circuitry (35) (at least ¶¶

0022, 0023) operative to receive vertex data (31) and generate pixel data (e.g., 36) corresponding to a primitive to be rendered, and back end circuitry (39, 42), coupled to the front end circuitry, operative to receive and process a portion of the pixel data (at least ¶¶ 0022, 0025, 0027).

Dependent claim 5 is directed to the graphics processing circuit, wherein each of the at least two graphics pipelines further includes a scan converter (37, 40), coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry (at least ¶¶ 0024-0026).

Dependent claim 11 is directed to the graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines (101) further includes a scan converter (37), coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry (39), the scan converter (37) including a pixel identification line for receiving tile identification data (38, 41) indicating which of the set of tiles is to be processed by the back end circuitry (at least ¶¶ 0022-0026).

Dependent claim 13 is directed to the graphics processing circuit, wherein the second of the at least two graphics pipelines (102) further includes a scan converter (40), coupled to front end circuitry and back end circuitry (42), operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data (41) indicating which of the set of tiles is to be processed by the back end circuitry (at least ¶¶ 0022-0026).

Dependent claim 14 is directed to a third graphics pipeline (201) and a fourth graphics pipeline (202), wherein the third graphics pipeline includes front end circuitry (135) operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back

end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern (FIG. 2, FIG. 5, at least ¶¶ 0031-0035).

Dependent claim 15 is directed to a graphics processing circuit, wherein the third graphics pipeline (201) further includes a scan converter (137), coupled to the front end circuitry (135) and the back end circuitry (139), operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry (139), the scan converter (137) including a pixel identification line for receiving tile identification data (138) indicating which of the sets of tiles is to be processed by the back end circuitry (FIG. 5, at least ¶¶ 0022-0026, 0037-0039).

Dependent claim 16 is directed to a graphics processing circuit, wherein the fourth graphics pipeline (202) further includes a scan converter (140), coupled to the front end circuitry (135) and the back end circuitry (142), operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data (141) indicating which of the sets of tiles is to be processed by the back end circuitry. (Fig. 5 at least ¶¶ 0032-0039)

Dependent claim 19 is directed to a graphics processing circuit wherein the data includes a polygon and wherein each separate chip creates a bounding box (Fig. 7) around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated

with a separate chip, then the processing circuit rejects the whole polygon and processes a next one. (Fig. 3, Fig. 7, Fig. 8, at least ¶¶0049-0051)

Independent claim 20 is directed to a graphics processing method, including receiving vertex data for a primitive to be rendered (100), generating pixel data in response to the vertex data (102), passing the same pixel data to both of the at least two graphics pipelines on a same chip, determining the pixels within a set of tiles (72, 73) of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of the at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions (Fig. 3), performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines (108), and transmitting the processed pixels to a memory controller (146), wherein the at least two graphics pipelines share the memory controller wherein the memory controller transfers pixel data from each of the at least two pipelines, to a shared memory. (Fig. 6, at least ¶¶ 0040-0045, 0027-0030)

Independent claim 24 is directed to a graphics processing circuit (34), including front end circuitry (35) on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered, first back end circuitry (39) on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates, a first scan converter (37) on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data, second back end circuitry (42) on the

chip, coupled to the front end circuitry (35), operative to process a second portion of the pixel data in response to position coordinates, a second scan converter (42) on the chip, coupled between the front end circuitry (35) and the second back end circuitry (42), operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data, and a memory controller (146) on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data. (Fig. 2, at least ¶¶0018-0030)

Independent claim 25 is directed to a graphics processing circuit (34), including at least two graphics pipelines (101,102) on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions, wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels; and a memory controller (46) on the chip, coupled to the at least two graphics pipelines on the chip and operative to transfer pixel data between each of the two graphics pipelines and a memory (48) shared among the at least two graphics pipelines. ((FIG. 2, FIG. 3, at least ¶¶ 0018-0030).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 7, 10, 12, 14 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego).

Claims 5, 18 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 5,794,016 (Kelleher).

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 6,778,177 (Furtner).

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 5,794,016 (Kelleher), further in view of U.S. Patent No. 5,905,506 (Hamburg).

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 6,778,177 (Furtner), further in view of U.S. Publication No. 2003/0164830 (Kent).

Claims 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,864,896 (Perego).

VI. ARGUMENT

The references and claim language cannot be mischaracterized in an effort to render a claim unpatentable (See e.g., *In Re Rouffet*, 149 F. 3d. 1350, 47 USPQ 2d 1453 (Fed. Circ. 1998, *In Re Fine*, 837 F.2d 1071)). Claims cannot be interpreted in a vacuum but must be *reasonably* interpreted in light of the specification as it would be interpreted by one of ordinary skill in the art. *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (en banc) (Fed. Cir. 2005). (see also MPEP 2111 and cited cases incorporated by reference herein). Claims must be interpreted to be consistent with the claims themselves and with the Specification. Also, if a reference does not teach what is alleged, a prima facie case has not been made. (See MPEP sections 2142-2144 and cited cases incorporated by reference herein). *Graham v John Deere Co.*, 383 U.S. 1 (1966), (see also, *KSR International Co. v. Teleflex Inc. et al.,* 127 S. Ct. 1727 (2007). For one or more of these reasons the rejections must be reversed and the claims should be allowed.

1. THE PEREGO REFERENCE DOES NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103 REJECTION OF CLAIMS 1-7, 10-22, 24 AND 25 MUST BE REVERSED

Claims 1-4, 7, 10, 12, 14 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego). MacInnis is a conventional graphics processing circuit that includes a single pipeline and corresponding memory controller on chip. It is admitted that MacInnis does not teach at least two graphics pipelines on a same chip that process data in a corresponding set of tiles for a repeating tile pattern corresponding to screen locations. Nor does it teach a plurality of graphics pipelines and associated memory controller on the same chip in communication with the at least two graphics pipelines wherein the memory controller transfers pixel data between each of the two pipelines and a memory that is shared among the at least two graphic on chip pipelines. The office action alleges that Perego teaches this subject matter.

Perego is directed to a scalable unified CPU and graphics memory architecture and employs independent groups of memory modules 304 that are coupled to a memory controller/graphics controller (col. 3, lns. 63-67). Perego describes each memory module 304 as including a rendering engine 312 and a dedicated corresponding shared memory 314 such that shared memory 314 is shared between a CPU and the rendering engine 312. As described by Perego, the shared memory may be made up of multiple memory devices however, the shared memory 314 is still only shared between the rendering engine on the particular memory module and the CPU. The shared memory of Perego is not shared between multiple rendering engines on different modules or shared between multiple rendering engines on a single module.

Claims 1 states, inter alia,

> a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines

As claimed, the shared memory is shared among at least two graphics pipelines on the same chip. Appellants respectfully submit that the Perego reference has been misapprehended, as it does not teach what is alleged and is directed to a different operation and structure from that claimed by Appellants. The Perego teachings instead describe main memory of a CPU that is shared with a single graphics pipeline. Multiple pipelines in Perego do not share the same graphics memory. The final office action alleges on pages 6-7 that:

> Perego teaches…memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines 312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10,48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory that is shared among the at least two graphics pipelines (emphasis added).

The final office action further alleges on page 4 that:

> Perego describes "The shared memory 314 typically includes multiple memory devices coupled together to form a block of storage space" (col. 4, lines 8-10). Thus, the block of storage space is considered to be a memory shared among the two graphics pipelines (emphasis added).

Appellants respectfully submit that the final office action misinterprets the term "shared memory" as used by Perego. As best understood by Appellants, the final office action interprets the term "shared memory" as memory shared between graphics pipelines. However, Perego instead defines "shared memory" as memory devices partitioned for use as both CPU "main memory" and "graphics memory", not as memory shared between two or more graphics pipelines. Furthermore, "main memory" is described as memory used only by the CPU, not memory used for graphics. Perego states:

> Each memory module 304 includes a rendering engine 312 and a shared memory 314 (i.e., main memory and graphics memory). The main memory typically contains instructions and/or data used by the CPU. The graphics memory typically contains instructions and/or data used to process, render, or otherwise handle graphical images or graphical information. (column 4, lines 1-6; emphasis added)

Perego uses the term "shared memory" because a portion of the memory on each separate memory module is used by the CPU while the remainder is used as graphics memory. In other words, the physical memory devices are "shared" between the CPU and a rendering engine. However, the memory used for graphics processing is separate from the memory used by the CPU. Perego explicitly states that, "the graphics memory is statically or dynamically partitioned off from the main memory pool" (column 1, lines 46-47; emphasis added).

Additionally, Appellants respectfully submit that at no point does Perego teach that multiple rendering engines (alleged by the final office action to teach Appellants' multiple graphics pipelines) access the same memory. In fact, Perego teaches each rendering engine as having separate, dedicated memory. Perego's FIG. 8 (reproduced below) shows two separate rendering engines (802 and 810), each associated with their own dedicated group of memory

devices (memory devices 804 and 812, respectively) using distinct memory interconnects (806 and 814, respectively). These separate groups of memory are each comprised of multiple memory devices that are coupled together into separate discrete blocks of storage.

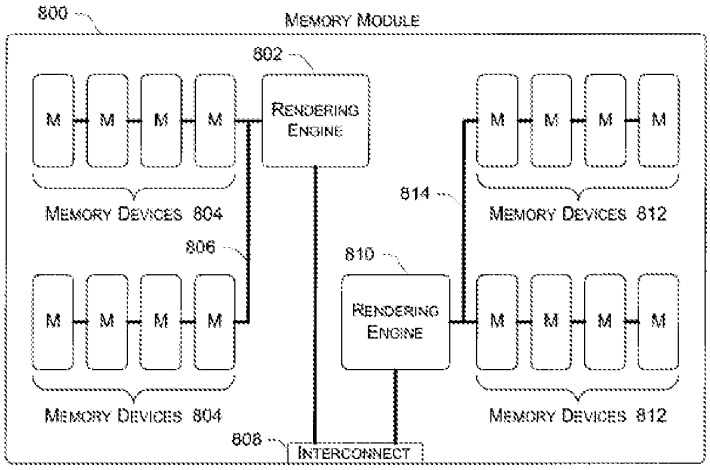


Fig. 8

Additionally or alternatively, Appellants respectfully submit that Perego teaches away from Appellants' claimed design where a single memory controller shares a single memory between multiple graphics pipelines. Perego explicitly states the advantages of having distinct memory devices tied to individual rendering engines:

> The architecture of FIG. 3 allows the memory controller/graphics controller 310 to issue high level primitive commands to the various rendering engines 312, thereby reducing the volume or bandwidth of data that must be communicated between the controller 310 and the memory modules 304. Thus, the partitioning of memory among multiple memory modules 304 improves graphical data throughput relative to systems in which a single graphics controller performs all processing tasks and reduces bandwidth contention with the CPU. This bandwidth reduction occurs because the primitive commands typically contain significantly less data than the amount of data referenced when rendering the primitive. Additionally, the system partitioning described allows aggregate bandwidth between the rendering engines and the memory devices to be much higher than the bandwidth between the controller and memory modules. Thus, effective system bandwidth is increased for processing graphics tasks (column 4, lines 47-65; emphasis added).

In other words, bandwidth is increased by having each distinct rendering engine utilize its own dedicated memory present on the same memory module as the rendering engine. Assuming for the sake of argument that Perego did share graphics memory between rendering engines, no bandwidth gain would be attained as graphics data would necessarily be transferred through the memory/graphics controller to another memory module – exactly the scenario Perego seeks to avoid. Perego places rendering engines on separate memory modules specifically to prevent the bottleneck created by passing data through the memory controller during parallel processing. Accordingly, Perego does not teach the claimed subject matter and the rejection should be reversed.

As to independent claim 25, the Examiner rejected this claim for the same reasons as claim 1 as being similar in scope and rejected it by stating that it is "rejected under the same rationale" as claim 1 (final action, page 10). Accordingly, Appellants respectfully reassert the relevant remarks made with respect to claim 1. The rejection should be reversed for the same reasons as to claim 1.

Dependent claims 2 and 3 for purposes of this Appeal only, stand or fall together with independent claim 1.

As per dependent claim 4, the claim requires that each of the graphics pipelines each further include front end circuitry that receive vertex data and generate pixel data corresponding to the primitive to be rendered, and back end circuitry, coupled to the front end circuitry operative to receive and process a portion of the pixel data. The final rejection cites Perego as allegedly teaching pipeline front end circuitry as being element 308 in FIG. 3. The office action cites col. 3, ln. 64 to col. 4, ln. 2; col. 5, lns. 19-44. However as shown below and reproduced FIG. 3, element 308 is actually a "CPU" and is not a pixel pipeline which the Examiner has

already asserted is actually graphics pipeline 312 in the rejection of claim 1. Appellants respectfully submit that it is logically impossible to have the CPU 308 as described in Perego as being separate from rendering engine 312 as actually being in rendering engine 312 as alleged by the Examiner. For example, plugging in Examiner's contention that the rendering engine 312 in Perego (as set forth in the rejection of claim 1) corresponds to the claimed graphics pipelines and substituting element 308 as allegedly corresponding to the claimed front end circuitry, such a substitution results in an allegation that Perego teaches that the rendering engine 312 contains the CPU 308 since the claim requires that each of the graphics pipeline include the front end circuitry. Perego clearly does not teach that the CPU is part of the rendering engine 312 and actually requires that they be separate processors. Accordingly, Appellants respectfully submit that the rejection must be reversed.

It is also alleged as to claim 4 that the "CPU is operative to…generate pixel data corresponding to a primitive to be rendered (col. 5, lns. 19-27; col. 1, lns. 18-21)" (page 9 of final rejection). However, the cited portions do not describe what is alleged since the CPU in Perego does not generate pixel data. To the contrary, the cited portion instead states as is well known in the art, that CPUs may sort primitive data which may be then submitted to, for example, the rendering pipeline. The CPU does not generate pixel data as alleged, since the rendering engine must generate pixel data. Also, the citation as to col. 1 also fails to describe the CPU generating any pixel data corresponding to a primitive to be rendered. Since the reference does not teach what is alleged, Appellants respectfully submit that the rejection must be reversed.

As to dependent claim 7, this claim depends on claim 4 and as such, the rejection must be reversed with respect to this claim as well for the reasons given above with respect to claim 4. In addition, the rejection uses the same logical error with respect to claim 4 alleging that the

claimed front end circuitry that is coupled to the graphics pipeline is the CPU 308, as noted above with respect to claim 4 the graphics pipelines must include front end circuitry as claimed, however element 308 is actually a CPU in Perego and is not part of a graphics pipeline and is not front end circuitry. Accordingly, Appellants respectfully submit that the rejection must be reversed.

As to dependent claim 10, Appellants respectfully submit for purposes of this Appeal only, that the rejection of this claim should be reversed for one or more reasons above given with respect to the claims from which it depends.

As to dependent claim 12, Appellants respectfully submit for purposes of this Appeal only, that this claim stands or falls with respect to independent claim 1.

As to dependent claim 14, this claim is similar to that of claim 4 with respect to each of the third and fourth graphics pipelines include front end circuitry operative to receive vertex data and to generate pixel data corresponding to a primitive to be rendered. The Examiner used the same reasoning as to claim 4, according, Appellants respectfully reassert the relevant remarks made above with respect to claim 4 since the CPU of Perego is not in the rendering engine of Perego and therefore the reference does not teach what is alleged by the Examiner and does not teach the claimed subject matter and accordingly, the rejection must be reversed.

2. THE REFERENCES DO NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103(A) REJECTION OF CLAIMS 5, 18 AND 24 MUST BE REVERSED

Claims 5, 18 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 5,794,016 (Kelleher). Claim 5 depends on claim 4 and hence the rejection must be reversed for at least the reasons given above with respect to claim 4.

As to claim 18, this claim depends on claim 14 and the rejection must be reversed for at least the same reasons provided above with respect to claim 14 and/or claim 1.

As to independent claim 24, it is alleged that Perego teaches "that two graphics pipelines are the same chip, and so the front end circuitry, first back end circuitry, and second back end circuitry on the same chip." (office action, page 14) referring to FIG. 8. However, Perego does not teach nor does not contemplate both front and back end circuitry on the chip both coupled to the same front end circuitry as claimed. In fact, FIG. 8 actually shows separate front end circuitry being employed since separate rendering engines 802 and 810 are employed and each of these are identical in structure. There is no teaching or suggestion in Perego as alleged and as such, the rejection should be withdrawn.

3. THE REFERENCES DO NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103(A) REJECTION OF CLAIMS 6 AND 17 MUST BE REVERSED

Claims 6 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 6,778,177 (Furtner). The rejection as to Claims 6 and 7, for purposes of this Appeal, should be reversed for one or more reasons given above with respect to claims from which they depend.

4. THE REFERENCES DO NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103(A) REJECTION OF CLAIMS 11, 13, 15 AND 16 MUST BE REVERSED

Claims 11, 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 5,794,016 (Kelleher), further in view of U.S. Patent No.

5,905,506 (Hamburg). As to claim 11, this rejection must be reversed for one or more of the above reasons with respect to one or more of the claims from which this claim depends.

In addition or alternatively, Appellants respectfully submit that the rejection must also be reversed because the claim language is being ignored and since the cited reference does not teach what is alleged. As required by the claim, the scan converter is unique in that it is required to include a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry (see for example, ¶ 0026 of Appellants' Specification). In this embodiment, each scan converter may be, for example, hard wired or programmably set to be dedicated to a particular tile and as claimed. It will only process or determine those pixels with a primitive that are within a portion of a triangle that are within a particular tile. (See FIG. 3). Accordingly, the scan converter is set based on tile identification data indicating which of the set of tiles is to be processed by the corresponding back end circuitry.

Hamburg is alleged to teach a pixel identification line for receiving the tile identification data indicating which tiles are to be processed but the office action omits critical language because the claim requires that the claimed tile identification data and the claimed scan converter utilizes the tile identification data to indicate which sets of tiles are to be processed by the back end circuitry. The Hamburg reference is directed to a system post-pixel rendering whereas Appellants are actually claiming a scan converter and back end circuitry used to generate pixels whereas Hamburg describes a system where pixels are already generated and then undergo a copy operation from one tile to another tile. As such, the tile identification data described in the cited portion of Hamburg, namely col. 5, lns. 35-52, do not designate any back end circuitry of any kind but instead merely indicate that a pixel may be copied from one tile to another tile after

it has already been rendered. Accordingly, one of ordinary skill in the art would understand Hamburg as teaching utilizing a tile ID and the location with the tile in which to write a pixel value for a copy operation and for a new pixel value is into a particular pixel location. The reasoning given for utilizing Hamburg by the Examiner is that this would allow easily tracking of storage locations of tile pixel data and to be able to easily retrieve data for a particular image tile. This reasoning however is irrelevant to the claimed subject matter which is actually dealing with a different operation namely pixel generation using scan converter and back end circuitry whereas the alleged motivation deals with tracking storage locations of already generated pixel data and retrieving already generated pixel data. Hamburg teaches a post-pipeline operation. Accordingly, Appellants respectfully submit that the rejection should be reversed.

As to claim 13, this claim includes similar language as that in claim 11. Accordingly, Appellants respectfully reassert the relevant remarks made above and accordingly, this rejection should also be reversed for the same reasons.

Claims 15 and 16 have been rejected under similar rationale as claim 11. Accordingly, Appellants respectfully reassert the relevant remarks made above respect to claim 11 and for the same reasons the rejections as to these dependent claims should also be reversed.

5. THE REFERENCES DO NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103(A) REJECTION OF CLAIM 19 MUST BE REVERSED

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,570,579 (MacInnis) in view of U.S. Patent No. 6,864,896 (Perego), further in view of U.S. Patent No. 6,778,177 (Furtner), further in view of U.S. Publication No. 2003/0164830 (Kent).

Appellants respectfully submit that the rejection must be reversed for one or more of the reasons given above with respect to claims from which this claim depends.

In addition, or alternatively, the claim requires, inter alia, that each separate chip creates a bounding box around the polygon and each corner of the bounding box is checked against a super tile that belongs to each separate chip. If the bounding box does not overlap any of the super tiles associated with a separate chip, then the graphics processing circuit rejects the whole polygon and processes the next one. As set forth, for example, in ¶ 0050 and elsewhere in Appellants' Specification, in one example the polygons coming from an application are all broadcast to all chips. Each chip processes the vertices as needed to generate the same x, y coordinates for all vertices. Then each chip creates a bounding box around the polygon (see FIG. 7). The x, y coordinates of each corner of the bounding box is checked against the super tiles that belong to that processor. Checking the corners of the bounding box against a processor's super tiles is a quick way of determining whether a processor should render some or the entire polygon. If the bounding box overlaps a super tile assigned to a given processor, then the processor renders some or all of the polygon. The setup unit then sends the whole polygon to the various raster pipes. If the bounding box does not overlap any of the tiles associated with a processor, then the setup unit rejects the whole polygon and processes the next one. In this manner, triangle setup performance may not scale with each processor since all polygons go through all setup units, but fill rate which is the number of pixels that are output in total, does scale with each processor added.

It is alleged that Kent teaches the claimed operation of calculating a bounding box of primitives and testing it against the corners and wherein the corners are checked against a super tile that belongs to a particular graphics pipeline. Appellants respectfully submit that the cited teaching in Kent instead is a per pixel based center point comparison using antialiased points as set forth in ¶ 0144 of Kent. Kent's teaching does not use corner testing against super tiles

associated with different pipelines but instead uses a per point radius calculation. As stated in Kent the distance from each subpixel sample point in a point's bounding box to a point center is calculated and compared this to the point's radius. (paragraph 0144 of Kent). Accordingly, as best understood, Kent describes a method where every subpixel sample point is evaluated in comparison to a bounding box from the point's center and compared to the point's radius which is a time consuming and costly operation. Moreover, this is done to determine which subsample points do not contribute to a pixel's coverage. Appellants claim a different operation wherein the corners of a bounding box is checked against a super tile to determine if the bounding box overlaps any of the super tiles associated with the chip. No super tile level comparison is described in Kent nor is a bounding box corner approach described in Kent. Accordingly, Appellants respectfully submit that the reference does not teach what is alleged and does not teach the claimed subject matter. Accordingly, the rejection must be reversed.

6. THE PEREGO REFERENCE DOES NOT TEACH WHAT IS ALLEGED THEREFORE THE 35 U.S.C. § 103(A) REJECTION OF CLAIMS 20-22 MUST BE REVERSED

Claims 20-22 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. US 6,864,896 (Perego). Appellants respectfully submit that the Perego reference has been misapprehended and it is directed to a different operation and structure from that claimed by Appellants. The final office action states on page 18 that:

> Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines (emphasis added).
>
> In claim 20, inter alia, Appellants specifically require:
>
> passing the same pixel data to both of the at least two graphics pipelines on a same chip; (emphasis added).

Appellants respectfully submit Perego does not teach transferring the same pixel data to two or more graphics pipelines. Appellants' FIG. 2 discloses that front end circuitry 35 passes identical pixel data 36 to two separate graphics pipelines (pipeline A comprised of scan converter 37 and back end circuitry 38; pipeline B comprised of scan converter 40 and back end circuitry 42) located on the same chip. In sharp contrast thereto, Perego specifically teaches each separate rendering engine receiving distinct and different pixel data. Perego states:

> The memory controller/graphics controller partitions the processing task into multiple portions (block 404) and distributes each portion of the processing task to a rendering engine on a memory module (block 406). (column 5, lines 3-6; emphasis added)

Appellants respectfully submit that Perego teaches that each rendering engine receives only the specific portion of the processing task that it is responsible for processing. The memory controller/graphics controller is responsible for dividing the processing task into discrete portions, so that each rendering engine can process its portion of the data independently and in parallel. Perego's FIG. 8 (reproduced above) shows that each rendering engine (802 and 810) on a memory module has a separate connection to the memory module interconnect, and thus to the memory controller – thereby allowing for each rendering engine to receive only the data it will process. As such, Perego does not teach multiple rendering engines receiving identical pixel data as required Appellants' above claim language. Therefore, the rejection must be reversed.

The rejection as to Claims 21 and 22 must also be reversed for the reasons given above with respect to Claim 20.

VII. CONCLUSION

For the reasons advanced above, Appellants submit that the Examiner erred in rejecting pending claims 1-7, 10-22, 24 and 25 and respectfully request reversal of the decision of the Examiner.

Respectfully submitted,

/Christopher J. Reckamp/

Date: 02/22/2011 By: _____

Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005

CLAIMS APPENDIX

CLAIMS ON APPEAL

1. A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

2. The graphics processing circuit of claim 1, wherein the square regions comprise a two dimensional partitioning of memory.

3. The graphics processing circuit of claim 2, wherein the memory is a frame buffer.

4. The graphics processing circuit of claim 1, wherein each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data.

5. The graphics processing circuit of claim 4, wherein each of the at least two graphics pipelines further includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry.

APPENDIX A

6. The graphics processing circuit of claim 1, wherein each tile of the set of tiles further comprises a 16x16 pixel array.

7. The graphics processing circuit of claim 4, wherein the at least two graphics pipelines separately receive the pixel data from the front end circuitry.

10. The graphics processing circuit of claim 7, wherein a first of the at least two graphics pipelines processes the pixel data only in a first set of tiles in the repeating tile pattern.

11. The graphics processing circuit of claim 10, wherein the first of the at least two graphics pipelines further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the first set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

12. The graphics processing circuit of claim 1, wherein a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern.

13. The graphics processing circuit of claim 12, wherein the second of the at least two graphics pipelines further includes a scan converter, coupled to front end circuitry and back end circuitry, operative to provide position coordinates of the pixels within the second set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the set of tiles is to be processed by the back end circuitry.

APPENDIX A

14. The graphics processing circuit of claim 1 including a third graphics pipeline and a fourth graphics pipeline, wherein the third graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a third set of tiles in the repeating tile pattern, and wherein the fourth graphics pipeline includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process the pixel data in a fourth set of tiles in the repeating tile pattern.

15. The graphics processing circuit of claim 14, wherein the third graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the third set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

16. The graphics processing circuit of claim 14, wherein the fourth graphics pipeline further includes a scan converter, coupled to the front end circuitry and the back end circuitry, operative to provide position coordinates of the pixels within the fourth set of tiles to be processed by the back end circuitry, the scan converter including a pixel identification line for receiving tile identification data indicating which of the sets of tiles is to be processed by the back end circuitry.

APPENDIX A

17. The graphics processing circuit of claim 14, wherein the third and fourth graphics pipelines are on separate chips.

18. The graphics processing circuit of claim 14, further including a bridge operative to transmit vertex data to each of the first, second, third and fourth graphics pipelines.

19. The graphics processing circuit of claim 17 wherein the data includes a polygon and wherein each separate chip creates a bounding box around the polygon and wherein each corner of the bounding box is checked against a super tile that belongs to each separate chip and wherein if the bounding box does not overlap any of the super tiles associated with a separate chip, then the processing circuit rejects the whole polygon and processes a next one.

20. A graphics processing method, comprising:

receiving vertex data for a primitive to be rendered;

generating pixel data in response to the vertex data;

passing the same pixel data to both of the at least two graphics pipelines on a same chip;

determining the pixels within a set of tiles of a repeating tile pattern corresponding to screen locations to be processed by a corresponding one of the at least two graphics pipelines on a same chip in response to the pixel data, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions;

performing pixel operations on the pixels within the determined set of tiles by the corresponding one of the at least two graphics pipelines; and

transmitting the processed pixels to a memory controller, wherein the at least two graphics pipelines share the memory controller wherein the memory controller transfers pixel data from each of the at least two pipelines, to a shared memory.

APPENDIX A

21. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises determining the set of tiles that the corresponding graphics pipeline is responsible for.

22. The graphics processing method of claim 20, wherein determining the pixels within a set of tiles of the repeating tile pattern to be processed further comprises providing position coordinates of the pixels within the determined set of tiles to be processed to the corresponding one of the at least two graphics pipelines.

24. A graphics processing circuit, comprising:

front end circuitry on a chip operative to generate pixel data in response to primitive data for a primitive to be rendered;

first back end circuitry on the chip, coupled to the front end circuitry, operative to process a first portion of the pixel data in response to position coordinates;

a first scan converter on the chip, coupled between the front end circuitry and the first back end circuitry, operative to determine which set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions, and operative to provide the position coordinates to the first back end circuitry in response to the pixel data;

second back end circuitry on the chip, coupled to the front end circuitry, operative to process a second portion of the pixel data in response to position coordinates;

a second scan converter on the chip, coupled between the front end circuitry and the second back end circuitry, operative to determine which set of tiles of the repeating tile pattern are to be processed by the second back end circuitry, and operative to provide the position coordinates to the second back end circuitry in response to the pixel data; and

a memory controller on the chip, coupled to the first and second back end circuitry operative to transmit and receive the processed pixel data.

25. A graphics processing circuit, comprising:

at least two graphics pipelines on a chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile, wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of regions;

wherein the horizontally and vertically repeating pattern of regions include NxM number of pixels; and a memory controller on the chip, coupled to the at least two graphics pipelines on the chip and operative to transfer pixel data between each of the two graphics pipelines and a memory shared among the at least two graphics pipelines.

APPENDIX A

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS

[NONE]

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Evelyn Stenseth
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Filing a brief in support of an appeal	1402	1	540	540
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 5 months with $0 paid	1255	1	2350	2350
Miscellaneous:				
		Total in USD ($)		**2890**

Electronic Acknowledgement Receipt	
EFS ID:	9494801
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Evelyn Stenseth
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	22-FEB-2011
Filing Date:	12-JUN-2003
Time Stamp:	16:36:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2890
RAM confirmation Number	3556
Deposit Account	220259
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Extension of Time	5MO-EOT.pdf	331795 059663223b8c6bf4ae35059ed1058a0852b102b0	no	2
Warnings:					
Information:					
2	Appeal Brief Filed	AppealBrief.pdf	212949 4c3be5c41d58c7f62e80a767a50148f292f21605	no	37
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	32029 dd54afc41b4934282362a3f69bfe03063b14dee9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	576773		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a) **FY 2009** (*Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).*)	Docket Number (Optional) 00100.02.0053
Application Number 10/459797	Filed 2003-06-12
For Dividing Work Among Multiple Graphics Pipelines Using a Super-Tiling Technique	
Art Unit 2628	Examiner Joni Hsu

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	
☐	One month (37 CFR 1.17(a)(1))	$130	$65	$
☐	Two months (37 CFR 1.17(a)(2))	$490	$245	$
☐	Three months (37 CFR 1.17(a)(3))	$1110	$555	$
☐	Four months (37 CFR 1.17(a)(4))	$1730	$865	$
☑	Five months (37 CFR 1.17(a)(5))	$2350	$1175	$ 2350

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 220259.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration Number 34414

☐ attorney or agent under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Christopher J. Reckamp/ — Signature

02/22/2011 — Date

Christopher J. Reckamp — Typed or printed name

312.609.7599 — Telephone Number

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☑ Total of 1 forms are submitted.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 04/05/2011

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
04/05/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/459,797
Filing Date: June 12, 2003
Appellant(s): LEATHER ET AL.

Christopher J. Reckamp

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 22, 2011 appealing from the Office action mailed April 22, 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-7, 10-22, 24 and 25 are pending and stand rejected.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the

appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,570,579	MACINNIS	5-2003
6,864,896	PEREGO	3-2005
5,794,016	KELLEHER	8-1998
6,778,177	FURTNER	8-2004
5,905,506	HAMBURG	5-1999
2003/0164830	KENT	9-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in Graham **v.** John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4, 7, 10, 12, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2).

4. As per Claim 1, MacInnis teaches a graphics processing circuit, comprising: a graphics pipeline (58, Fig. 2) on a chip (10); a memory controller (54) on the chip (10), as shown in Fig. 2 (col. 4, lines 65-67; col. 5, lines 36-41), in communication with the graphics pipeline (58), operative to transfer pixel data between the pipeline (58) and a memory (col. 6, lines 10-13, 59-66).

However, MacInnis does not teach at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63) having at least 2 graphics pipelines (312) operative to process data in corresponding set of tiles of repeating tile pattern corresponding to screen locations, respective one of at least 2 graphics pipelines operative to process data in dedicated tile (col. 5, lines 19-27, 38-44); and memory controller (310, Fig. 3) in communication with at least 2 graphics pipelines

312, operative to transfer pixel data between each of 1st pipeline and 2nd pipeline and shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one memory that is shared among the at least two graphics pipelines. Repeating tile pattern includes horizontally and vertically repeating pattern of regions of square regions, as shown in Fig. 5 (col. 5, lines 19-27, 38-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include at least two graphics pipelines on the same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; wherein the repeating tile pattern includes a horizontally and vertically

repeating pattern of square regions because Perego suggests that this parallel processing significantly reduces the processing burden on the memory controller/graphics controller (col. 5, lines 38-46).

5. As per Claim 2, MacInnis does not teaches that the square regions comprise a two dimensional partitioning of memory. However, Perego teaches square regions have two dimensional partitioning of memory (col. 5, lines 19-33). This would be obvious for the reasons given in the rejection for Claim 1.

6. As per Claim 3, MacInnis teaches wherein the memory is a frame buffer (col. 6, line 66-col. 7, line 2).

7. As per Claim 4, MacInnis does not teach that each of the at least two graphics pipelines further includes front end circuitry operative to receive vertex data and generate pixel data corresponding to a primitive to be rendered, and back end circuitry, coupled to the front end circuitry, operative to receive and process a portion of the pixel data. However, Perego teaches each of at least 2 graphics pipelines includes front end circuitry (308, Fig. 3) operative to generate pixel data corresponding to primitive to be rendered, and back end circuitry (312), coupled to front end circuitry, operative to receive and process portion of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). In order for front end circuitry (308) to generate pixel data, it must receive vertex data. Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels (col. 5, lines 19-27). One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to

store data which are referenced during the execution of the programs (col. 1, lines 18-21). Therefore, the CPU is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and generate pixel data corresponding to a primitive to be rendered (col. 5, lines 19-27; col. 1, lines 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312 performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline. This would be obvious for the reasons given in the rejection for Claim 1.

8. As per Claim 7, MacInnis does not teach that the at least two graphics pipelines separately receive the pixel data from the front end circuitry. However, Perego teaches at least two graphics pipelines (312) separately receive pixel data from front end circuitry (308) (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). This would be obvious for the reasons given in the rejection for Claim 1.

9. As per Claim 10, MacInnis does not teach that a first of the at least two graphics pipelines processes the pixel data only in the first set of tiles in the repeating tile pattern. However, Perego teaches first of at least two graphics pipelines (first rendering engine of 312, Fig. 3) processes pixel data only in first set of tiles (tiles labeled "RE0" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

10. As per Claim 12, MacInnis does not teach that a second of the at least two graphics pipelines processes the data only in a second set of tiles in the repeating tile pattern. However, Perego teaches second of at least two graphics pipelines (second rendering engine of 312, Fig. 3) processes pixel data only in second set of tiles (tiles labeled "RE1" in Fig. 5) in repeating tile pattern (col. 5, lines 23-44). This would be obvious for the reasons given in the rejection for Claim 1.

11. As per Claim 14, Claim 14 is similar to Claims 4 and 10, except that Claim 14 is for a third and fourth graphics pipeline. Perego teaches four graphics pipelines (col. 5, lines 41-44). So Claim 14 is rejected under the same rationale as Claims 4 and 10.

12. As per Claim 25, Claim 25 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

13. Claims 5, 18, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A).

14. As per Claim 5, MacInnis and Perego are relied on for teachings for Claim 4.

But, MacInnis and Perego do not explicitly teach at each of 2 graphics pipelines includes scan converter, coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry. But, Kelleher teaches each of at least 2 graphics pipelines (20A, 20B, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) includes scan converter (update stage, Fig. 7), coupled to back end circuitry, operative to determine portion of pixel data to be processed by back end circuitry (col. 8, lines 52-61; col. 9, lines 1-23; col. 6, lines 26-28).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so at each of at least two graphics pipelines includes a scan converter, coupled to the back end circuitry, operative to determine the portion of the pixel data to be processed by the back end circuitry because Kelleher suggests scan converters are needed in order to define image data as array of pixels by calculating pixel addresses (col. 9, lines 1-23), as is well-known in the art.

15. As per Claim 18, MacInnis does not teach a bridge operable to transmit vertex data to each of the 1st, 2nd, 3rd and 4th graphics pipelines. But, Kelleher teaches a bridge (38, Fig. 3) operative to transmit vertex data to each of the 1st (20A), 2nd (20B), 3rd (20C) and 4th (20N) graphics pipelines (col. 3, lines 22-23; col. 4, lines 9-14; col. 8, lines 56-65; col. 3, lines 46-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis to include a bridge operable to transmit vertex data to each of the first, second, third and fourth graphics pipelines because Kelleher suggests being able to convert the vertex data to pixel data in parallel, which increases the efficiency of the graphics system (col. 2, lines 31-35; col. 8, lines 56-65; col. 9, lines 1-23).

16. As per Claim 24, MacInnis teaches a graphics processing circuit, comprising: front end circuitry (90, Fig. 4) operative to generate pixel data in response to primitive data for a primitive to be rendered (col. 8, lines 49-59); back end circuitry (98), coupled to the front end circuitry (90) (col. 9, lines 15-34), operative to process the pixel data in response to position coordinates (col. 9, lines 35-54). The front end circuitry (90) and the back end circuitry (98) are in the graphics display pipeline (80) (col. 7, lines 55-63), and the graphics display pipeline (80) is equivalent to display engine (58, Fig. 2), which is on graphics chip (10) (col. 4, lines 65-67; col.

5, lines 36-39). A memory controller (54) is also on graphics chip (10) (col. 4, lines 65-67; col. 5, lines 36-39). Therefore, the front end circuitry (90), the back end circuitry (98), and the memory controller (54) are on the chip (10). The memory controller (54) is coupled to the display engine (58) and is operative to transmit and receive the processed pixel data (col. 6, lines 10-13, 59-67; col. 7, lines 1-2). Since the display engine (58) is equivalent to the graphics display pipeline (80) which contains the back end circuitry (98) (col. 6, lines 59-67; col. 7, lines 55-63), the memory controller (54) is coupled to the back end circuitry (98) and is operative to transmit and receive the processed pixel data.

However, MacInnis does not teach first back end circuitry operative to process a first portion of the pixel data; set of tiles of a repeating tile pattern are to be processed by the first back end circuitry, the repeating tile pattern including a horizontally and vertically repeating pattern of square regions; second back end circuitry operative to process a second portion of the pixel data; set of tiles of the repeating tile pattern are to be processed by the second back end circuitry. However, Perego teaches graphics processing circuit (300, Fig. 3; col. 3, lines 61-63), having front end circuitry (308) operative to generate pixel data in response to primitive data for primitive to be rendered (col. 5, lines. 19-23); 1st back end circuitry (1st rendering engine 312), coupled to front end circuitry 308, operative to process 1st portion of pixel data (labeled "RE0" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be processed by 1st back end circuitry, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; 2nd back end circuitry (second rendering engine 312), coupled to front end circuitry 308, operative to process 2nd portion of pixel data (labeled "RE1" in Fig. 5) in response to position coordinates; set of tiles of repeating tile pattern are to be

processed by 2nd back end circuitry (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44); and memory controller (310), coupled to 1st and 2nd back end circuitry (312) operative to transmit and receive processed pixel data (col. 3, lines 65-67; col. 4, lines 1-53; col. 5, lines 32-44). Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system, such as a computer system. As subsystems with high memory performance requirements (such as graphics subsystems) are combined with the traditional main memory controller, the resulting architecture may provide a single high-performance main memory interface" (col. 1, lines 34-43). Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip, and so the first back end circuitry and second back end circuitry are on the same chip. Since MacInnis teaches that the front end circuitry, the back end circuitry and the memory controller are on the same chip, this teaching from Perego can be implemented into the device of MacInnis so that the front end circuitry sends pixel data to both the first back end circuitry and the second back end circuitry, and the front end circuitry, the first back end circuitry, the second back end circuitry, and the memory controller are on the same chip. This would be obvious for the reasons given in the rejection for Claim 1.

However, MacInnis and Perego do not explicitly teach first scan converter and second scan converter. However, Kelleher teaches first scan converter, coupled between front end circuitry (14, Fig. 3) and first back end circuitry (update stage, Fig. 7 in 20A, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by first back end circuitry (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23), and operative to provide position coordinates to first back end circuitry in response to pixel data (col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38); second scan converter, coupled between front end circuitry and second back end circuitry (update stage, Fig. 7 in 20B, Fig. 3), operative to determine which set of tiles of repeating tile pattern are to be processed by second back end circuitry, and operative to provide position coordinates to second back end circuitry in response to pixel data (col. 3, lines 22-23; col. 8, line 33-col. 9, line 23; col. 4, lines 60-62; col. 8, lines 52-65; col. 6, lines 36-38). Therefore, by implement this teaching into the device of Perego, front end circuitry, first back end circuitry, and first scan converter of Perego-Kelleher combination make up one graphics pipeline, and front end circuitry, second back end circuitry, and second scan converter of Perego-Kelleher combination make up another graphics pipeline. Since Perego teaches graphics pipelines are on the same chip, the teaching from Kelleher can be applied to Perego so that the first scan converter and the second scan converter are also on the same chip. This would be obvious for reasons given in the rejection for Claim 5.

17. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1).

18. As per Claim 6, MacInnis and Perego are relied upon for the teachings as discussed above relative to Claim 1.

However, MacInnis and Perego do not expressly teach that each tile of the set of tiles further comprises a 16x16 pixel array. However, Furtner teaches that each tile of the set of tiles further comprises a 16x16 pixel array (col. 11, lines 45-48, 64-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis and Perego so each tile of set of tiles further has 16x16 pixel array because Furtner suggests depending on number of parallel image-rendering pipelines and depending on memory organization, optimum tile size and shape can be selected (col. 11, lines 45-48, 64-65), and so it would be obvious to modify tile size to be 16x16 pixels if that would be optimum tile size for particular number of parallel image-rendering pipelines and particular memory organization.

19. As per Claim 17, MacInnis does not teach 3rd and 4th graphics pipelines are on separate chips. However, Furtner teaches this limitation (col. 6, lines 47-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis so pipelines are on separate chips because Furtner teaches this makes system more configurable by being able to easily add more graphics pipelines to increase performance (col. 6, lines 29-30, 42-51).

20. Claims 11, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Kelleher (US005794016A), further in view of Hamburg (US005905506A).

MacInnis and Perego are relied upon for teachings relative to Claim 10.

However, MacInnis and Perego do not explicitly teach scan converter. However, Kelleher teaches first of the at least two graphics pipelines (20A, Fig. 3; col. 3, lines 22-23; col. 4, lines 9-14) further includes scan converter (84, Fig. 7), coupled to front end circuitry (80, 82) and back end circuitry (col. 8, line 52-col. 9, line 23). Scan converter determines which groups of blocks 52 within graphics memory 22 are allocated to and controlled by graphics pipelines (col. 8, lines 52-65; col. 6, lines 26-28). Graphics memory is partitioned into plurality of pixel blocks that are tiled in x-and y-direction of graphics memory (col. 4, lines 60-62). So, scan converter is inherently operative to provide memory addresses or position coordinates of pixels within first set of tiles to be processed by back end circuitry. This would be obvious for the reasons given in the rejection for Claim 5.

But, MacInnis, Perego, and Kelleher do not expressly teach using tile identification data to indicate which tiles are to be processed. But, Hamburg teaches pixel identification line for receiving tile identification data indicating which tiles are to be processed (col. 5, lines 35-52).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Kelleher to include using tile identification data to indicate which tiles are to be processed because Hamburg suggests advantage of using tile identification data to easily track storage locations of tile pixel data and being able to easily retrieve data for particular image tile (col. 1, lines 46-54).

21. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis (US006570579B1) in view of Perego (US006864896B2), further in view of Furtner (US006778177B1), further in view of Kent (US 20030164830A1).

MacInnis, Perego, and Furtner are relied upon for the teachings as discussed above relative to Claim 17. MacInnis teaches data includes polygon (col. 58, lines 50-54). Furtner teaches third and fourth graphics pipelines are on separate chips (col. 6, lines 47-51), as discussed for Claim 17.

But, MacInnis, Perego, and Furtner do not teach creating bounding box around polygon and each corner of bounding box is checked against super tile that belongs to each separate chip and if bounding box does not overlap any of super tiles associated with separate chip, then processing circuit rejects whole polygon and processes next one. But, Kent teaches graphics pipeline [0006] calculates bounding box of primitive and testing this against VisRect. If bounding box of primitive is contained in other P10's super tile the primitive is discarded at this stage [0129]. Primitive can be polygon [0088]. Method used is to calculate distance from each subpixel sample point in point's bounding box to point's center and compare this to point's radius. Subpixel sample points with distance greater than radius do not contribute to pixel's coverage. Cost of this is kept low by only allowing small radius points hence distance calculation is a small multiply and by taking a cycle per subpixel sample per pixel within bounding box [0144]. Since method calculates distance from each subpixel sample point in point's bounding box, this must include all corners of bounding box. So, Kent teaches data includes polygon and graphics pipeline creates bounding box around polygon and wherein each corner of bounding box is checked against super tile that belongs to graphics pipeline and if bounding box does not overlap any of super tiles, then processing circuit rejects whole polygon and processes next one.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify MacInnis, Perego, and Furtner to include bounding box as because Kent suggests processing super tiles one at a time in order to hide page break costs [0129, 0051].

22. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perego (US006864896B2).

23. As per Claim 20, Perego teaches graphics processing method, comprising generating pixel data (col. 5, lines 19-25), which is inherently generated in response to received vertex data. Perego teaches a shared front end (308, Fig. 3) that passes the pixel data to both of the two graphics pipelines (first rendering engine 312 and second rendering engine 312) (col. 3, line 63-col. 4, line 2; col. 5, lines 19-44), similarly as what is described in the instant specification, and so Perego teaches passing the same pixel data to both of the two graphics pipelines. Perego shows in Fig. 8 that in one embodiment, a memory module 800 contains two different rendering engines 802 and 810 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip. Perego teaches determining pixels within set of tiles of repeating tile pattern corresponding to screen locations to be processed by corresponding one of the at least two graphics pipelines (312, Fig. 3) in response to pixel data, repeating tile pattern including horizontally and vertically repeating pattern of square regions, as shown in Fig. 5; performing pixel operations on pixels within determined set of tiles by corresponding one of at least two graphics pipelines (col. 5, lines 19-44); and transmitting processed pixels to memory controller 310, at least 2 graphics pipelines share

memory controller (col. 3, line 65-col. 4, line 25; col. 5, lines 31-44) wherein the memory controller transfers pixel data from each of the at least two pipelines, to shared memories 314 (col. 3, lines 65-67; col. 4, lines 1-10, 48-65). Shared memories 314 are each part of main memory (col. 1, lines 44-54; col. 3, lines 3-6), and so are considered to be one shared memory. Perego describes "Improvements in integrated circuit design and manufacturing technologies allow higher levels of integration, thereby allowing an increasing number of subsystems to be integrated into a single device. This increased integration reduces the total number of components in a system" (col. 1, lines 34-39). Perego teaches that CPU 308 generates the pixel data (col. 5, lines 19-27). CPU 308 passes the same pixel data to the memory controller/graphics controller 310, as shown in Fig. 3. The memory controller/graphics controller 310 passes the pixel data to the rendering engines 312 (col. 5, lines 3-6), as was pointed out by Appellant. The first rendering engine 312 and the second rendering engine 312 are both coupled to the same memory controller/graphics controller 310. Thus, the memory controller/graphics controller 310 and the first rendering engine 312 are considered to be one graphics pipeline, and the memory controller/graphics controller 310 and the second rendering engine 312 are considered to be another graphics pipeline. Since CPU 308 passes the same pixel data to the memory controller/ graphics controller 310, and the memory controller/graphics controller 310 and the first rendering engine 312 are considered to be one graphics pipeline, and the memory controller/graphics controller 310 and the second rendering engine 312 are considered to be another graphics pipeline, this means that the same pixel data is passed to at least two graphics pipelines.

24. As per Claim 21, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed further comprises determining set of tiles that corresponding graphics pipeline is responsible for (col. 5, lines 19-50).

25. As per Claim 22, Perego teaches determining pixels within set of tiles of repeating tile pattern to be processed comprises providing position coordinates of pixels within determined set of tiles to be processed to corresponding one of at least 2 graphics pipelines (col. 5, lines 19-44).

(10) Response to Argument

1. Appellant's arguments filed February 22, 2011 have been fully considered but they are not persuasive.

2. As per Claim 1, Appellant argues that Perego (US006864896B2) describes that shared memory 314 is shared between a CPU and the rendering engine 312. The shared memory of Perego is not shared between multiple rendering engines on different modules or shared between multiple rendering engines on a single module (p. 17). Perego defines "shared memory" as memory devices partitioned for use as both CPU "main memory" and "graphics memory", not as memory shared between two or more graphics pipeline. The memory used for graphics processing is separate from the memory used by the CPU. Perego explicitly states that, "the graphics memory is statically or dynamically partitioned off from the main memory pool." Perego teaches each rendering engine as having separate, dedicated memory. Perego's Fig. 8 shows two separate rendering engines, each associated with their own dedicated group of memory devices (memory devices 804 and 812, respectively) using distinct memory interconnects (806 and 814, respectively). Perego teaches away from the claimed design where a single memory controller shares a single memory between multiple graphics pipelines. Perego

explicitly states the advantage of having distinct memory devices tied to individual rendering engines: "the partitioning of memory among multiple memory modules 304 improves graphical data throughput relative to systems in which a single graphics controller performs all processing tasks and reduces bandwidth contention with the CPU…the system partitioning described allows aggregate bandwidth between the rendering engines and the memory devices to be much higher than the bandwidth between the controller and memory modules" (p. 18-19). If Perego did share graphics memory between rendering engines, no bandwidth gain would be attained as graphics data would necessarily be transferred through the memory/graphics controller to another memory module -- exactly the scenario Perego seeks to avoid (p. 20).

In reply, the Examiner points out that Perego describes "The shared memory 314 typically includes multiple memory devices coupled together to form a block of storage space" (col. 4, lines 8-10). Thus, the block of storage space is considered to be a memory shared among the two graphics pipelines. Claim 1 recites "at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile…wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions", and Claim 2 recites "wherein the square regions comprise a two dimensional partitioning of memory". Since each graphics pipeline processes a dedicated tile that is a square region, and each square region is a partition of memory, this means that each graphics pipelines stores data to a partition of memory. Since Perego teaches that each graphics pipeline stores data to a partition of the block of storage space, and the block of storage space is

shared among the two graphics pipelines (col. 1, lines 44-54; col. 3, lines 3-6, 65-67; col. 4, lines 1-10, 48-65; col. 5, lines 42-44), Perego reads on the limitations as recited in the Claim 1.

3. As per Claim 4, Appellant argues that element 308 of Perego is actually a "CPU" and is not a pixel pipeline. Perego teaches that CPUs may sort primitive data which may be then submitted to the rendering pipeline. The CPU does not generate pixel data as alleged, since the rendering engine must generate pixel data (p. 20-21).

In reply, the Examiner points out that Perego teaches that the CPU sorts the primitive data according to the spatial region of the rendering surface (e.g., the x and y coordinates) covered by that primitive, and the rendering surface is divided into multiple rectangular regions of pixels, referred to as "tiles", and then these tiles are sent to the multiple rendering engines (col. 5, lines 19-27). Thus, the tiles that were divided by the CPU already contain pixels prior to sending the tiles to the rendering engines. Thus, the CPU generates pixel data. One of ordinary skill in the art would understand that data pertaining to the x and y coordinates covered by the primitive would include vertex data. The main memory is used to store data which are referenced during the execution of the programs (col. 1, lines 18-21). Therefore, the **CPU** is operative to receive vertex data (data pertaining to the x and y coordinates covered by the primitive) from the main memory and **generate pixel data** corresponding to a primitive to be rendered (col. 5, lines 19-27; col. 1, lines 18-21). Perego teaches that rendering engine 312 is coupled to the CPU, and is operative to receive and process a rectangular region of pixel data (col. 3, line 64-col. 4, line 2; col. 5, lines 19-44). Since the CPU is coupled to the rendering engine 312, and the CPU and the rendering engine 312 both perform graphics processing, and, the CPU performs the operations of the front end circuitry, and the rendering engine 312

performs the operations of the back end circuitry, the CPU and the rendering engine 312 are considered to be part of a graphics pipeline, and the CPU is considered to be the front end circuitry included in the graphics pipeline.

4. As per Claim 24, Appellant argues that Perego does not teach that both front and back end circuitry on the chip are both coupled to the same front end circuitry. Fig. 8 actually shows separate front end circuitry being employed since separate rendering engines 802 and 810 are employed and each of these are identical in structure (p. 23).

In reply, the Examiner points out that Perego shows in Fig. 8 that the two different rendering engines 802 and 810 are within the same memory module 800 (Fig. 8; col. 6, lines 61-62), and therefore at least two graphics pipelines (802, 810) are on a same memory module 800. From Fig. 8 and from the description in Perego, one of ordinary skill in the art would understand that a memory module is equivalent to a chip. Therefore, Perego teaches that two graphics pipelines are on the same chip, and so first backend circuitry (first rendering engine 312) and second backend circuitry (second rendering engine 312) (col. 3, lines 65-67; col. 4, liens 1-53; col. 5, lines 32-44) are on a common chip. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). MacInnis (US006570579B1) is used to expressly teach common front end circuitry and memory controller are on a common chip.

5. As per Claim 11, Appellant argues that the claim requires that the claimed tile identification data and the claimed scan converter utilizes the tile identification data to indicate

which sets of tiles are to be processed by the back end circuitry. The Hamburg reference (US005905506A) is directed to a system post-pixel rendering whereas Appellants are actually claiming a scan converter and back end circuitry used to generated pixels whereas Hamburg describes a system where pixels are already generated and then undergo a copy operation from one tile to another tile (p. 24). The reasoning given for utilizing Hamburg by the Examiner is that this would allow easily tracking of storage location of tile pixel data and to be able to easily retrieve data for a particular image tile. This reasoning however is irrelevant to the claimed subject matter which is actually dealing with a different operation namely pixel generation using scan converter and back end circuitry whereas the alleged motivation deals with tracking storage locations of already generated pixel data and retrieving already generated pixel data (p. 25).

In reply, the Examiner points out that Hamburg describes "**During pixel modification**, the system must write a pixel within at least one tile within image B. As above, the system determines a tile index, tile ID...indexing into the tile array 6 for image A to obtain the tile ID for the corresponding tile in image A. The system then physically copies the pixel data in that image A tile to the corresponding image tile in image B found by indexing into the tile array 6' for image B" (col. 5, lines 35-52). Thus, Hamburg teaches receiving tile identification data indicating which tiles are to be copied, and this copying is part of a pixel modification process. Thus, Hamburg teaches receiving tile identification data indicating which tiles are to be processed in a pixel modification process.

6. As per Claim 19, Appellant argues that Kent (US 20030164830A1) describes a method where every subpixel sample point is evaluated in comparison to a bounding box from the point's center and compared to the point's radius. Moreover, this is done to determine which subsample

points do not contribute to a pixel's coverage. Appellants claim a different operation wherein the corners of a bounding box is checked against a super tile to determine if the bounding box overlaps any of the super tiles associated with the chip (p. 27).

In reply, the Examiner points out that since Kent teaches that the bounding box is checked, this includes the corners of the bounding box. Since Claim 19 does not recite that **only** the corners of the bounding box are checked, Kent still teaches the limitation as it is recited in Claim 19. Kent describes "If the bounding box of the primitive is contained in the other P10's super tile the primitive is discarded at this stage" [0129]. Since the bounding box is checked, this includes the corners of the bounding box. Thus, Kent teaches that the corners of a bounding box is checked against a super tile to determine if the bounding box overlaps any of the super tiles associated with the chip. Thus, Kent teaches the limitation as it is recited in Claim 19.

7. As per Claim 20, Appellant argues that Perego does not teach transferring the same pixel data to two or more graphics pipelines. Perego teaches each separate rendering engine receiving distinct and different pixel data. Perego states: "The memory controller/graphics controller partitions the processing task into multiple portions and distributes each portion of the processing task to a rendering engine" (col. 5, lines 3-6). Perego teaches that each rendering engine receives only the specific portion of the processing task that it is responsible for processing (p. 28).

In reply, the Examiner points out that Perego teaches that CPU 308 generates the pixel data (col. 5, lines 19-27). CPU 308 passes the same pixel data to the memory controller/graphics controller 310, as shown in Fig. 3. The memory controller/graphics controller 310 passes the pixel data to the rendering engines 312 (col. 5, lines 3-6), as was pointed out by Appellant. The first rendering engine 312 and the second rendering engine 312 are both coupled to the same

memory controller/graphics controller 310. Thus, the memory controller/graphics controller 310 and the first rendering engine 312 are considered to be one graphics pipeline, and the memory controller/graphics controller 310 and the second rendering engine 312 are considered to be another graphics pipeline. Since CPU 308 passes the same pixel data to the memory controller/ graphics controller 310, and the memory controller/graphics controller 310 and the first rendering engine 312 are considered to be one graphics pipeline, and the memory controller/graphics controller 310 and the second rendering engine 312 are considered to be another graphics pipeline, this means that the same pixel data is passed to at least two graphics pipelines.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joni Hsu

/Joni Hsu/

Primary Examiner, Art Unit 2628

Conferees:

/Kee M Tung/

Supervisory Patent Examiner, Art Unit 2628

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Mark M. Leather et al.	Examiner: Joni Hsu
Application No.: 10/459,797	Group Art Unit: 2628
Filed: June 12, 2003	Docket No.: 00100.02.0053
For: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**	

APPELLANTS' REPLY BRIEF IN RESPONSE TO EXAMINER'S ANSWER

Dear Sir:

Appellants wish to thank the Examiner for the "Response to Argument" set forth in the Examiner's Answer. Appellants respectfully reiterate their prior remarks as it appears that the claim construction and teachings of Perego are incorrect. Appellants again respectfully submit that the claims must be reasonably interpreted in view of the Specification and that the claims themselves contradict the Examiner's construction as do the actual teachings of the Perego reference which were not addressed in the Examiner's "Response to Arguments" section. Claim 1, for example, recites the memory controller on the chip in communication with at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and a second pipeline in a memory shared among the at least two graphics pipelines… As such, the same memory controller that is on the chip is in communication with two graphics pipelines and the memory is shared among the at least two graphics pipelines. The Examiner's position appears to overlook what the Perego reference actually teaches as being shared. What is shared in Perego is memory between a CPU and a single rendering engine which is specifically described and shown in Perego as a memory module 304 or 804 including a rendering engine 312 and dedicated

memory that the CPU can access but no other rendering engine can access. Only a single rendering engine can access the memory on a memory module.

FIG. 8 clearly shows this structure since each rendering engine only has access to its own memory devices. Appellants claim a different configuration wherein the same memory controller on a chip is in communication with shared memory that is shared between two graphics processors. The graphics rendering engines in Perego cannot share memory amongst graphics engines and do not incorporate a common memory controller to do so. Perego uses the term "shared memory" because a portion of the memory on each separate memory module is used by the CPU, the claims do not claim such an operation but instead claim that the memory controller on the chip is in communication with multiple graphics pipelines and transfers pixel data between each of the pipelines and the memory controller that is in communication with a memory shared among the at least two graphics pipelines. Multiple rendering engines in Perego do not share the same graphics memory through a common memory controller on a chip as alleged in the office action. Accordingly, Appellants respectfully reversal of the rejections.

Appellants also respectfully reassert their other remarks from their Brief.

Respectfully submitted,

Date: June 6, 2011

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005

Electronic Acknowledgement Receipt

EFS ID:	10240393
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	06-JUN-2011
Filing Date:	12-JUN-2003
Time Stamp:	15:34:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reply Brief Filed	10459797_ReplyBrief.pdf	22033 c005e4fdf41b2ef936df78b7084a4385e36d61c8	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	22033

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 06/17/2011

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
06/17/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address : COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10/459,797	12 June 2003	LEATHER ET AL.	00100.02.0053

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER
JONI HSU

ART UNIT	PAPER
2628	20110606

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The Reply Brief filed June 6, 2011 has been noted by the examiner and has been placed in the file.

/Joni Hsu/
Primary Examiner, Art Unit 2628

PTO-90C (Rev.04-03)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 06/23/2011

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
06/23/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

United States Patent and Trademark Office

Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

Appeal No: 2011-010197
Application: 10/459,797
Appellant: Mark M. Leather et al.

Board of Patent Appeals and Interferences
Docketing Notice

Application 10/459,797 was received from the Technology Center at the Board on June 20, 2011 and has been assigned Appeal No: 2011-010197.

In all future communications regarding this appeal, please include both the application number and the appeal number.

The mailing address for the Board is:

BOARD OF PATENT APPEALS AND INTERFERENCES
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VIRGINIA 22313-1450

The facsimile number of the Board is 571-273-0052. Because of the heightened security in the Washington D.C. area, facsimile communications are recommended. Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number listed above.

By order of the Board of Patent Appeals and Interferences.

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 29153

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 29153

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

ATI Technologies ULC
1 Commerce Valley Drive East
Markham, Ontario, Canada L3T 7X6

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	June 15 2011
Name	Kevin A. O'Neil	Telephone	289-695-0642
Title	Director, Patents and Licensing		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Mark M. Leather et al.

Application No./Patent No.: 10/459,797 Filed/Issue Date: June 12, 2003

Titled: Dividing work among multiple graphics pipelines using a super-tiling technique

ATI Technologies ULC , a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025573, Frame 0443, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Christopher J. Reckamp/ October 19, 2012

Signature Date

Christopher J. Reckamp Attorney for Applicant

Printed or Typed Name Title

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	14096717
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Tanya Fishero
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	29-OCT-2012
Filing Date:	12-JUN-2003
Time Stamp:	15:06:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	ATI-POA.pdf	113490 a941caee2871b9244348392ca620331093e35c79	no	1

Warnings:	
Information:	

2	Assignee showing of ownership per 37 CFR 3.73.	020053-37-cfr.pdf	423434 537f4fc82569d7c73cac6b7ffb8036e3fb950d0e	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	536924

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053

CONFIRMATION NO. 4148

29153
ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

POA ACCEPTANCE LETTER

OC000000057439566

Date Mailed: 11/06/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/29/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ddinh/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053

CONFIRMATION NO. 4148

29153
ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

POWER OF ATTORNEY NOTICE

OC000000057439543

Date Mailed: 11/06/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/29/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/ddinh/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 06/26/2014

ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER	
RICHER, JONI	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
06/26/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteas@faegrebd.com
michelle.davis@faegrebd.com
cynthia.payson@faegrebd.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MARC M. LEATHER and ERIC DEMERS

Appeal 2011-010197
Application 10/459,797
Technology Center 2600

Before ROBERT E. NAPPI, JASON V. MORGAN, and J. JOHN LEE, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the rejection of claims 1 through 7, 10 through 22, 24, and 25.

We affirm-in-part.

INVENTION

The invention is directed to a graphics processing circuit that includes at least two pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two pipelines operative to process data in a dedicated tile. *See* Abstract of Appellants' Specification. Claim 1 is illustrative of the invention and reproduced below:

1. A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

REJECTIONS AT ISSUE

The Examiner has rejected claims 1 through 4, 7, 10, 12, 14, and 25 under 35 U.S.C. § 103(a) as unpatentable over MacInnis (U.S. 6,570,579 B1; May 27, 2003) and Perego (U.S. 6,864,896 B2; Mar. 8, 2005). Answer 4-8.[1]

The Examiner has rejected claims 5, 18, and 24 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, and Kelleher (U.S. 5,794,016; Aug. 11, 1998). Answer 8-12.

The Examiner has rejected claims 6 and 17 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, and Furtner (U.S. 6,778,177 B1; Aug. 17, 2004). Answer 12-13.

The Examiner has rejected claims 11, 13, 15, and 16 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, Kelleher, and Hamburg (U.S. 5,905,506; May 18, 1999). Answer 13-14.

---

[1] Throughout this opinion we refer to the Appeal Brief dated February 22, 2011, Reply Brief dated June 6, 2011, and the Examiner's Answer mailed on April 5, 2011.

The Examiner has rejected claim 19 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, Furtner and Kent (US 2003/0164830 A1; Sept. 4, 2003). Answer 14-16.

The Examiner has rejected claims 20 through 22 under 35 U.S.C. § 103(a) as unpatentable over Perego. Answer 16-18.

ISSUES

Rejection independent claims 1 and 25.

Appellants argue on pages 16 through 22 of the Appeal Brief and pages 1 and 2 of the Reply Brief, the Examiner's rejection of independent claims 1 and 25 is in error. The dispositive issue presented by this argument is: Did the Examiner err in finding that the combination of MacInnis and Perego teach a memory shared among the graphics pipelines?

Rejection independent claim 20.

Appellants argue on pages 27 and 28 of the Appeal Brief that the Examiner's rejection of claim 20 is in error. Appellants' argument with respect to this claim presents us with the issue: did the Examiner err in finding that Perego teaches passing the same pixel data to both of the graphics pipelines on the same chip?

Rejection independent claim 24.

Appellants argue on pages 22 and 23 of the Appeal Brief that the Examiner's rejection of claim 24 is in error. Appellants' argument with respect to this claim present us with the issue: did the Examiner err in

finding that the combination of MacInnis, Perego, and Kelleher teaches both the front end and the back end circuitry on the same chip as claimed?

ANALYSIS

We have reviewed Appellants' arguments in the Briefs, the Examiner's rejection and the Examiner's response to the Appellants' arguments. We agree with Appellants' conclusion that the Examiner erred rejecting claims 1 through 7, 10 through 22, and 25 under 35 U.S.C. § 103(a) but disagree with Appellants' conclusion the Examiner erred in rejecting claim 24 under 35 U.S.C. § 103(a).

Rejection independent claims 1 and 25.

The Examiner's response, to Appellants' arguments directed to the rejection of these claims, cites to Perego's teaching of memory (item 314 of Figure 3) which the Examiner finds is shared between the pipelines (items 312 of Figure 3). Answer 4, 5, 19, and 20. We disagree with the Examiner's finding. As argued by Appellants on page 17 of the Appeal Brief, Perego teaches item 314 is a shared memory, but it is shared between the CPU and the individual rendering engines and not shared among the rendering engines (which the Examiner equates to graphics pipelines) as claimed. The Examiner has not found that MacInnis teaches this feature. Thus, we do not find the Examiner has shown that combination of MacInnis and Perego teaches all of the limitations of independent claims 1 and 25. Accordingly, we will not sustain the Examiner's rejection of claims 1

through 4, 7, 10, 12, 14, and 25 under 35 U.S.C. § 103(a) as unpatentable over MacInnis and Perego.

The Examiner has not found that Kelleher, Furtner, Kent, or Hamburg teaches the shared memory as recited in independent claims 1. Accordingly, we similarly will not sustain the Examiner's rejection of claims 5, 6, 11, 13, and 15 through 19 under 35 U.S.C. § 103(a)

Rejection independent claim 20.

The Examiner's response to Appellants' arguments directed to the rejection of claim 20 cites to Perego's teaching of the CPU (item 308 Figure 3) generating the pixel data through the graphic controller (item 310) to the rendering engines (item 312). Answer 23-24. We disagree with the Examiner's finding. As argued by Appellants, on page 28 of the Appeal Brief, Perego teaches each rendering engine receives different portions of the processing task. Thus, we do not find the Examiner has shown that Perego teaches or makes obvious all of the limitations of independent claim 20. Accordingly we will not sustain the Examiner's rejection of claims 20 through 22 under 35 U.S.C. § 103(a) as unpatentable over Perego, Furtner and Kent.

Rejection independent claim 24.

The Examiner's response, to Appellants' arguments directed to the rejection of claim 24, cites to Perego's teaching in Figure 8 that two different rendering engines, which the Examiner equates with the claimed back end circuitry, are within the same memory module or chip. Answer 22. Further, the Examiner finds that MacInnis teaches that a common front end

circuitry, a back end circuitry, and a memory controller are on the same chip. Answer 9, 10, and 22. Appellants' arguments, directed to the rejection of claim 24, do not address the teachings of MacInnis or the combined teachings. Rather Appellants only assert that Perego does not teach the front end and back end circuitry on the same chip as claimed. Thus, Appellants' arguments directed to the rejection of independent claim 24 have not persuaded us of error in the Examiner's rejection as it has not addressed the combined teachings of the references. Accordingly, we sustain the Examiner's rejection of claim 24 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, and Kelleher.

DECISION

The decision of the Examiner to reject claims 1 through 7, 10 through 22, 24, and 25 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

ELD

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mark. M. Leather et al.	Examiner:	Joni Hsu
Serial No.	10/459,797	Art Group:	2611
Filing Date:	June 12, 2003	Docket No.:	00100.02.0053
Conf. No.:	4148		
Title:	**DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER TILING TECHNIQUE**		

EXAMINER INTERVIEW SUMMARY

Dear Examiner:

Applicants' attorney, Christopher J. Reckamp, wishes to thank the Examiner for the courtesies extended during the telephone conferences of August 26, 2014. Applicants' attorney and the Examiner discussed the cancellation of claim 24 and the passage of remaining claims to allowance in view of the Board's Decision on Appeal. The Examiner indicated Applicants need not file any response and that claim 24 will be canceled and the other claims passed to allowance.

The Examiner is invited to contact the below-listed attorney if the Examiner has any questions.

Respectfully submitted,

Dated: August 26, 2014

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Reg. No. 34,414

Faegre Baker Daniels LLP
311 S. Wacker Drive
Chicago, IL 60606
PHONE: (312) 356-5094
FAX: (312) 212-6501

Electronic Acknowledgement Receipt

EFS ID:	19967889
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	26-AUG-2014
Filing Date:	12-JUN-2003
Time Stamp:	14:43:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	020053_InterviewSummary.pdf	98472 01c97d86c9ae53ca2c65798b2e6eae10d2bcbce5	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	98472

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

29153 7590 09/04/2014

ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER
RICHER, JONI

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 09/04/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

TITLE OF INVENTION: Dividing work among multiple graphics pipelines using a super-tiling technique

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/04/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

29153 7590 09/04/2014
ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

TITLE OF INVENTION: Dividing work among multiple graphics pipelines using a super-tiling technique

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/04/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
RICHER, JONI	2611	345-506000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 09/04/2014

ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER	
RICHER, JONI	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 09/04/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 10/459,797	Applicant(s) LEATHER ET AL.	
	Examiner JONI RICHER	Art Unit 2611	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers received June 26, 2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-7,10-22 and 25*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JONI RICHER/
Primary Examiner, Art Unit 2611

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Christopher Reckamp on August 26, 2014.

3. The application has been amended as follows:

Claim 24 has been canceled.

Allowable Subject Matter

4. Claims 1-7, 10-22, and 25 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI RICHER whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JR

/JONI RICHER/
Primary Examiner, Art Unit 2611

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 4148

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/459,797	06/12/2003 RULE	345	2611	00100.02.0053

APPLICANTS

INVENTORS

Mark M. Leather, Saratoga, CA;
Eric Demers, Palo Alto, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/429,641 11/27/2002

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/07/2003

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /JONI RICHER/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	24	3

ADDRESS

ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606
UNITED STATES

TITLE

Dividing work among multiple graphics pipelines using a super-tiling technique

FILING FEE RECEIVED		
1122	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	Art Unit
	Richer, Joni	2611

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
345	506, 530, 505, 588, 544, 545, 532, 501, 502, 531, 519	4/12/10	JR
Above	UPDATED	8/29/14	JR

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB) -- See attached search history.	8/29/14	JR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Interference Search History Printout.	8/29/14	JR

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	JONI RICHER	2611

CPC						
Symbol					**Type**	**Version**
G06T		11	/	40	F	2013-01-01
G06T		1	/	20	I	2013-01-01
G06T		15	/	005	I	2013-01-01
G09G		5	/	363	I	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/JONI RICHER/ Primary Examiner.Art Unit 2611	8/29/14	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	JONI RICHER	2611

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
345	506	G 0 6 T 1 / 20 (2006.01.01)	
CROSS REFERENCE(S)		G 0 6 F 13 / 14 (2006.01.01)	
		G 0 6 F 12 / 02 (2006.01.01)	

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
345	519	544			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	21	
/JONI RICHER/ Primary Examiner.Art Unit 2611	8/29/14	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10459797	LEATHER ET AL.
	Examiner	**Art Unit**
	JONI RICHER	2611

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
2	2	17	18												
3	3	16	19												
4	4	18	20												
5	5	19	21												
9	6	20	22												
6	7		23												
	8		24												
	9	21	25												
7	10		26												
8	11														
10	12														
11	13														
12	14														
13	15														
14	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/JONI RICHER/ Primary Examiner.Art Unit 2611	8/29/14	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1305	345/545.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L2	974	345/530.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L3	234	345/544.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L4	169	345/532.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L5	2337	345/501.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L6	1377	345/502.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L7	96	345/588.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L8	1386	345/531.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L9	1101	345/506.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L10	3866	til$3 and repeat$3 and pattern$3 and pixel$1 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L11	3018	til$3 and repeat$3 and pattern$3 and pixel$1 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L12	1056	345/505.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45

L13	601	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L14	390	til$3 and repeat$3 same (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L15	283	til$3 and repeat$3 with (til$3 pattern$3) same pixel$1 and pattern$3 and horizontal$2 and vertical$2 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L16	601	scan adj conver$5 and pixel$1 and til$3 and pipelin$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L17	849	(multiple plurality) same pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L18	323	(multiple plurality) near2 pipelin$3 and scan adj conver$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L19	187	non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L20	93	repeat$3 and til$3 and non adj square same til$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L21	596	345/519.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L22	314	(multiple plural$3) adj2 graphic$1 adj (pipelin$3 process$3 engine$1) same (circuit chip)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45
L23	223	graphic$1 adj pipelin$3 same memory adj controller$1 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/08/29 10:45

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L26	150	(til$3 and repeat$3 and pattern$3 and pixel$1).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/29 10:51
L27	91	(graphics and pipelines and shar$3 and memory).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/29 10:52
L29	95	(graphics and pipelines and tiles and memory).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/29 10:52
L30	129	(graphics and pipelines and chip and memory).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/08/29 10:52

8/29/2014 10:53:29 AM
C:\Users\jhsu\Documents\10459797a.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

29153 7590 09/04/2014
ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Christine A. Wright	(Depositor's name)
/Christine A. Wright/	(Signature)
December 4, 2014	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

TITLE OF INVENTION: Dividing work among multiple graphics pipelines using a super-tiling technique

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/04/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
RICHER, JONI	2611	345-506000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Faegre Baker Daniels LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: ATI Technologies ULC
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Markham, Ontario, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 020390 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Christopher J. Reckamp/ Date December 4, 2014
Typed or printed name Christopher J. Reckamp Registration No. 34,414

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	10459797
Filing Date:	12-Jun-2003
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Filer:	Christopher J. Reckamp/Christine Wright
Attorney Docket Number:	00100.02.0053

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	20863538
Application Number:	10459797
International Application Number:	
Confirmation Number:	4148
Title of Invention:	Dividing work among multiple graphics pipelines using a super-tiling technique
First Named Inventor/Applicant Name:	Mark M. Leather
Customer Number:	29153
Filer:	Christopher J. Reckamp/Christine Wright
Filer Authorized By:	Christopher J. Reckamp
Attorney Docket Number:	00100.02.0053
Receipt Date:	04-DEC-2014
Filing Date:	12-JUN-2003
Time Stamp:	12:11:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$960
RAM confirmation Number	11328
Deposit Account	020390
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	020053_IssueFee.pdf	1597152 8c16e4ee97f56ba3cbe288bc72515e91cd6f9003	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30155 1f53dd067fd3af805c150fdbd8c3d519a3f62ba4	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1627307		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/459,797
Filing Date	June 12, 2003
First Named Inventor	Mark M. Leather
Art Unit	2628
Examiner Name	Joni Hsu
Attorney Docket Number	00100.02.0053

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.H./		US- 6,980,209 B1	12-27-2005	Donham et al.	
/J.H./		US- 5,550,962	08-27-1996	Nakamura et al.	
/J.H./		US- 5,818,469	10-06-1998	Lawless et al.	
/J.H./		US- 6,118,452	~~09-12-2000~~	Gannett	September 12, 2000
/J.H./		US- 6,353,439 B1	03-05-2002	Lindholm et al.	
/J.H./		US- 6,384,824 B1	05-07-2002	Morgan et al.	
/J.H./		US- 6,417,858 B1	07-09-2002	Bosch et al.	
/J.H./		US- 6,573,893 B1	06-03-2003	Naqvi et al.	
/J.H./		US- 6,650,327 B1	11-18-2003	Airey et al.	
/J.H./		US- 6,650,330 B2	11-18-2003	Lindholm et al.	
/J.H./		US- 6,724,394 B1	04-20-2004	Zatz et al.	
/J.H./		US- 6,731,289 B1	05-04-2004	Peercy et al.	
/J.H./		US- 6,809,732 B2	10-26-2004	Zatz et al.	
/J.H./		US- 6,864,893 B2	03-08-2005	Zatz	
/J.H./		US- 6,897,871 B1	05-24-2005	Morein et al.	
/J.H./		US- 7,015,913 B1	03-21-2006	Lindholm et al.	
/J.H./		US- 2003/0076320 A1	04-24-2003	Collodi	
/J.H./		US- 2005/0200629 A1	09-15-2005	Morein et al.	
/J.H./		US- 2004/0041814 A1	03-04-2004	Wyatt et al.	

Change(s) applied to document
/D.D./
10/18/2014

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Joni Hsu/	Date Considered	12/13/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	01/13/2015	8933945	00100.02.0053	4148

29153 7590 12/23/2014

ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1808 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Mark M. Leather, Saratoga, CA;
Eric Demers, Palo Alto, CA;

✎ AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Delaware on the following X Patents or Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
15cv1177-RGA	12/21/2015	DISTRICT OF DELAWARE

PLAINTIFF	DEFENDANT
Advanced Silicon Technologies, LLC	NVIDIA Corporation

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 6,339,428 B1	1/15/2002	Advanced Silicon Technologies, LLC
2	US 6,546,439 B1	4/8/2003	Advanced Silicon Technologies, LLC
3	US 6,630,935 B1	10/7/2003	Advanced Silicon Technologies, LLC
4	US 8,933,945 B2	1/13/2015	Advanced Silicon Technologies, LLC
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT
See attached Order

CLERK	(BY) DEPUTY CLERK	DATE
JOHN A. CERINO, CLERK OF COURT		5/3/2016

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**