UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/459,797	06/12/2003	Mark M. Leather	00100.02.0053	4148

29153 7590 06/26/2014
ADVANCED MICRO DEVICES, INC.
C/O Faegre Baker Daniels LLP
311 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER
RICHER, JONI

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
06/26/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteas@faegrebd.com
michelle.davis@faegrebd.com
cynthia.payson@faegrebd.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte MARC M. LEATHER and ERIC DEMERS

Appeal 2011-010197
Application 10/459,797
Technology Center 2600

Before ROBERT E. NAPPI, JASON V. MORGAN, and J. JOHN LEE, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) of the rejection of claims 1 through 7, 10 through 22, 24, and 25.

We affirm-in-part.

INVENTION

The invention is directed to a graphics processing circuit that includes at least two pipelines operative to process data in a corresponding set of tiles of a repeating tile pattern, a respective one of the at least two pipelines operative to process data in a dedicated tile. *See* Abstract of Appellants' Specification. Claim 1 is illustrative of the invention and reproduced below:

1. A graphics processing circuit, comprising:

at least two graphics pipelines on a same chip operative to process data in a corresponding set of tiles of a repeating tile pattern corresponding to screen locations, a respective one of the at least two graphics pipelines operative to process data in a dedicated tile; and

a memory controller on the chip in communication with the at least two graphics pipelines, operative to transfer pixel data between each of a first pipeline and a second pipeline and a memory shared among the at least two graphics pipelines;

wherein the repeating tile pattern includes a horizontally and vertically repeating pattern of square regions.

REJECTIONS AT ISSUE

The Examiner has rejected claims 1 through 4, 7, 10, 12, 14, and 25 under 35 U.S.C. § 103(a) as unpatentable over MacInnis (U.S. 6,570,579 B1; May 27, 2003) and Perego (U.S. 6,864,896 B2; Mar. 8, 2005). Answer 4-8.[1]

The Examiner has rejected claims 5, 18, and 24 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, and Kelleher (U.S. 5,794,016; Aug. 11, 1998). Answer 8-12.

The Examiner has rejected claims 6 and 17 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, and Furtner (U.S. 6,778,177 B1; Aug. 17, 2004). Answer 12-13.

The Examiner has rejected claims 11, 13, 15, and 16 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, Kelleher, and Hamburg (U.S. 5,905,506; May 18, 1999). Answer 13-14.

---

[1] Throughout this opinion we refer to the Appeal Brief dated February 22, 2011, Reply Brief dated June 6, 2011, and the Examiner's Answer mailed on April 5, 2011.

The Examiner has rejected claim 19 under 35 U.S.C. § 103(a) as unpatentable over MacInnis, Perego, Furtner and Kent (US 2003/0164830 A1; Sept. 4, 2003). Answer 14-16.

The Examiner has rejected claims 20 through 22 under 35 U.S.C. § 103(a) as unpatentable over Perego. Answer 16-18.

ISSUES

Rejection independent claims 1 and 25.

Appellants argue on pages 16 through 22 of the Appeal Brief and pages 1 and 2 of the Reply Brief, the Examiner's rejection of independent claims 1 and 25 is in error. The dispositive issue presented by this argument is: Did the Examiner err in finding that the combination of MacInnis and Perego teach a memory shared among the graphics pipelines?

Rejection independent claim 20.

Appellants argue on pages 27 and 28 of the Appeal Brief that the Examiner's rejection of claim 20 is in error. Appellants' argument with respect to this claim presents us with the issue: did the Examiner err in finding that Perego teaches passing the same pixel data to both of the graphics pipelines on the same chip?

Rejection independent claim 24.

Appellants argue on pages 22 and 23 of the Appeal Brief that the Examiner's rejection of claim 24 is in error. Appellants' argument with respect to this claim present us with the issue: did the Examiner err in

finding that the combination of MacInnis, Perego, and Kelleher teaches both the front end and the back end circuitry on the same chip as claimed?

ANALYSIS

We have reviewed Appellants' arguments in the Briefs, the Examiner's rejection and the Examiner's response to the Appellants' arguments. We agree with Appellants' conclusion that the Examiner erred rejecting claims 1 through 7, 10 through 22, and 25 under 35 U.S.C. § 103(a) but disagree with Appellants' conclusion the Examiner erred in rejecting claim 24 under 35 U.S.C. § 103(a).

Rejection independent claims 1 and 25.

The Examiner's response, to Appellants' arguments directed to the rejection of these claims, cites to Perego's teaching of memory (item 314 of Figure 3) which the Examiner finds is shared between the pipelines (items 312 of Figure 3). Answer 4, 5, 19, and 20. We disagree with the Examiner's finding. As argued by Appellants on page 17 of the Appeal Brief, Perego teaches item 314 is a shared memory, but it is shared between the CPU and the individual rendering engines and not shared among the rendering engines (which the Examiner equates to graphics pipelines) as claimed. The Examiner has not found that MacInnis teaches this feature. Thus, we do not find the Examiner has shown that combination of MacInnis and Perego teaches all of the limitations of independent claims 1 and 25. Accordingly, we will not sustain the Examiner's rejection of claims 1

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.