IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Mark M. Leather et al.	Examiner: Joni Hsu
Application No.: 10/459,797	Group Art Unit: 2628
Filed: June 12, 2003	Docket No.: 00100.02.0053
For: **DIVIDING WORK AMONG MULTIPLE GRAPHICS PIPELINES USING A SUPER-TILING TECHNIQUE**	

APPELLANTS' REPLY BRIEF IN RESPONSE TO EXAMINER'S ANSWER

Dear Sir:

Appellants wish to thank the Examiner for the "Response to Argument" set forth in the Examiner's Answer. Appellants respectfully reiterate their prior remarks as it appears that the claim construction and teachings of Perego are incorrect. Appellants again respectfully submit that the claims must be reasonably interpreted in view of the Specification and that the claims themselves contradict the Examiner's construction as do the actual teachings of the Perego reference which were not addressed in the Examiner's "Response to Arguments" section. Claim 1, for example, recites the memory controller on the chip in communication with at least two graphics pipelines, operative to transfer pixel data between each of the first pipeline and a second pipeline in a memory shared among the at least two graphics pipelines… As such, the same memory controller that is on the chip is in communication with two graphics pipelines and the memory is shared among the at least two graphics pipelines. The Examiner's position appears to overlook what the Perego reference actually teaches as being shared. What is shared in Perego is memory between a CPU and a single rendering engine which is specifically described and shown in Perego as a memory module 304 or 804 including a rendering engine 312 and dedicated

memory that the CPU can access but no other rendering engine can access. Only a single rendering engine can access the memory on a memory module.

FIG. 8 clearly shows this structure since each rendering engine only has access to its own memory devices. Appellants claim a different configuration wherein the same memory controller on a chip is in communication with shared memory that is shared between two graphics processors. The graphics rendering engines in Perego cannot share memory amongst graphics engines and do not incorporate a common memory controller to do so. Perego uses the term "shared memory" because a portion of the memory on each separate memory module is used by the CPU, the claims do not claim such an operation but instead claim that the memory controller on the chip is in communication with multiple graphics pipelines and transfers pixel data between each of the pipelines and the memory controller that is in communication with a memory shared among the at least two graphics pipelines. Multiple rendering engines in Perego do not share the same graphics memory through a common memory controller on a chip as alleged in the office action. Accordingly, Appellants respectfully reversal of the rejections.

Appellants also respectfully reassert their other remarks from their Brief.

Respectfully submitted,

Date: June 6, 2011

By: /Christopher J. Reckamp/
Christopher J. Reckamp
Registration No. 34,414

Vedder Price P.C.
222 N. LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7599
FAX: (312) 609-5005